# 74AHC374-Q100; 74AHCT374-Q100

## Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 1 — 11 March 2014 Product data sheet

## 1. General description

The 74AHC374-Q100; 74AHCT374-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC374-Q100; 74AHCT374-Q100 comprises eight D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock input (CP) and an output enable input ($\overline{OE}$) are common to all flip-flops.

The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold times requirements for the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW the content of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than $V_{CC}$
- Common 3-state output enable input
- Input levels:
  - For 74AHC374-Q100: CMOS level
  - For 74AHCT374-Q100: TTL level
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

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## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| **74AHC374-Q100** | | | | |
| 74AHC374D-Q100 | −40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHC374PW-Q100 | −40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| **74AHCT374-Q100** | | | | |
| 74AHCT374D-Q100 | −40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHCT374PW-Q100 | −40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |

## 4. Functional diagram

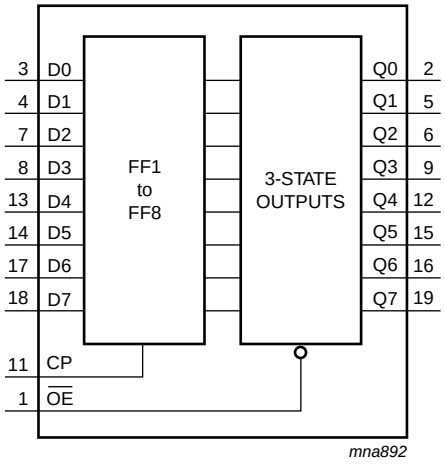



**Fig 1. Functional diagram**

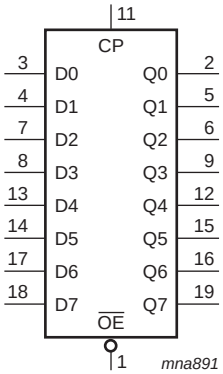



**Fig 2. Logic symbol**

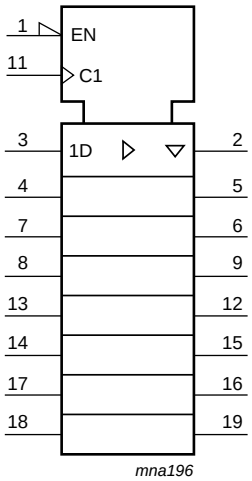



**Fig 3. IEC logic symbol**

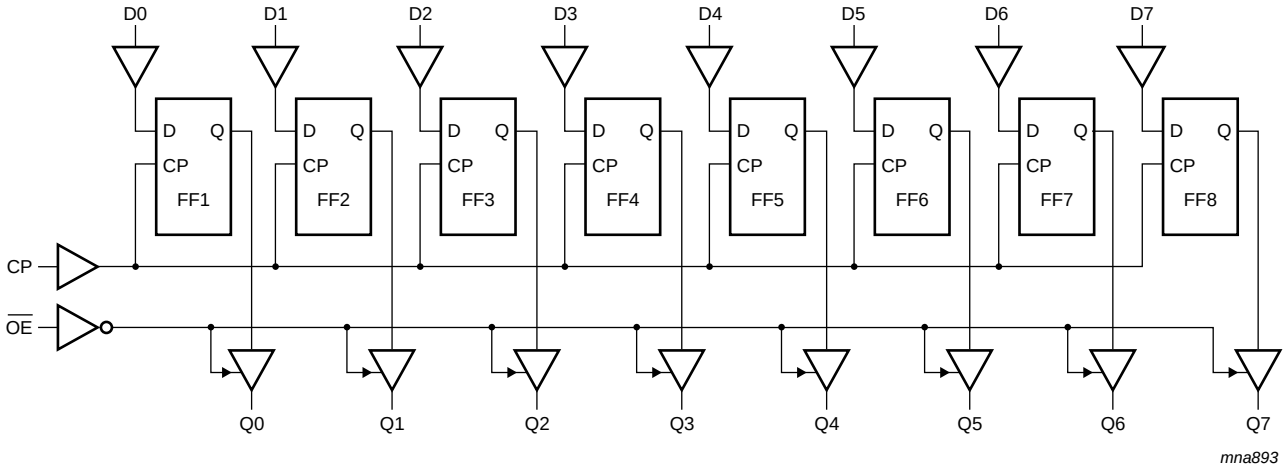



**Fig 4. Logic diagram**

# 5. Pinning information

## 5.1 Pinning

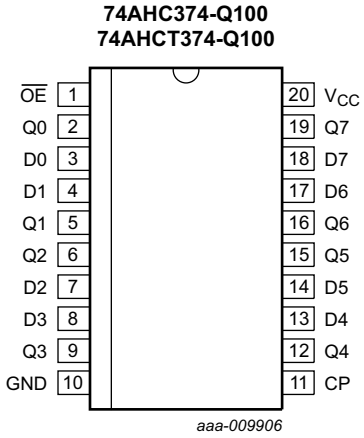



**Fig 5. Pin configuration SO20 and TSSOP20**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}$ | 1 | 3-state output enable input (active LOW) |
| Q0 | 2 | 3-state flip-flop output |
| D0 | 3 | data input |
| D1 | 4 | data input |
| Q1 | 5 | 3-state flip-flop output |
| Q2 | 6 | 3-state flip-flop output |
| D2 | 7 | data input |
| D3 | 8 | data input |
| Q3 | 9 | 3-state flip-flop output |
| GND | 10 | ground (0 V) |
| CP | 11 | clock input (LOW-to-HIGH, edge triggered) |
| Q4 | 12 | 3-state flip-flop output |
| D4 | 13 | data input |
| D5 | 14 | data input |
| Q5 | 15 | 3-state flip-flop output |
| Q6 | 16 | 3-state flip-flop output |
| D6 | 17 | data input |
| D7 | 18 | data input |
| Q7 | 19 | 3-state flip-flop output |
| $V_{CC}$ | 20 | supply voltage |

# 6. Functional description

**Table 3. Function table[1]**

| Operating mode | Control | | Input | Internal flip-flop | Output |
|---|---|---|---|---|---|
| | $\overline{OE}$ | CP | Dn | | Q0 to Q7 |
| Load and read register | L | ↑ | l | L | L |
| | L | ↑ | h | H | H |
| Load register and disable outputs | H | ↑ | l | L | Z |
| | H | ↑ | h | H | Z |

[1] H = HIGH voltage level;
h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH CP transition;
Z = high-impedance OFF-state.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7.0 | V |
| $V_I$ | input voltage | | | −0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V | [1] | −20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | −20 | +20 | mA |
| $I_O$ | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | | −25 | +25 | mA |
| $I_{CC}$ | supply current | | | - | +75 | mA |
| $I_{GND}$ | ground current | | | −75 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 packages: above 70 °C the value of $P_{tot}$ derates linearly at 8 mW/K.
For TSSOP20 packages: above 60 °C the value of $P_{tot}$ derates linearly at 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **74AHC374-Q100** | | | | | | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 100 | ns/V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 20 | ns/V |
| **74AHCT374-Q100** | | | | | | |
| $V_{CC}$ | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 20 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC374-Q100** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –50 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = –8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8.0 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| $C_I$ | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| $C_O$ | output capacitance | | - | 4 | - | - | - | - | - | pF |
| **74AHCT374-Q100** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = –50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I = V_{CC}$ – 2.1 V; other pins at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| $C_I$ | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| $C_O$ | output capacitance | | - | 4 | - | - | - | - | - | pF |

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| **74AHC374-Q100** | | | | | | | | | | |
| $t_{pd}$ | propagation delay | CP to Qn; see Figure 6 and Figure 8 [2] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 6.4 | 12.7 | 1.0 | 15.0 | 1.0 | 16.0 | ns |
| | | $C_L$ = 50 pF | - | 8.4 | 16.2 | 1.0 | 18.5 | 1.0 | 20.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.4 | 8.1 | 1.0 | 9.5 | 1.0 | 10.0 | ns |
| | | $C_L$ = 50 pF | - | 5.7 | 10.1 | 1.0 | 11.5 | 1.0 | 12.5 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 7 [3] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.5 | 11.0 | 1.0 | 13.0 | 1.0 | 14.0 | ns |
| | | $C_L$ = 50 pF | - | 7.3 | 14.5 | 1.0 | 16.5 | 1.0 | 18.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.9 | 7.6 | 1.0 | 9.0 | 1.0 | 9.5 | ns |
| | | $C_L$ = 50 pF | - | 5.2 | 9.6 | 1.0 | 11.0 | 1.0 | 12.0 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 7 [4] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.6 | 10.5 | 1.0 | 12.5 | 1.0 | 13.0 | ns |
| | | $C_L$ = 50 pF | - | 9.4 | 14.0 | 1.0 | 16.0 | 1.0 | 17.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.2 | 6.8 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| | | $C_L$ = 50 pF | - | 6.4 | 8.8 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| $f_{max}$ | maximum frequency | see Figure 6 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | 80 | 130 | - | 70 | - | 70 | - | MHz |
| | | $C_L$ = 50 pF | 55 | 85 | - | 50 | - | 50 | - | MHz |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | 130 | 185 | - | 110 | - | 110 | - | MHz |
| | | $C_L$ = 50 pF | 85 | 120 | - | 75 | - | 75 | - | MHz |
| $t_W$ | pulse width | CP HIGH or LOW; see Figure 6 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 5.0 | - | - | 5.5 | - | 5.5 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 4.5 | - | - | 4.0 | - | 4.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 3.0 | - | - | 3.0 | - | 3.0 | - | ns |

**Table 7. Dynamic characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_h$ | hold time | Dn to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.0 | - | - | 2.0 | - | 2.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ [5] | - | 10 | - | - | - | - | - | pF |
| **74AHCT374-Q100; $V_{CC}$ = 4.5 V to 5.5 V** | | | | | | | | | | |
| $t_{pd}$ | propagation delay | CP to Qn; see Figure 6 and Figure 8 [2] | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.3 | 9.4 | 1.0 | 10.5 | 1.0 | 12.0 | ns |
| | | $C_L$ = 50 pF | - | 5.6 | 10.4 | 1.0 | 11.5 | 1.0 | 13.0 | ns |
| $t_{en}$ | enable time | OE to Qn; see Figure 7 [3] | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.5 | 10.2 | 1.0 | 11.5 | 1.0 | 13.0 | ns |
| | | $C_L$ = 50 pF | - | 4.8 | 11.2 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| $t_{dis}$ | disable time | OE to Qn; see Figure 7 [4] | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.6 | 10.2 | 1.0 | 11.0 | 1.0 | 13.0 | ns |
| | | $C_L$ = 50 pF | - | 5.7 | 11.2 | 1.0 | 12.0 | 1.0 | 14.0 | ns |
| $f_{max}$ | maximum frequency | see Figure 6 | | | | | | | | |
| | | $C_L$ = 15 pF | 90 | 140 | - | 80 | - | 80 | - | MHz |
| | | $C_L$ = 50 pF | 85 | 130 | - | 75 | - | 75 | - | MHz |
| $t_W$ | pulse width | CP HIGH or LOW; see Figure 6 | 6.5 | - | - | 6.5 | - | 6.5 | - | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| $t_h$ | hold time | Dn to CP; see Figure 8 | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ [5] | - | 12 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V and $V_{CC}$ = 5.0 V).

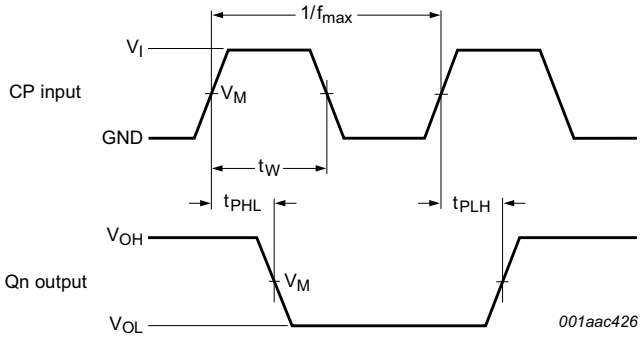
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[4] $t_{dis}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

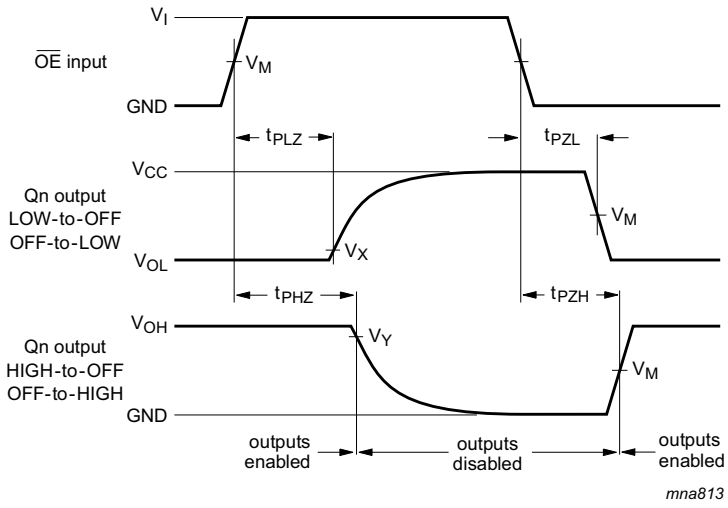
## 10.1 Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

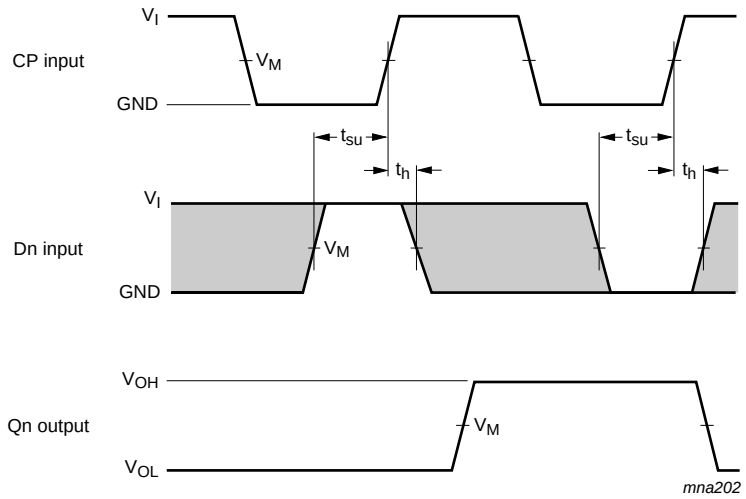
**Fig 6. Clock pulse width, maximum frequency and input to output propagation delays**




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**




Measurement points are given in Table 8.

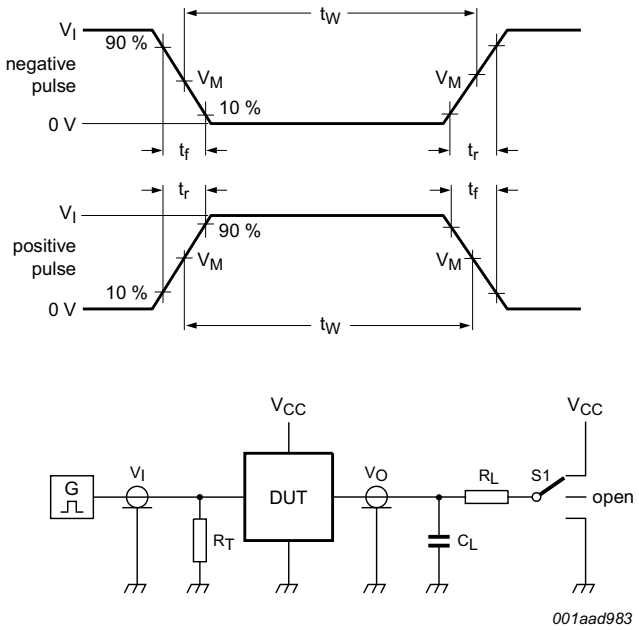
The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 8. Data set-up and hold times**

**Table 8. Measurement points**

| Type | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 74AHC374-Q100 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |
| 74AHCT374-Q100 | 1.5 V | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = load capacitance including jig and probe capacitance.

$R_L$ = load resistance.

S1 = test selection switch.

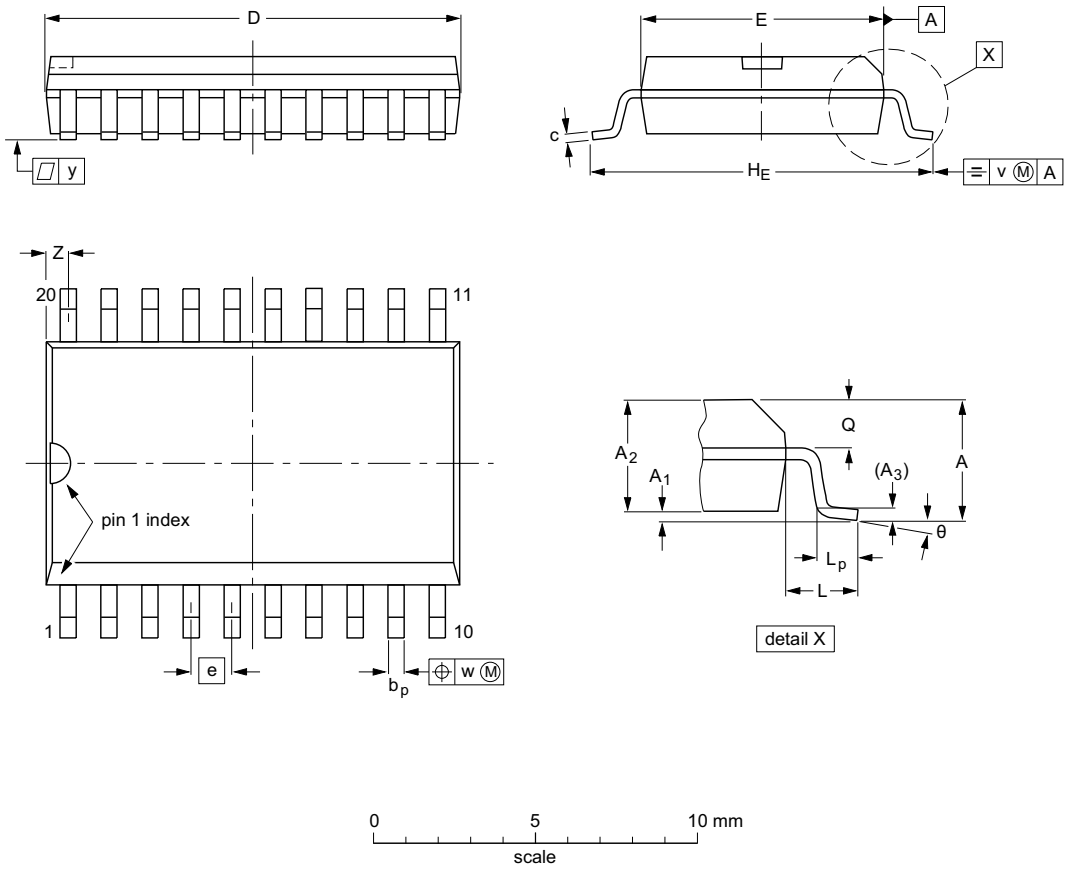
**Fig 9. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load | | S1 position |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ |
| 74AHC374-Q100 | $V_{CC}$ | ≤ 3.0 ns | 15 pF, 50 pF | 1 kΩ | open |
| 74AHCT374-Q100 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | 1 kΩ | open |

## 11. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

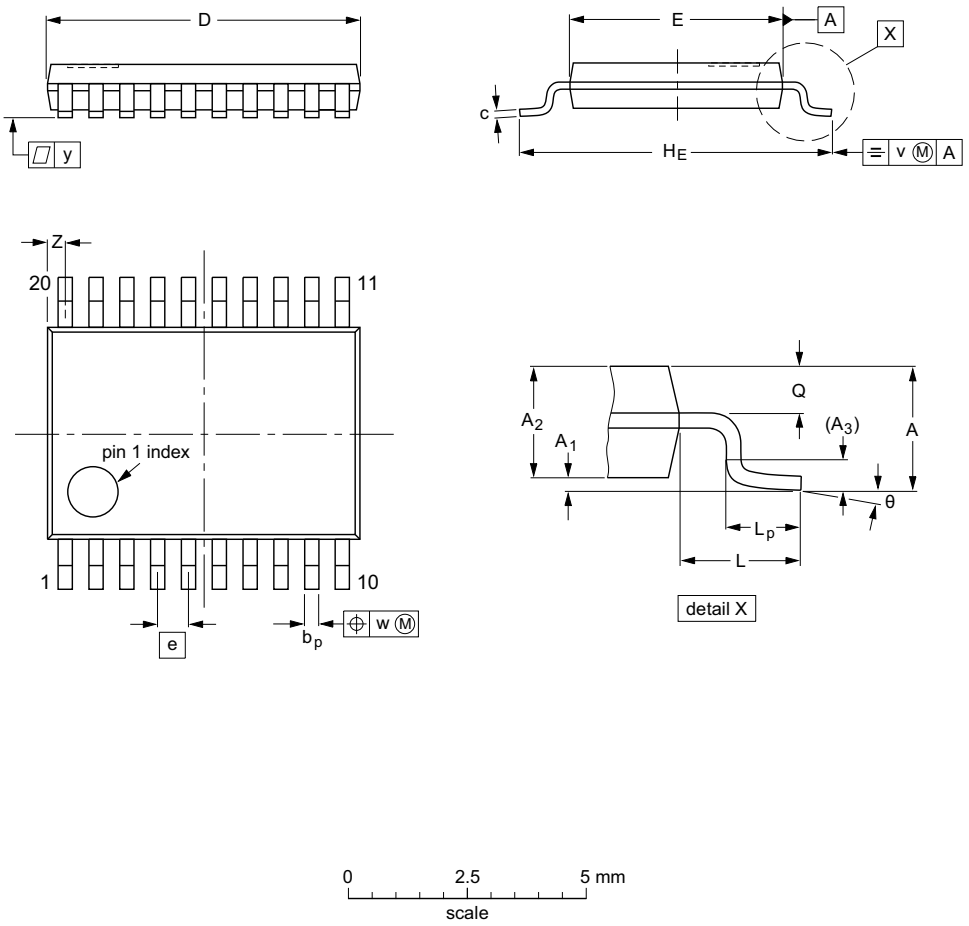
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT163-1 (SO20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 11. Package outline SOT360-1 (TSSOP20)**

## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MIL | Military |
| MM | Machine Model |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AHC_AHCT374_Q100 v.1 | 20140311 | Product data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 16. Contents





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**Date of release: 11 March 2014**