

# DATA SHEET

## **74ALS563A/74ALS564A** Latch flip/flop

Product specification  
IC05 Data Handbook

1996 Jul 01

## Latch/flip-flop

## 74ALS563A/74ALS564A

74ALS563A Octal transparent latch, inverting (3-State)

74ALS564A Octal D flip-flop, inverting (3-State)

## FEATURES

- 74ALS563A is broadside pinout and inverting version of 74ALS373
- 74ALS564A is broadside pinout and inverting version of 74ALS374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- 74ALS573A and 74ALS574A are non-inverting version of 74ALS563B and 74ALS564A respectively

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS563A	6.0ns	12mA
74ALS564A	6.0ns	15mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	74ALS563AN, 74ALS564AN	SOT146-1
20-pin plastic SOL	74ALS563AD, 74ALS564AD	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/2.0	20 $\mu$ A/0.2mA
E (74ALS563A)	Enable input	1.0/1.0	20 $\mu$ A/0.1mA
$\overline{OE}$	Output enable input (active-Low)	1.0/1.0	20 $\mu$ A/0.1mA
CP (74ALS564A)	Clock pulse input (active rising edge)	1.0/2.0	20 $\mu$ A/0.2mA
$\overline{Q}0$ – $\overline{Q}7$	Data outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

## DESCRIPTION

The 74ALS563A is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ( $\overline{OE}$ ) control gates.

The 74ALS563A is a complementary version of the 74ALS373 and has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the inverted data that is present one setup time before the High-to-Low enable transition.

The 74ALS564A is a complementary version of the 74ALS373 and has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ( $\overline{OE}$ ) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

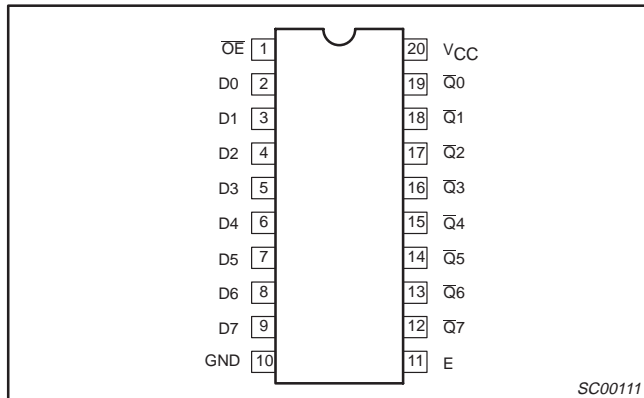
The active-Low output enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation. When  $\overline{OE}$  is Low, latched or transparent data appears at the output.

When  $\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

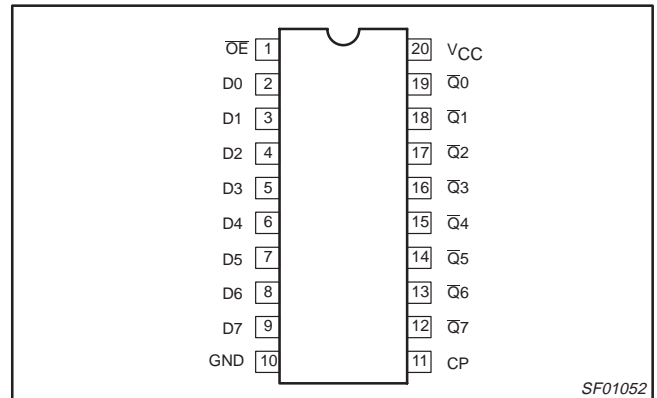
# Latch/flip-flop

# 74ALS563A/74ALS564A

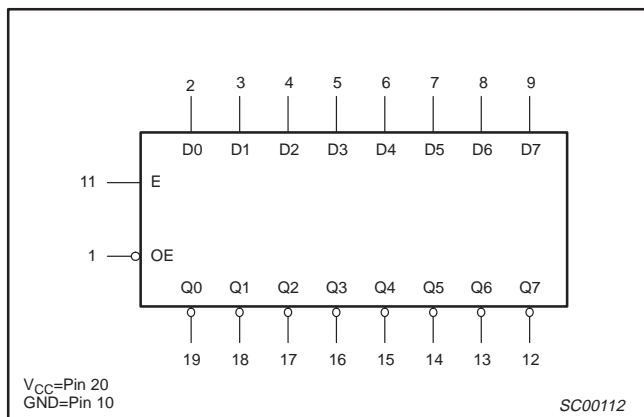
## PIN CONFIGURATION – 74ALS563A



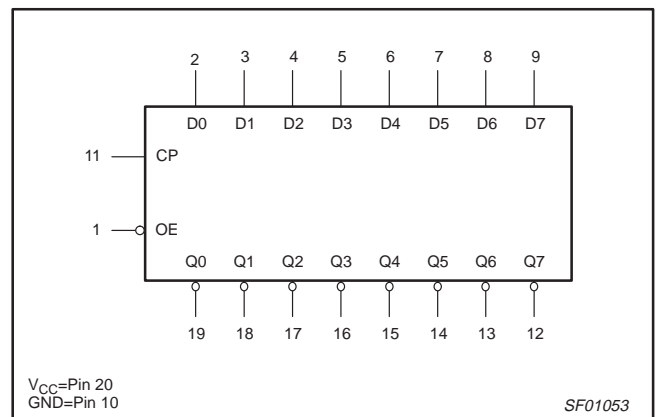
## PIN CONFIGURATION – 74ALS564A



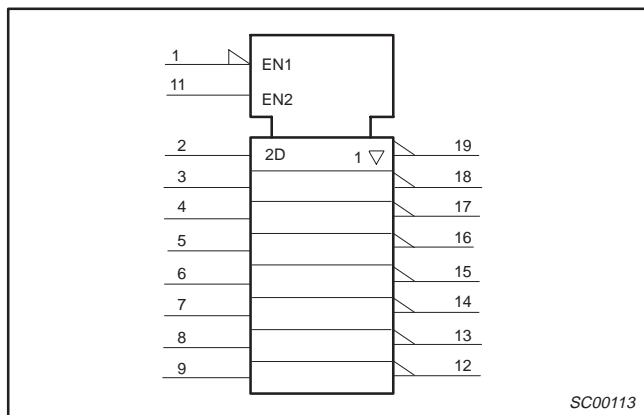
## LOGIC SYMBOL – 74ALS563A



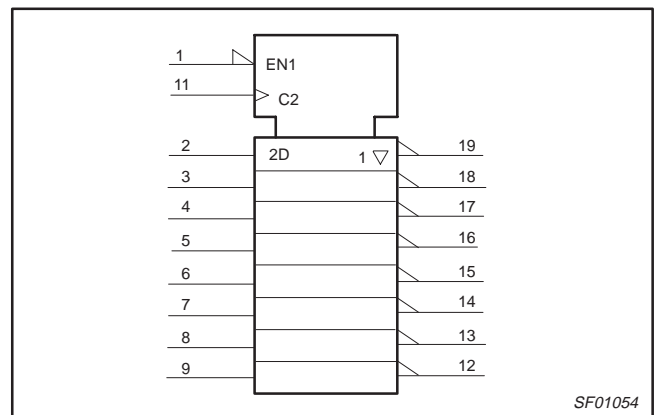
## LOGIC SYMBOL – 74ALS564A



## IEC/IEEE SYMBOL – 74ALS563A



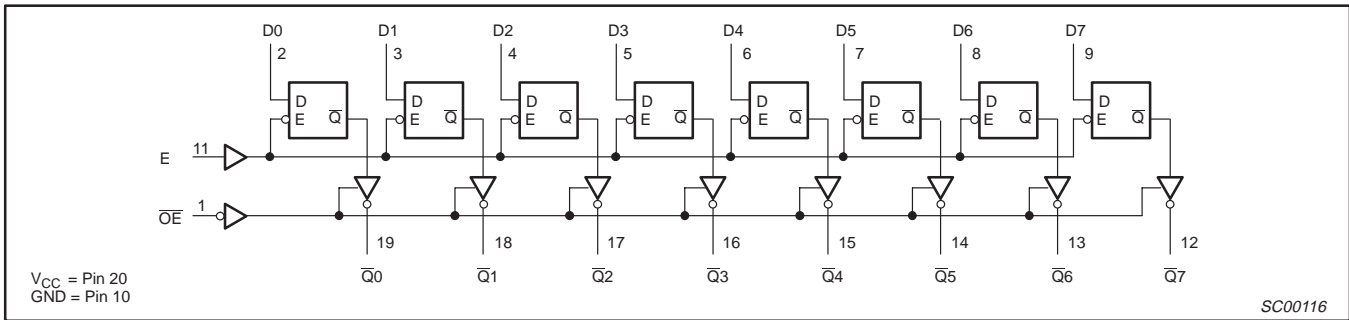
## IEC/IEEE SYMBOL – 74ALS564A



# Latch/flip-flop

# 74ALS563A/74ALS564A

## LOGIC DIAGRAM – 74ALS563A



## FUNCTION TABLE – 74ALS563A

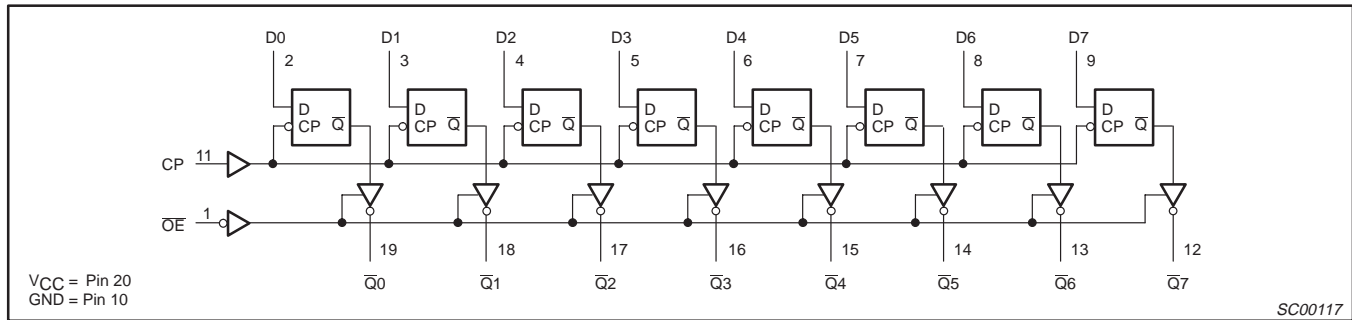
INPUTS			OUTPUTS REGISTER	INTERNAL	OPERATING MODE
$\overline{OE}$	E	D <sub>n</sub>		$\overline{Q0} - \overline{Q7}$	
L	H	L	L	H	Enable and read register
L	H	H	H	L	
L	↓	l	L	H	Latch and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D <sub>n</sub>	D <sub>n</sub>	Z	

- H = High voltage level
- h = High state must be present one setup time before the High-to-Low enable transition
- L = Low voltage level
- l = Low state must be present one setup time before the High-to-Low enable transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-Low enable transition

# Latch/flip-flop

# 74ALS563A/74ALS564A

## LOGIC DIAGRAM – 74ALS564A



## FUNCTION TABLE – 74ALS564A

INPUTS			OUTPUTS REGISTER	INTERNAL	OPERATING MODE
$\overline{OE}$	CP	Dn		$\overline{Q0} - \overline{Q7}$	
L	$\uparrow$	l	L	H	Load and read register
L	$\uparrow$	h	H	L	
L	$\updownarrow$	X	NC	NC	Hold
H	$\updownarrow$	X	NC	Z	Disable outputs
H	$\uparrow$	Dn	Dn	Z	

- H = High voltage level
- h = High state must be present one setup time before the Low-to-High clock transition
- L = Low voltage level
- l = Low state must be present one setup time before the Low-to-High clock transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- $\uparrow$  = Low-to-High clock transition
- $\updownarrow$  = Not Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	48	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## Latch/flip-flop

## 74ALS563A/74ALS564A

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-2.6	mA
$I_{OL}$	Low-level output current			24	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
				MIN	TYP <sup>2</sup>	MAX		
$V_{OH}$	High-level output voltage		$V_{CC} = \pm 10\%$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$	$I_{OH} = -0.4\text{mA}$	$V_{CC} - 2$		V	
				$I_{OH} = \text{MAX}$	2.4	3.2	V	
$V_{OL}$	Low-level output voltage		$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$	$I_{OL} = 12\text{mA}$		0.25	0.40	V
				$I_{OL} = 24\text{mA}$		0.35	0.50	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}$ , $I_I = I_{IK}$		-0.73	-1.5	V	
$I_I$	Input current at maximum input voltage		$V_{CC} = \text{MAX}$ , $V_I = 7.0\text{V}$			0.1	mA	
$I_{IH}$	High-level input current		$V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	74ALS563A	$V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$			-0.1	mA	
		74ALS564A				-0.2	mA	
$I_{OZH}$	Off-state output current, High-level voltage applied		$V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$	
$I_{OZL}$	Off-state output current, Low-level voltage applied		$V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$			-20	$\mu\text{A}$	
$I_O$	Output current <sup>3</sup>		$V_{CC} = \text{MAX}$ , $V_O = 2.25\text{V}$	-30		-112	mA	
$I_{CC}$	Supply current (total)		74ALS563A	$I_{CCH}$	$V_{CC} = \text{MAX}$	7	12	mA
				$I_{CCL}$		13	21	mA
				$I_{CCZ}$		15	24	mA
			74ALS564A	$I_{CCH}$		11	18	mA
				$I_{CCL}$		17	27	mA
				$I_{CCZ}$		18	28	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## Latch/flip-flop

## 74ALS563A/74ALS564A

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT	
			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$			
			MIN	MAX		
$t_{PLH}$ $t_{PHL}$	Propagation delay Dn to $\bar{Q}_n$	74ALS563A	Waveform 3	2.0 3.0	10.0 10.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay E to $\bar{Q}_n$		Waveform 2	4.0 4.0	13.0 13.0	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to High or Low level		Waveform 6 Waveform 7	1.0 3.0	9.0 11.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from High or Low level		Waveform 6 Waveform 7	1.0 2.0	9.0 11.0	ns
$f_{MAX}$	Maximum clock frequency	74ALS564A	Waveform 1	45		MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $\bar{Q}_n$		Waveform 1	3.0 4.0	12.0 12.0	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to High or Low level		Waveform 6 Waveform 7	1.0 3.0	9.0 11.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from High or Low level		Waveform 6 Waveform 7	1.0 2.0	9.0 11.0	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT	
			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$			
			MIN	MAX		
$t_{su(H)}$ $t_{su(L)}$	Setup time, High or Low Dn to E	74ALS563A	Waveform 4	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E		Waveform 4	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	10.0		ns
$t_{su(H)}$ $t_{su(L)}$	Setup time, High or Low Dn to CP	74ALS564A	Waveform 5	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP		Waveform 5	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 5	7.0 11.0		ns

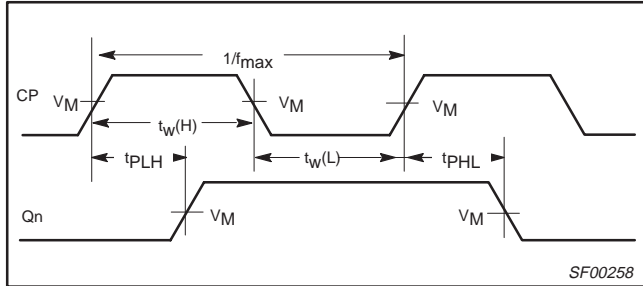
# Latch/flip-flop

# 74ALS563A/74ALS564A

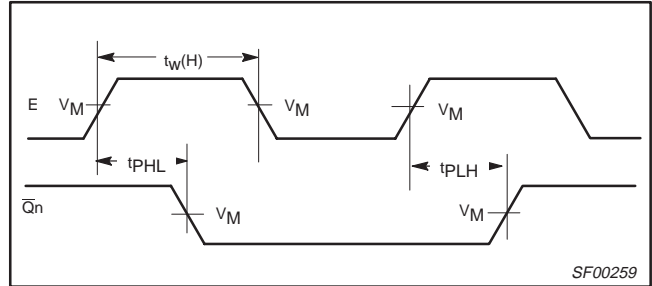
## AC WAVEFORMS

For all waveforms,  $V_M = 1.3V$ .

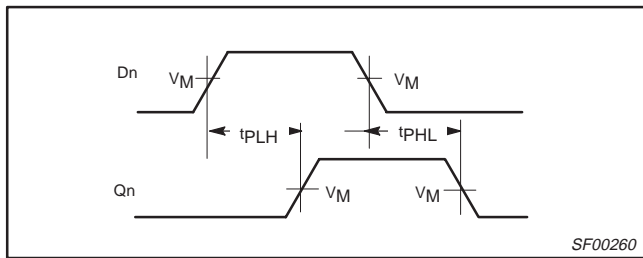
The shaded areas indicate when the input is permitted to change for predictable output performance.



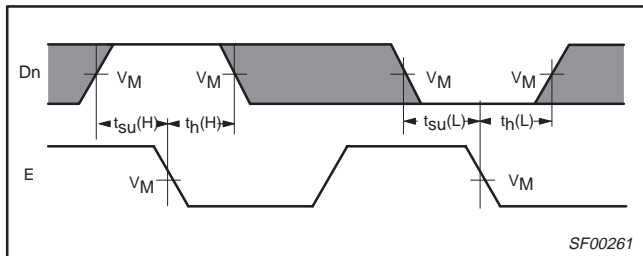
**Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency**



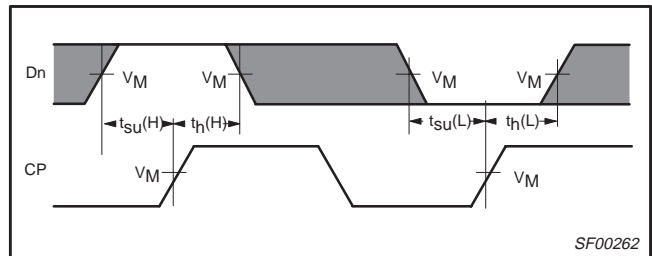
**Waveform 2. Propagation Delay for Enable to Output and Enable Pulse Width**



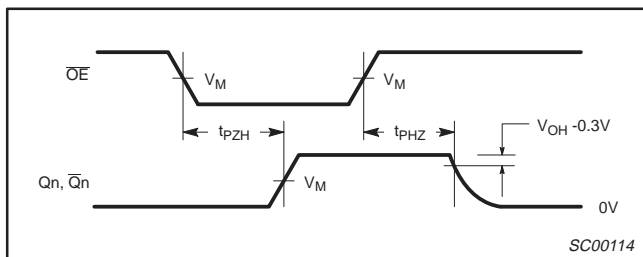
**Waveform 3. Propagation Delay for Data to Output**



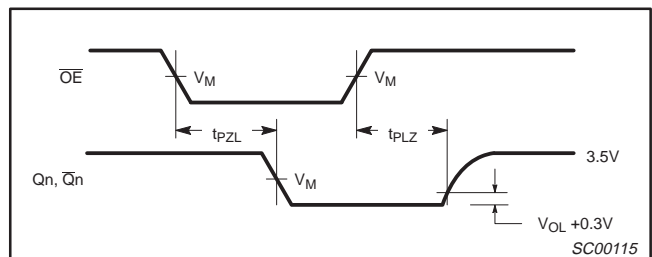
**Waveform 4. Data Setup Time and Hold Times**



**Waveform 5. Data Setup Time and Hold Times**



**Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



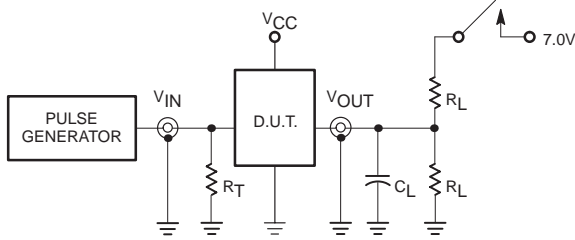
**Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**



# Latch/flip-flop

# 74ALS563A/74ALS564A

## TEST CIRCUIT AND WAVEFORMS



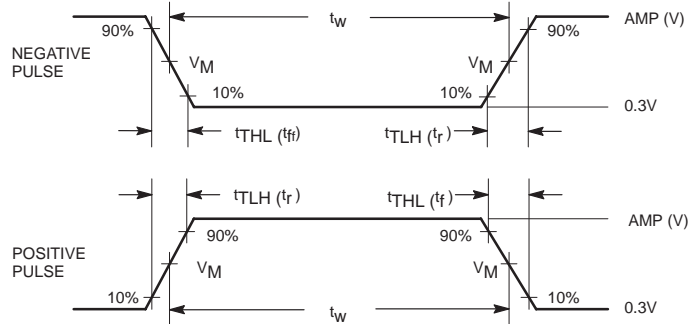
Test Circuit for 3-State Outputs

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$ , $t_{PZL}$	closed
All other	open

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

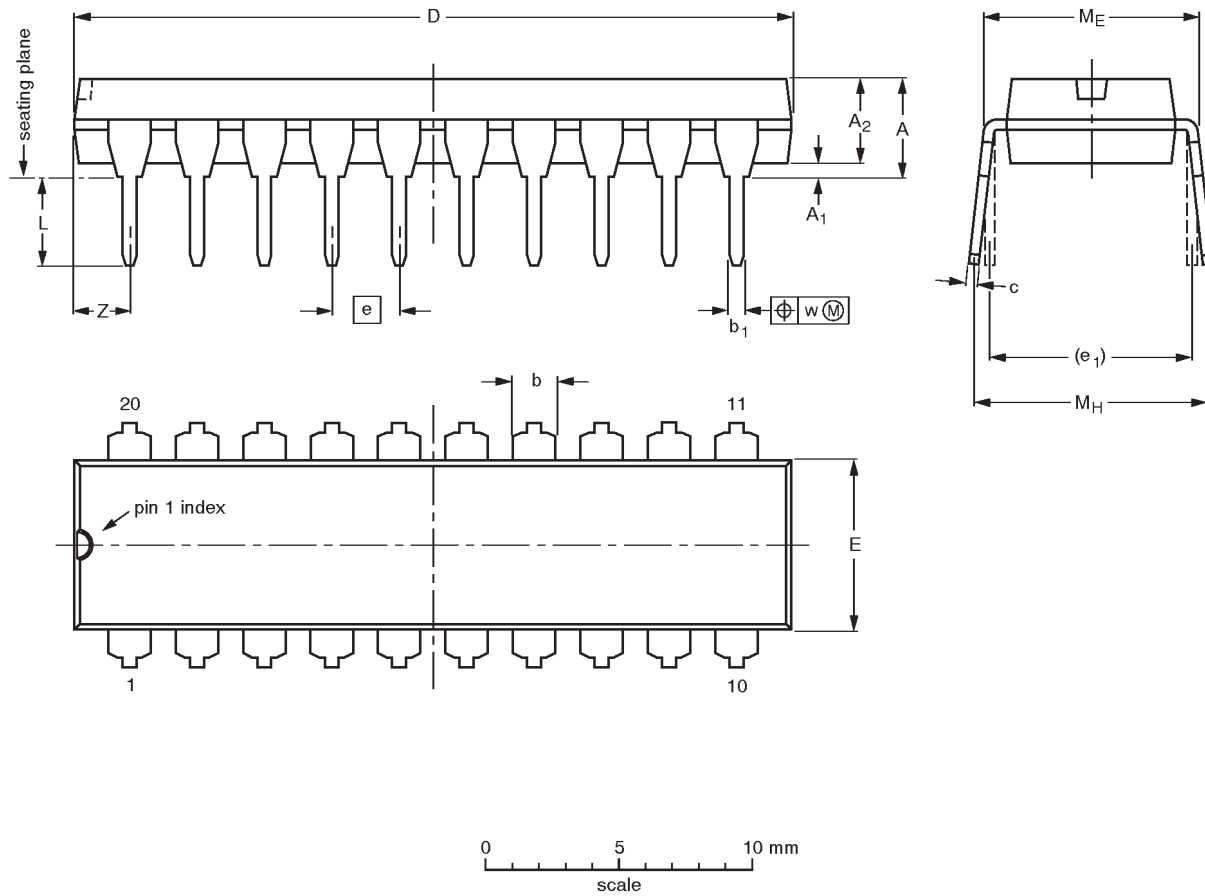
Family	INPUT PULSE REQUIREMENTS					
	Amplitude	$V_M$	Rep.Rate	$t_w$	$t_{TLH}$	$t_{THL}$
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072

# Latch flip-flop

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

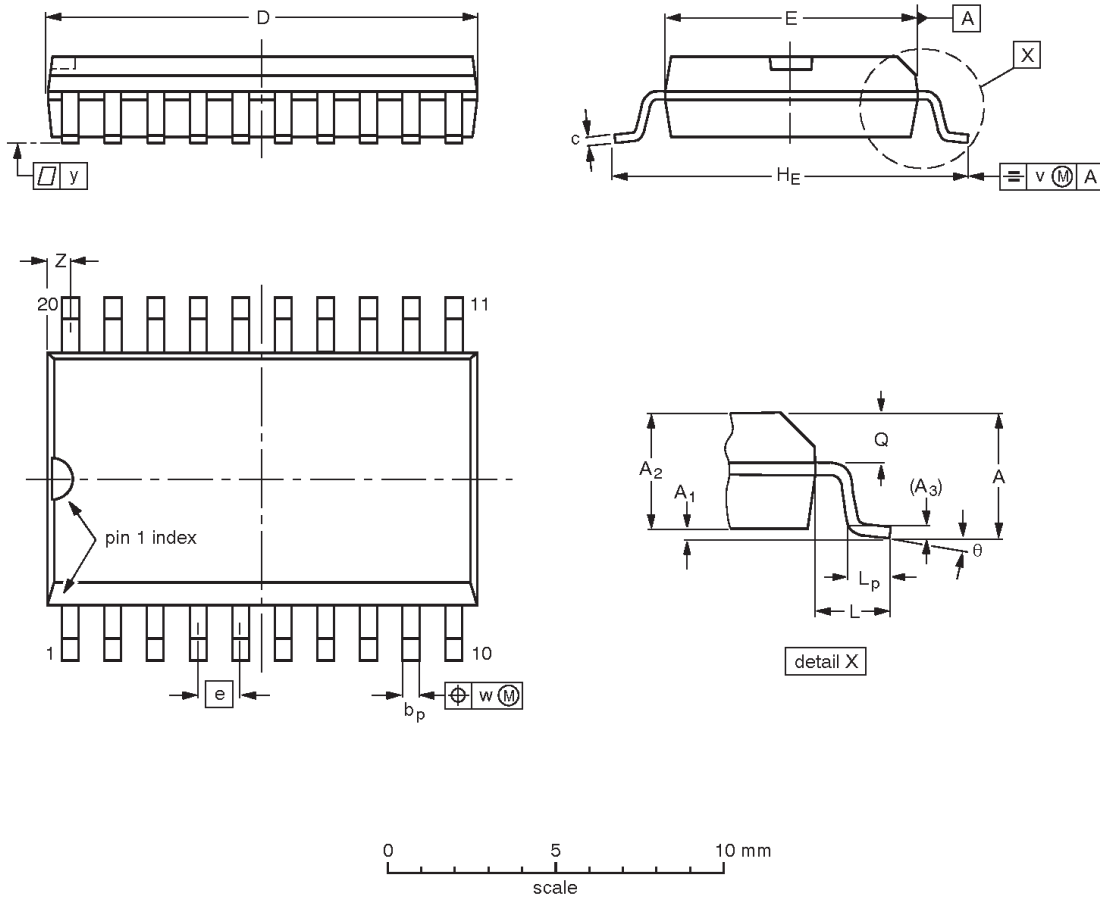
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Latch flip-flop

**SO20: plastic small outline package; 20 leads; body width 7.5 mm**

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

# Latch flip-flop

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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