

# 74ALVCH16823

18-bit bus-interface D-type flip-flop with reset and enable;  
3-state

Rev. 3 — 1 February 2018

Product data sheet

## 1 General description

The 74ALVCH16823 is a 18-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. Incorporates bushold data inputs which eliminate the need for external pull-up resistors to hold unused inputs. The 74ALVCH16823 consists of two sections of nine edge-triggered flip-flops. A clock (nCP) input, an output-enable (n $\overline{OE}$ ) input, a master reset (n $\overline{MR}$ ) input and a clock-enable (n $\overline{CE}$ ) input are provided for each total 9-bit section.

With the clock-enable (n $\overline{CE}$ ) input LOW, the D-type flip-flops will store the state of their individual nDn-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH nCP transition. Taking n $\overline{CE}$  HIGH disables the clock buffer, thus latching the outputs. Taking the master reset (n $\overline{MR}$ ) input LOW causes all the nQn outputs to go LOW independently of the clock.

When n $\overline{OE}$  is LOW, the contents of the flip-flops are available at the outputs. When the n $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the n $\overline{OE}$  input does not affect the state of flip-flops.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## 2 Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Current drive  $\pm 24$  mA at 3.0 V
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V<sub>CC</sub> and GND pins for minimum noise and ground bounce
- Output drive capability 50  $\Omega$  transmission lines at 85°C
- All data inputs have bushold
- Complies with JEDEC standard no. 8-1A
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

### 3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVCH16823DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

### 4 Functional diagram

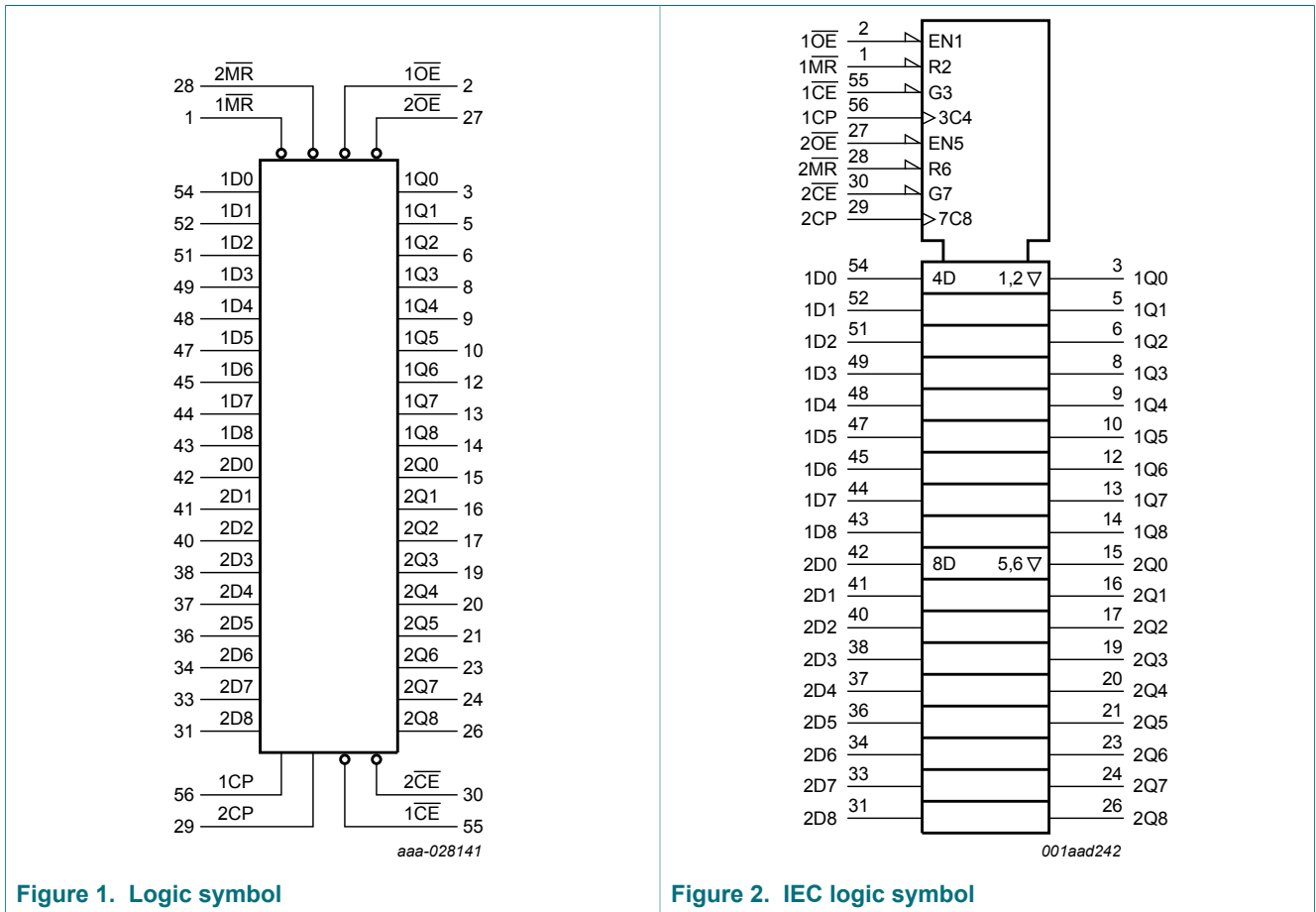


Figure 1. Logic symbol

Figure 2. IEC logic symbol

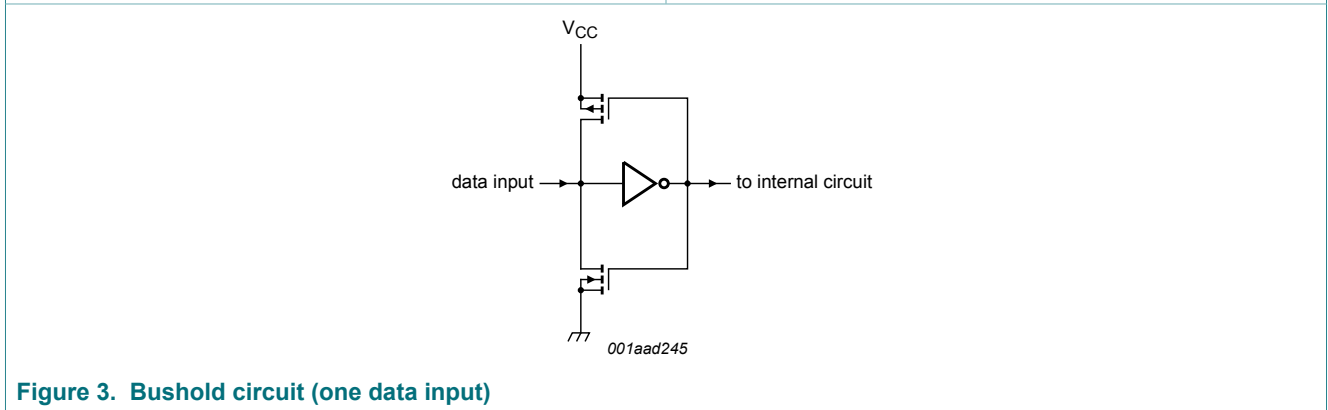


Figure 3. Bushold circuit (one data input)

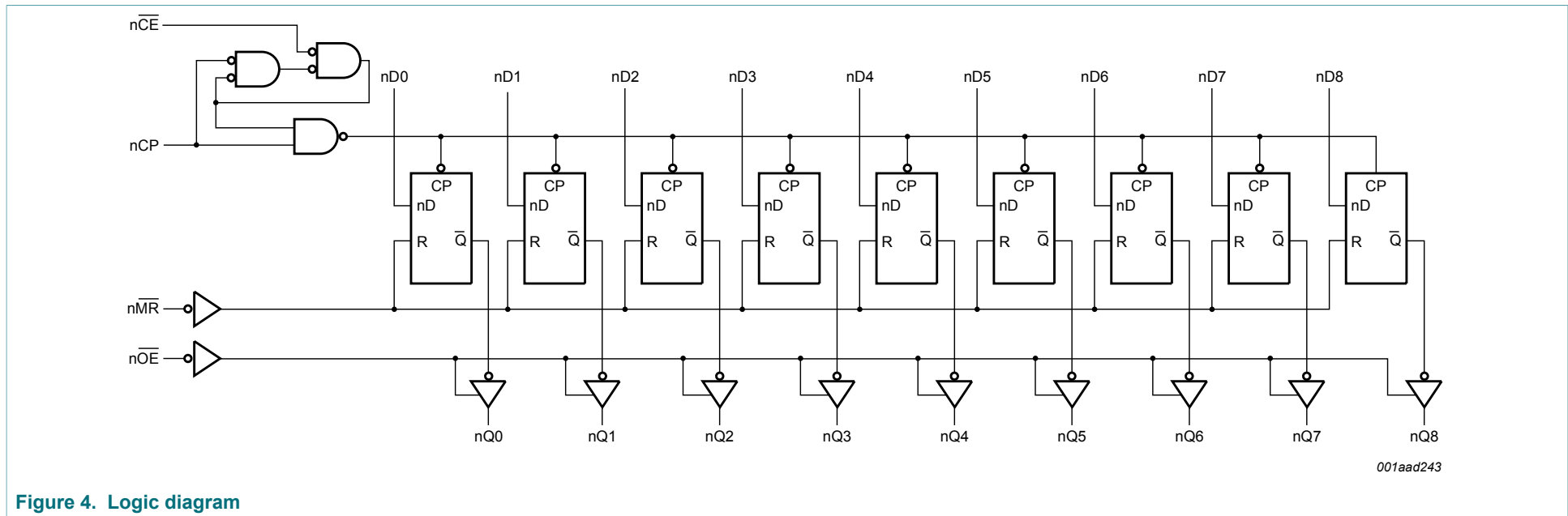


Figure 4. Logic diagram

## 5 Pinning information

### 5.1 Pinning

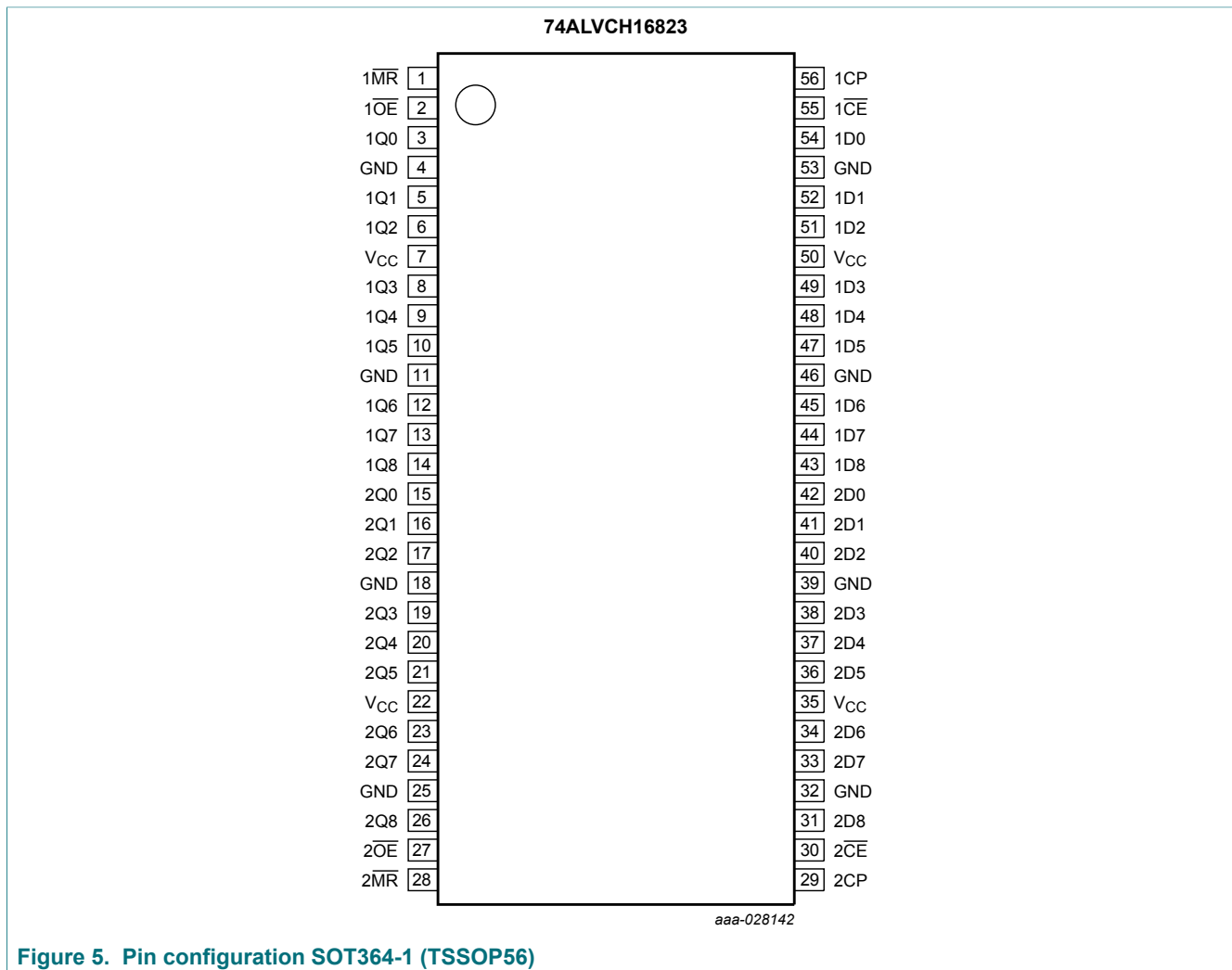


Figure 5. Pin configuration SOT364-1 (TSSOP56)

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8	54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8	3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8	42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8	15, 16, 17, 19, 20, 21, 23, 24, 26	data outputs
1 $\overline{\text{MR}}$ , 2 $\overline{\text{MR}}$	1, 28	master reset inputs (active-LOW)
1 $\overline{\text{OE}}$ , 2 $\overline{\text{OE}}$	2, 27	output enable inputs (active LOW)
1CP, 2CP	56, 29	clock pulse inputs (active rising edge)
1 $\overline{\text{CE}}$ , 2 $\overline{\text{CE}}$	55, 30	clock enable inputs (active-LOW)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V <sub>CC</sub>	7, 22, 35, 50	supply voltage

## 6 Functional description

Table 3. Function table <sup>[1]</sup>

Operating mode	Input					Output
	n $\overline{\text{OE}}$	n $\overline{\text{MR}}$	n $\overline{\text{CE}}$	nCP	nDn	nQn
clear	L	L	X	X	X	L
load and read data	L	H	L	↑	h	H
	L	H	L	↑	l	L
hold	L	H	L	L	X	NC
	L	H	H	X	X	NC
disable outputs	H	X	X	X	X	Z

- [1] H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
NC = no change;  
X = don't care;  
Z = high-impedance OFF-state;

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage	For control pins <sup>[1]</sup>	-0.5	+5.5	V
		For data inputs <sup>[1]</sup>	-0.5	$V_{CC} + 0.5$	V
$V_O$	output voltage	<sup>[1]</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$I_{O(sink/source)}$	output sink or source current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C <sup>[2]</sup>	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

## 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage	2.5 V range for maximum speed performance at 30 pF output load	2.3	2.7	V
		3.3 V range for maximum speed performance at 50 pF output load	3.0	3.6	V
		for low-voltage applications	1.2	3.6	V
$V_I$	input voltage	for data inputs	0	$V_{CC}$	V
		for control inputs	0	5.5	V
$V_O$	output voltage		0	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	-	10	ns/V

## 9 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions;  $T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$ ; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 1.8 V	0.7V <sub>CC</sub>	0.9	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	GND	V
		V <sub>CC</sub> = 1.8 V	-	0.9	0.2V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.8 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> - 0.4	V <sub>CC</sub> - 0.10	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.17	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.8 V to 3.6 V	-	GND	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.8 V	-	0.09	0.30	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.20	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.40	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	-	0.23	0.60	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	per control pin; V <sub>CC</sub> = 1.8 V to 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	0.1	5	μA
		per data pin; V <sub>CC</sub> = 1.8 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 1.8 V to 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	5	μA
		V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	10	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	40	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	150	750	μA

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V	45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	150	-	μA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V	-45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	-75	-175	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 2.7 V	300	-	-	μA
		V <sub>CC</sub> = 3.0 V	450	-	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 2.7 V	-300	-	-	μA
		V <sub>CC</sub> = 3.6 V	-450	-	-	μA
C <sub>I</sub>	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**

At recommended operating conditions; T<sub>amb</sub> = -40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#)

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
t <sub>pd</sub>	propagation delay	nCP to nQn; see <a href="#">Figure 6</a> <sup>[2]</sup>					
		V <sub>CC</sub> = 1.2 V	-	10.6	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	4.5	7.5	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	4.9	ns	
		V <sub>CC</sub> = 2.7 V	1.0	2.7	4.3	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	3.7	ns	
		nMR to nQn; see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 1.2 V	-	9.9	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	4.6	7.4	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.9	5.0	ns	
		V <sub>CC</sub> = 2.7 V	1.0	3.1	4.6	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.6	4.0	ns	
t <sub>en</sub>	enable time	nOE to nQn; see <a href="#">Figure 9</a> <sup>[3]</sup>					
		V <sub>CC</sub> = 1.2 V	-	10.4	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	4.4	7.7	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	5.3	ns	
		V <sub>CC</sub> = 2.7 V	1.0	3.1	5.2	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	4.3	ns	



Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
t <sub>dis</sub>	disable time	n $\overline{OE}$ to nQn; see <a href="#">Figure 9</a> <sup>[4]</sup>				
		V <sub>CC</sub> = 1.2 V	-	6.7	-	ns
		V <sub>CC</sub> = 1.8 V	1.5	3.3	5.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	4.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.1	4.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.8	3.9	ns
t <sub>su</sub>	set-up time	nDn to nCP; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 1.8 V	1.5	0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.2	0.2	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	0.4	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	0.2	-	ns
		n $\overline{CE}$ to nCP; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 1.8 V	2.0	-0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.8	-0.2	-	ns
		V <sub>CC</sub> = 2.7 V	1.9	-0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	-0.1	-	ns
t <sub>h</sub>	hold time	nDn to nCP; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 1.8 V	0.6	-0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.8	-0.1	-	ns
		V <sub>CC</sub> = 2.7 V	0.6	-0.2	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.8	0.0	-	ns
		n $\overline{CE}$ to nCP; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 1.8 V	0.3	0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.3	0.2	-	ns
		V <sub>CC</sub> = 2.7 V	0.4	0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	0.1	-	ns
t <sub>w</sub>	pulse width	nCP HIGH or LOW; see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 1.8 V	4.0	2.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.0	1.6	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	1.6	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.5	1.4	-	ns
		nMR HIGH or LOW; see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.8 V	4.0	0.8	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.0	0.4	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	0.6	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.5	0.3	-	ns

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
t <sub>rec</sub>	recovery time	nMR to nCP; see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.8 V	0.8	0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	0.3	-	ns
		V <sub>CC</sub> = 2.7 V	0.8	0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	0.2	-	ns
f <sub>max</sub>	maximum frequency	nCP; see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 1.8 V	125	250	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	150	300	-	MHz
		V <sub>CC</sub> = 2.7 V	150	300	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	200	350	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per latch; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>				
		outputs enabled	-	16	-	pF
		outputs disabled	-	10	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C

Typical values for V<sub>CC</sub> = 2.3 V to 2.7 V are measured at V<sub>CC</sub> = 2.5 V.

Typical values for V<sub>CC</sub> = 3.0 V to 3.6 V are measured at V<sub>CC</sub> = 3.3 V.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

[4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

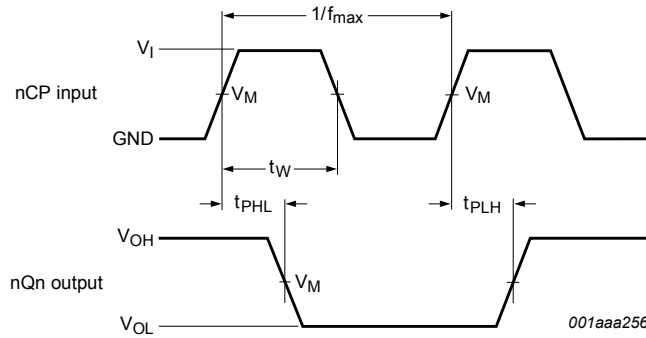
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts;

N = total load switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

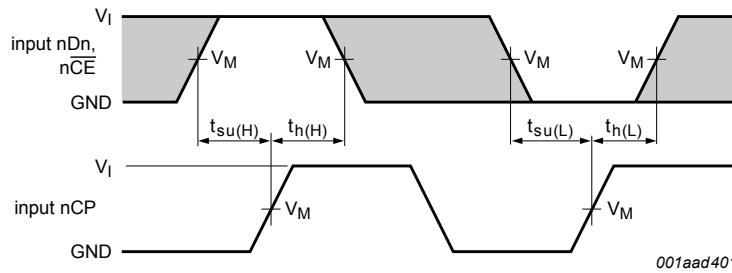
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

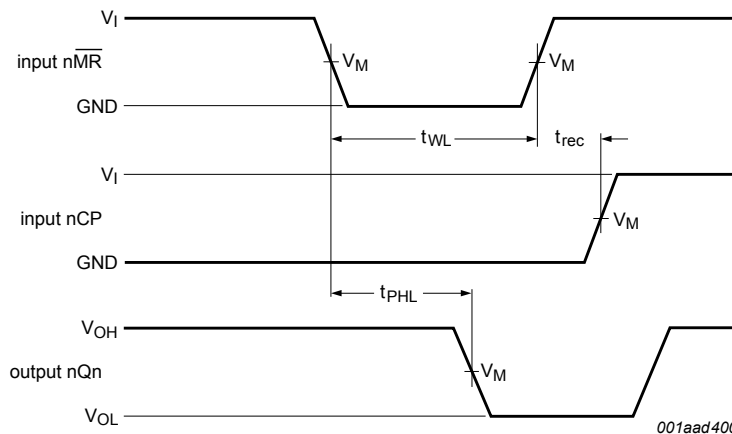
**Figure 6. Propagation delay clock input (nCP) to output (nQn), clock pulse (nCP) width and maximum clock (nCP) frequency**



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

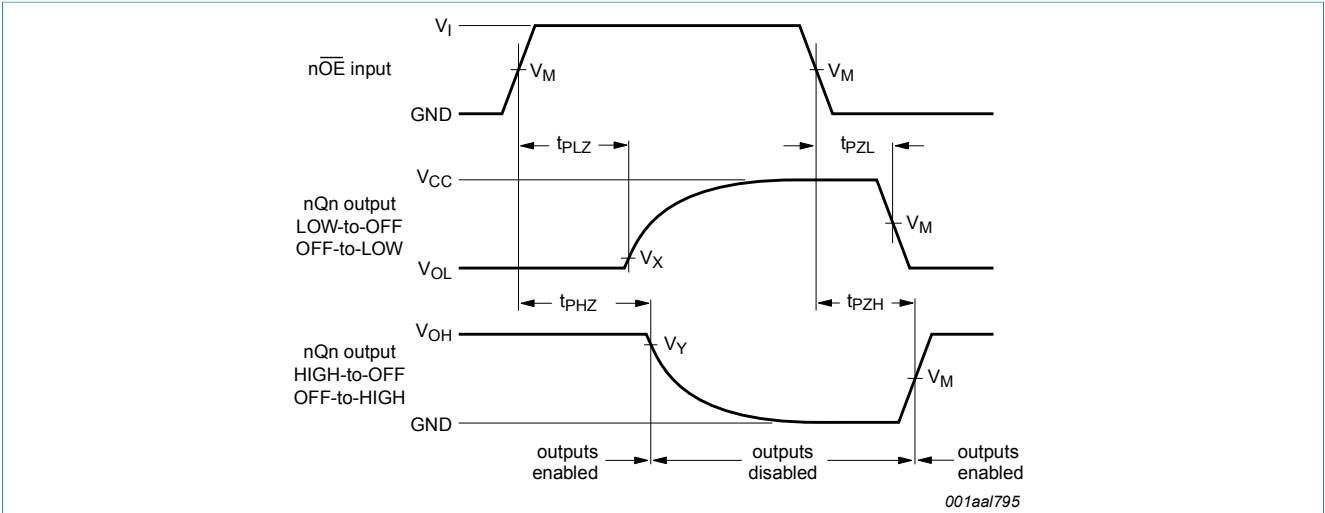
**Figure 7. Data set-up and hold times for the nDn or nCE input to the nCP input**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Figure 8. Master reset (nMR) pulse width, master reset (nMR) to output (nQn) propagation delay and master reset (nMR) to clock (nCP) recovery time**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Figure 9. OFF-state to HIGH and LOW propagation delays and LOW and HIGH to OFF-state propagation delays**

**Table 8. Measurement points**

$V_{CC}$	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$< 2.7\text{ V}$	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$\geq 2.7\text{ V}$	$2.7\text{ V}$	$1.5\text{ V}$	$1.5\text{ V}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

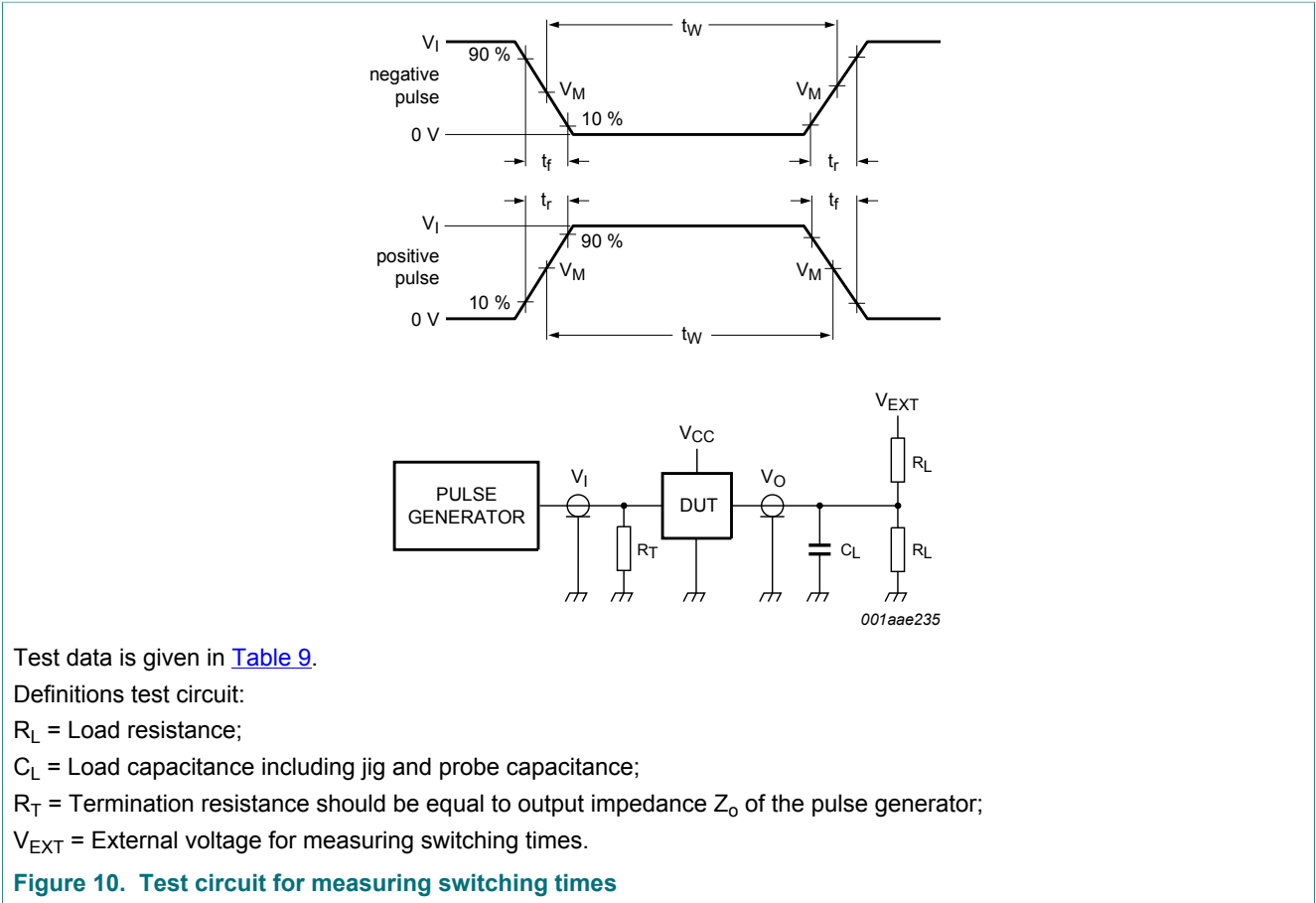


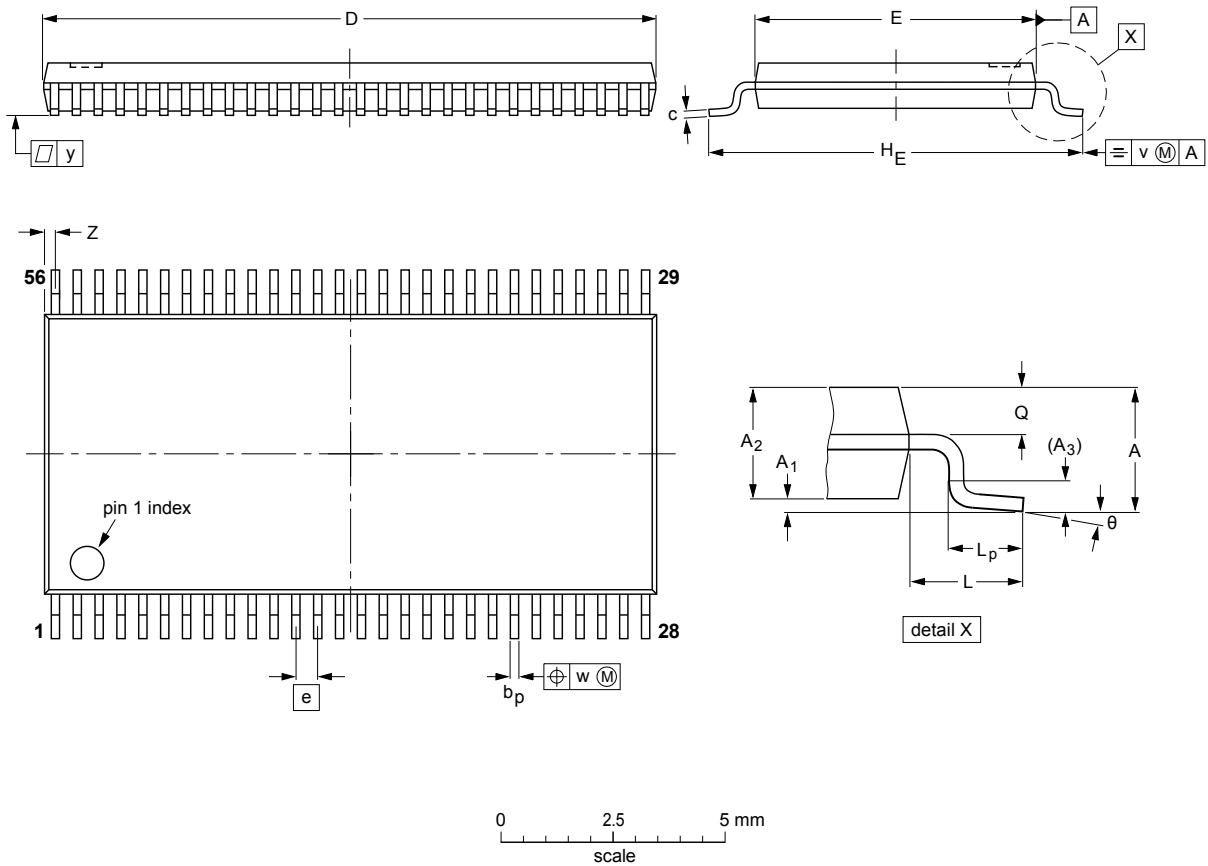
Table 9. Test data

Input			Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$R_L$	$C_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
< 2.7 V	$V_{CC}$	$\leq 2.0$ ns	500 $\Omega$	30 pF	GND	$2 \times V_{CC}$	open
$\geq 2.7$ V	2.7 V	$\leq 2.5$ ns	500 $\Omega$	50 pF	GND	$2 \times V_{CC}$	open

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT364-1		MO-153			99-12-27 03-02-19

Figure 11. Package outline SOT364-1 (TSSOP56)

## 12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16823 v.3	20180201	Product data sheet	-	74ALVCH16823 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ALVCH16823DL (SOT371-1 / SSOP56) removed</li> </ul>			
74ALVCH16823 v.2	19980729	Product specification	-	74ALVCH16823 v.1
74ALVCH16823 v.1	19980729	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 14.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia. In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

**Right to make changes** — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical

systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.



**Non-automotive qualified products** — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer

design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## Contents

---

<b>1</b>	<b>General description .....</b>	<b>1</b>
<b>2</b>	<b>Features and benefits .....</b>	<b>1</b>
<b>3</b>	<b>Ordering information .....</b>	<b>2</b>
<b>4</b>	<b>Functional diagram .....</b>	<b>2</b>
<b>5</b>	<b>Pinning information .....</b>	<b>4</b>
5.1	Pinning .....	4
5.2	Pin description .....	5
<b>6</b>	<b>Functional description .....</b>	<b>5</b>
<b>7</b>	<b>Limiting values .....</b>	<b>6</b>
<b>8</b>	<b>Recommended operating conditions .....</b>	<b>6</b>
<b>9</b>	<b>Static characteristics .....</b>	<b>7</b>
<b>10</b>	<b>Dynamic characteristics .....</b>	<b>8</b>
10.1	Waveforms and test circuit .....	11
<b>11</b>	<b>Package outline .....</b>	<b>14</b>
<b>12</b>	<b>Abbreviations .....</b>	<b>15</b>
<b>13</b>	<b>Revision history .....</b>	<b>15</b>
<b>14</b>	<b>Legal information .....</b>	<b>16</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© Nexperia B.V. 2018.

All rights reserved.

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

Date of release: 1 February 2018  
Document identifier: 74ALVCH16823