16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-stateRev. 3 — 16 August 2013Product data sheet

1. General description

The 74AVC16374 is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. The 74AVC16374 consist of 2 sections of 8 edge-triggered flip-flops. A clock input (CP) and an output enable (\overline{OE}) are provided per 8-bit section.

The 74AVC16374 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, $n\overline{OE}$ should be tied to VCC through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see Figure 5 and Figure 6).

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce

nexperia

Supports Live Insertion

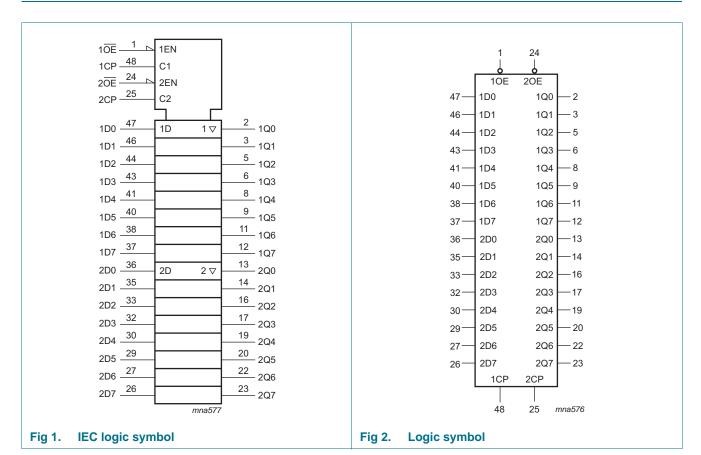
3. Ordering information

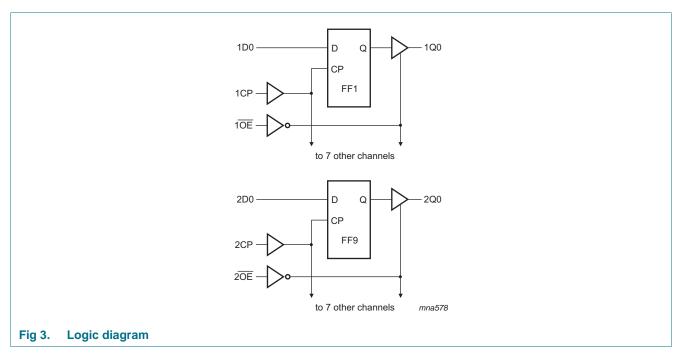
Table 1.Ordering information

| Type number | Package | | | | | | | |
|---------------|-------------------|---------|---|----------|--|--|--|--|
| | Temperature range | Name | Description | Version | | | | |
| 74AVC16374DGG | –40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 | | | | |

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

4. Functional diagram

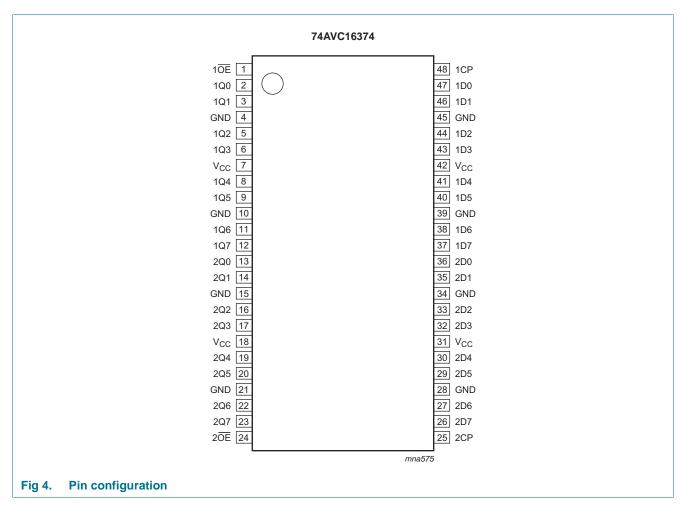




16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

5. Pinning information

5.1 Pinning



16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

5.2 Pin description

| Table 2. Pin d | escription | |
|-------------------|--------------------------------|----------------------------------|
| Symbol | Pin | Description |
| 1 <mark>OE</mark> | 1 | output enable input (active LOW) |
| 1Q0 to 1Q7 | 2, 3, 5, 6, 8, 9, 11, 12 | 3-state flip-flop outputs |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 2Q0 to 2Q7 | 13, 14, 16, 17, 19, 20, 22, 23 | 3-state flip-flop outputs |
| 2 0E | 24 | output enable input (active LOW) |
| 2CP | 25 | clock input |
| 2D0 to 2D7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input/output |
| 1D0 to 1D7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input/output |
| 1CP | 48 | clock input |

6. Functional description

Table 3. Function table^[1]

| Operating modes Inputs | | | | Internal flip-flops | Outputs |
|-----------------------------------|-----|------------|-----|---------------------|---------|
| | nOE | nCp | nDn | | nQn |
| Load and read register | L | \uparrow | I | L | L |
| | L | \uparrow | h | Н | Н |
| Load register and disable outputs | Н | \uparrow | I | L | Z |
| | Н | \uparrow | h | Н | Z |

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high-impedance OFF-state

 \uparrow = LOW-to-HIGH CP transition

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

Limiting values 7.

Limiting values Table 4.

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Parameter | Conditions | Min | Max | Unit |
|-------------------------|---|--|---|---|
| supply voltage | | -0.5 | +4.6 | V |
| input clamping current | V _I < 0 V | _ | -50 | mA |
| input voltage | | <u>[1]</u> –0.5 | +4.6 | V |
| output clamping current | V _O < 0 V | -50 | - | mA |
| output voltage | output HIGH or LOW | <u>[1]</u> –0.5 | V _{CC} + 0.5 | V |
| | output 3-state | <u>[1]</u> –0.5 | +4.6 | V |
| output current | $V_{O} = 0 V$ to V_{CC} | - | ±50 | mA |
| supply current | | - | +100 | mA |
| ground current | | -100 | - | mA |
| storage temperature | | -65 | +150 | °C |
| total power dissipation | $T_{amb} = -40 \ ^{\circ}C \ to \ +85 \ ^{\circ}C$ | [2] _ | 500 | mW |
| | supply voltage input clamping current input voltage output clamping current output voltage output voltage output current supply current ground current storage temperature | supply voltageinput clamping current $V_I < 0 V$ input voltage $V_O < 0 V$ output clamping currentoutput HIGH or LOWoutput voltageoutput 3-stateoutput current $V_O = 0 V$ to V_{CC} supply currentground currentstorage temperature $V_O = 0 V$ | -0.5input clamping current $V_1 < 0 V$ -input voltage11-0.5output clamping current $V_0 < 0 V$ -50output voltageoutput HIGH or LOW11output voltage0utput 3-state11output current $V_0 = 0 V$ to V_{CC} -supply currentground current100storage temperature-65 | supply voltage -0.5 +4.6 input clamping current $V_1 < 0 V$ - -50 input voltage 11 -0.5 +4.6 output clamping current $V_0 < 0 V$ -50 - output clamping current $V_0 < 0 V$ -50 - output voltage output HIGH or LOW 11 -0.5 $V_{CC} + 0.5$ output current $V_0 = 0 V to V_{CC}$ - +4.6 output current $V_0 = 0 V to V_{CC}$ - +50 supply current - - +100 ground current -100 - - storage temperature -65 +150 |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C, the value of Ptot derates linearly with 5.5 mW/K.

Recommended operating conditions 8.

| Table 5. | Recommended operating | conditions | | | | |
|-----------------------|--------------------------------|--|------|-----|----------|------|
| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
| V _{CC} | supply voltage | according to JEDEC Low Voltage Standards | 1.4 | - | 1.6 | V |
| | | | 1.65 | - | 1.95 | V |
| | | | 2.3 | - | 2.7 | V |
| | | | 3.0 | - | 3.6 | V |
| | | for low-voltage applications | 1.2 | - | 3.6 | V |
| VI | input voltage | | 0 | - | 3.6 | V |
| Vo | output voltage | output HIGH or LOW | 0 | - | V_{CC} | V |
| | | output 3-state | 0 | - | 3.6 | V |
| T _{amb} | ambient temperature | in free air | -40 | - | +85 | °C |
| $\Delta t / \Delta V$ | input transition rise and fall | $V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$ | 0 | - | 40 | ns/V |
| | rate | V_{CC} = 1.65 V to 2.3 V | 0 | - | 30 | ns/V |
| | | $V_{CC} = 2.3 \text{ V to } 3.0 \text{ V}$ | 0 | - | 20 | ns/V |
| | | V _{CC} = 3.0 V to 3.6 V | 0 | - | 10 | ns/V |

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

9. Static characteristics

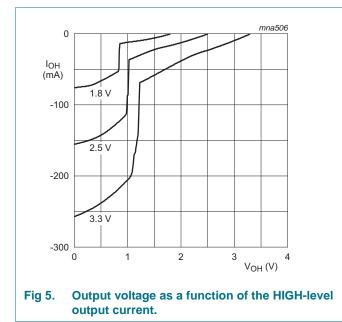
Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

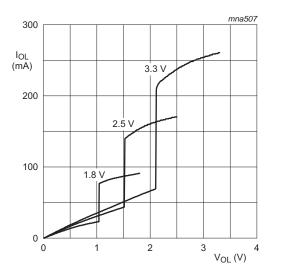
| Symbol | Parameter | Conditions | Min | Typ <mark>[1]</mark> | Max | Unit |
|----------------------|---------------------------|---|----------------------|----------------------|----------------------|------|
| T _{amb} = - | 40 °C to +85 °C | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | V _{CC} | - | - | V |
| | | $V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$ | $0.65 \times V_{CC}$ | 0.9 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | 0.9 | - | V |
| | | V_{CC} = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | 2.0 | 1.5 | - | V |
| VIL | LOW-level input voltage | V _{CC} = 1.2 V | - | - | GND | V |
| | | $V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$ | - | 0.9 | $0.35 \times V_{CC}$ | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | 0.9 | $0.35 \times V_{CC}$ | V |
| | | V_{CC} = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | - | 1.5 | 0.8 | V |
| V _{OH} | HIGH-level output voltage | $V_{I} = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | I_{O} = -100 μ A; V_{CC} = 1.65 V to 3.6 V | $V_{CC}-0.20$ | V _{CC} | - | V |
| | | $I_{O} = -3 \text{ mA}; V_{CC} = 1.4 \text{ V}$ | $V_{CC}-0.35$ | $V_{CC}-0.23$ | - | V |
| | | $I_{O} = -4$ mA; $V_{CC} = 1.65$ V | $V_{CC}-0.45$ | $V_{CC}-0.25$ | - | V |
| | | $I_{O} = -8$ mA; $V_{CC} = 2.3$ V | $V_{CC}-0.55$ | $V_{CC}-0.38$ | - | V |
| | | $I_0 = -12 \text{ mA}; V_{CC} = 3.0 \text{ V}$ | $V_{CC}-0.70$ | $V_{CC}-0.48$ | - | V |
| V _{OL} | LOW-level output voltage | $V_{I} = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | I_{O} = 100 µA; V_{CC} = 1.65 V to 3.6 V | - | GND | 0.20 | V |
| | | $I_0 = 3 \text{ mA}; V_{CC} = 1.4 \text{ V}$ | - | 0.10 | 0.35 | V |
| | | $I_0 = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$ | - | 0.10 | 0.45 | V |
| | | $I_0 = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$ | - | 0.26 | 0.55 | V |
| | | $I_0 = 12 \text{ mA}; V_{CC} = 3.0 \text{ V}$ | - | 0.36 | 0.70 | V |
| lı | input leakage current | per pin; $V_I = V_{CC}$ or GND; $V_{CC} = 1.4 \text{ V to } 3.6 \text{ V}$ | - | 0.1 | 2.5 | μA |
| I _{OFF} | power-off leakage current | $V_{1} \text{ or } V_{O} = 3.6 \text{ V}; V_{CC} = 0.0 \text{ V}$ | - | ±0.1 | ±10 | μA |
| l _{oz} | OFF-state output current | $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND | | | | |
| | | $V_{CC} = 1.4 \text{ V} \text{ to } 2.7 \text{ V}$ | - | 0.1 | 5 | μΑ |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | - | 0.1 | 10 | μA |
| I _{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ A | | | | |
| | | $V_{CC} = 1.4 \text{ V to } 2.7 \text{ V}$ | - | 0.1 | 20 | μA |
| | | V _{CC} = 3.0 V to 3.6 V | - | 0.2 | 40 | μA |
| CI | input capacitance | | - | 5 | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state



9.1 Graphs





10. Dynamic characteristics

Table 7. **Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). $t_r = t_f \le 2$ ns. For test circuit, see Figure 10.

| Symbol | Parameter | neter Conditions | | -40 | 0 °C to +85 | 5 °C | Unit |
|-----------------------------|-------------------|--|------------|-----|--------------------|------|------|
| | | | | Min | Typ ^[2] | Max | |
| t _{pd} | propagation delay | nCP to nQn; see Figure 7 | <u>[1]</u> | | | | • |
| | | $V_{CC} = 1.2 V$ | | - | 3.1 | - | ns |
| | | $V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$ | | 1.2 | 2.4 | 8.4 | ns |
| | | V_{CC} = 1.65 V to 1.95 V | | 1.0 | 2.0 | 6.7 | ns |
| | | V_{CC} = 2.3 V to 2.7 V | | 0.8 | 1.5 | 4.1 | ns |
| | | V_{CC} = 3.0 V to 3.6 V | | 0.7 | 1.3 | 3.3 | ns |
| t _{en} enable time | enable time | n <mark>OE</mark> to nQn, nBn; see <u>Figure 8</u> | <u>[1]</u> | | | | |
| | | $V_{CC} = 1.2 V$ | | - | 5.4 | - | ns |
| | | V_{CC} = 1.4 V to 1.6 V | | 1.6 | 3.9 | 8.5 | ns |
| | | V_{CC} = 1.65 V to 1.95 V | | 2.3 | 3.3 | 6.7 | ns |
| | | V_{CC} = 2.3 V to 2.7 V | | 0.9 | 2.3 | 4.3 | ns |
| | | V_{CC} = 3.0 V to 3.6 V | | 0.7 | 2.0 | 3.4 | ns |
| t _{dis} | disable time | nOE to nQn; see <u>Figure 8</u> | <u>[1]</u> | | | | |
| | | $V_{CC} = 1.2 V$ | | - | 5.6 | - | ns |
| | | $V_{CC} = 1.4 \text{ V} \text{ to } 1.6 \text{ V}$ | | 2.5 | 4.5 | 9.4 | ns |
| | | V_{CC} = 1.65 V to 1.95 V | | 1.8 | 3.3 | 7.8 | ns |
| | | V_{CC} = 2.3 V to 2.7 V | | 1.0 | 1.8 | 4.2 | ns |
| | | V_{CC} = 3.0 V to 3.6 V | | 1.2 | 2.0 | 3.9 | ns |

74AVC16374 **Product data sheet**

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | Unit |
|--------|-------------------|--|------------|------------------|--------------------|-----|------|
| | | | _ | Min | Typ ^[2] | Max | |
| w | pulse width | HIGH; nCP; see <u>Figure 7</u> | | | | | |
| | | $V_{CC} = 1.2 V$ | | - | 0.8 | - | ns |
| | | $V_{CC} = 1.4 \text{ V}$ to 1.6 V | | - | 0.5 | - | ns |
| | | V_{CC} = 1.65 V to 1.95 V | | 3.1 | 0.3 | - | ns |
| | | V_{CC} = 2.3 V to 2.7 V | | 2.5 | 0.2 | - | ns |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | | 2.5 | 0.2 | - | ns |
| su | set-up time | nDn to nCP; see Figure 8 | | | | | |
| | | $V_{CC} = 1.2 V$ | | - | -0.6 | - | ns |
| | | V_{CC} = 1.4 V to 1.6 V | | 2.7 | -0.3 | - | ns |
| | | V_{CC} = 1.65 V to 1.95 V | | 1.9 | -0.3 | - | ns |
| | | V_{CC} = 2.3 V to 2.7 V | | 1.4 | -0.2 | - | ns |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | | 1.4 | -0.1 | - | ns |
| h | hold time | nDn to nCP; see Figure 8 | | | | | |
| | | $V_{CC} = 1.2 V$ | | - | 0.8 | - | ns |
| | | V_{CC} = 1.4 V to 1.6 V | | 1.3 | 0.7 | - | ns |
| | | V_{CC} = 1.65 V to 1.95 V | | 1.2 | 0.6 | - | ns |
| | | V_{CC} = 2.3 V to 2.7 V | | 1.1 | 0.5 | - | ns |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | | 1.1 | 0.4 | - | ns |
| nax | maximum frequency | see Figure 8 | | | | | |
| | | $V_{CC} = 1.2 V$ | | - | 250 | - | MHz |
| | | V_{CC} = 1.4 V to 1.6 V | | - | 300 | - | MHz |
| | | V_{CC} = 1.65 V to 1.95 V | | 160 | 320 | - | MHz |
| | | V_{CC} = 2.3 V to 2.7 V | | 200 | 350 | - | MHz |
| | | $V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$ | | 200 | 350 | - | MHz |
| PD | power dissipation | per input; $V_I = GND$ to V_{CC} | <u>[3]</u> | | | | |
| | capacitance | outputs enabled | | - | 66 | - | pF |
| | | outputs disabled | | - | 1 | - | pF |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). $t_r = t_f \le 2$ ns. For test circuit, see Figure 10.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} \times N + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$

 f_i = input frequency in MHz; f_o = output frequency in MHz

 C_L = output load capacitance in pF

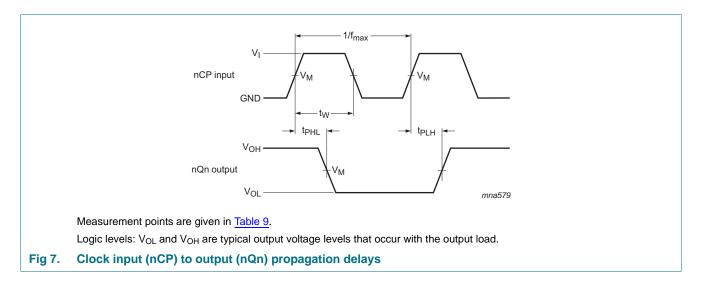
 V_{CC} = supply voltage in Volts

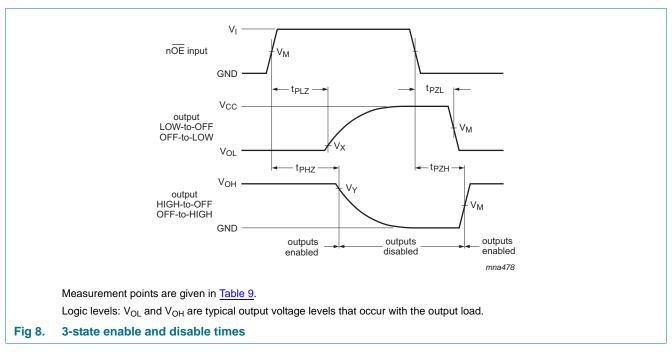
N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of the outputs.

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

11. Waveforms





16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

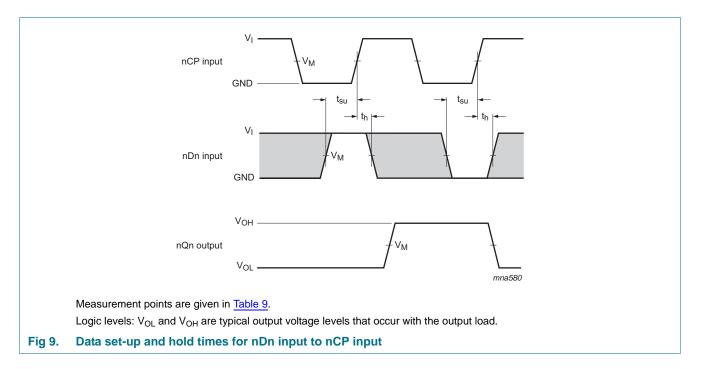


Table 8. Measurement points

| Supply voltage | V _M | Input | Input | | | | | |
|------------------|--------------------|-----------------|-------------|--------------------------|--------------------------|--|--|--|
| V _{cc} | | VI | $t_r = t_f$ | V _X | V _Y | | | |
| 1.2 V | $0.5 	imes V_{CC}$ | V _{CC} | ≤ 2 ns | V _{OL} + 0.15 V | V _{OH} – 0.15 V | | | |
| 1.4 V to 1.6 V | $0.5\times V_{CC}$ | V _{CC} | \leq 2 ns | V _{OL} + 0.15 V | V _{OH} – 0.15 V | | | |
| 1.65 V to 1.95 V | $0.5\times V_{CC}$ | V _{CC} | \leq 2 ns | V _{OL} + 0.15 V | V _{OH} – 0.15 V | | | |
| 2.3 V to 2.7 V | $0.5\times V_{CC}$ | V _{CC} | \leq 2 ns | V _{OL} + 0.15 V | V _{OH} – 0.15 V | | | |
| 3.0 V to 3.6 V | $0.5\times V_{CC}$ | V _{CC} | \leq 2 ns | V _{OL} + 0.3 V | V _{OH} – 0.3 V | | | |

Nexperia

74AVC16374

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

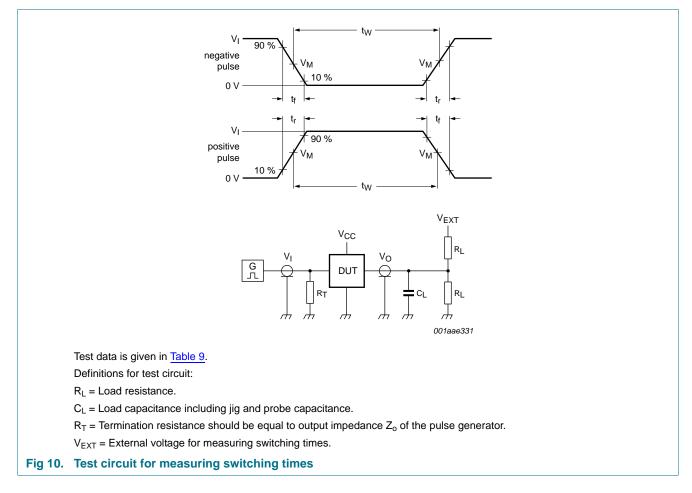


Table 9. Test data

| Supply voltage | Input | | Load | Load | | V _{EXT} | | |
|------------------|-----------------|---------------------------------|-------|-------|-------------------------------------|-------------------------------------|-------------------------------------|--|
| | VI | t _r , t _f | CL | RL | t _{PLH} , t _{PHL} | t _{PLZ} , t _{PZL} | t _{PHZ} , t _{PZH} | |
| 1.2 V | V _{CC} | \leq 2 ns | 15 pF | 2 kΩ | open | $2 \times V_{CC}$ | GND | |
| 1.4 V to 1.6 V | V _{CC} | \leq 2 ns | 15 pF | 2 kΩ | open | $2 \times V_{CC}$ | GND | |
| 1.65 V to 1.95 V | V _{CC} | \leq 2 ns | 30 pF | 1 kΩ | open | $2 \times V_{CC}$ | GND | |
| 2.3 V to 2.7 V | V _{CC} | \leq 2 ns | 30 pF | 500 Ω | open | $2\times V_{CC}$ | GND | |
| 3.0 V to 3.6 V | V _{CC} | \leq 2 ns | 30 pF | 500 Ω | open | $2\times V_{CC}$ | GND | |

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

12. Package outline

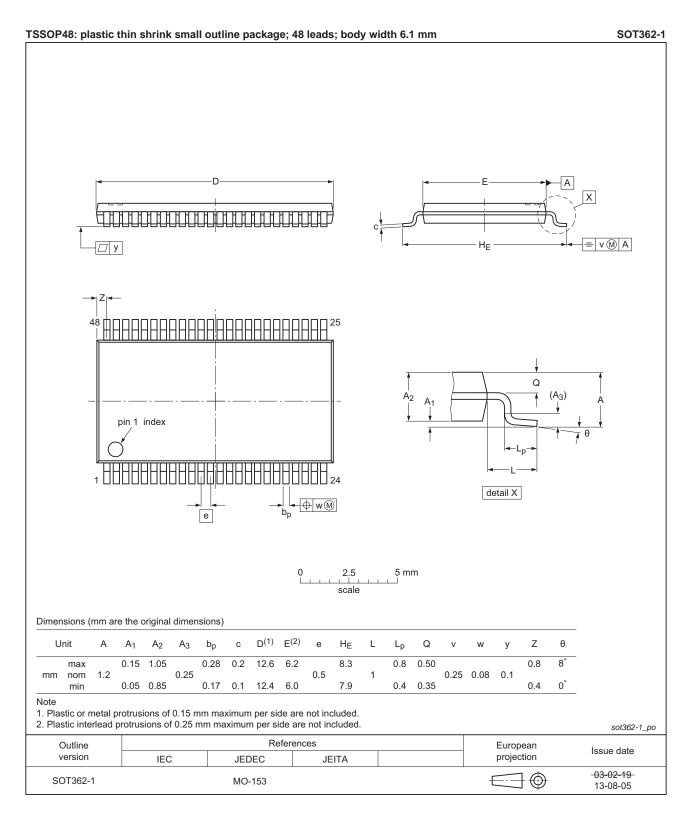


Fig 11. Package outline SOT362-1 (TSSOP48)

All information provided in this document is subject to legal disclaimers.

74AVC16374

13. Abbreviations

| Table 10. | Abbreviations | | | | | |
|-----------|---|--|--|--|--|--|
| Acronym | Description | | | | | |
| CMOS | Complementary Metal-Oxide Semiconductor | | | | | |
| DUT | Device Under Test | | | | | |
| TTL | Transistor-Transistor Logic | | | | | |

14. Revision history

Table 11.Revision history

| Document ID | Release date | Data sheet status | Change notice | Order number | Supersedes | | |
|----------------|---|--------------------------|------------------|----------------|----------------|--|--|
| 74AVC16374 v.3 | 20130816 | Product data sheet | - | - | 74AVC16374 v.2 | | |
| Modifications: | The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. | | | | | | |
| | Legal text | s have been adapted to t | he new company r | ame where appr | opriate. | | |
| 74AVC16374 v.2 | 20000309 | Product specification | - | - | 74AVC16374 v.1 | | |
| 74AVC16374 v.1 | 19981211 | Product specification | - | - | - | | |

15. Legal information

15.1 Data sheet status

| Document status[1][2] | Product status ^[3] | Definition |
|--------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any

representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and

customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia

products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Nexperia

74AVC16374

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of

non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: http://www.nexperia.com

For sales office addresses, please send an email to: salesaddresses@nexperia.com

74AVC16374

Nexperia

74AVC16374

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

17. Contents

| General description 1 |
|------------------------------------|
| Features and benefits 1 |
| Ordering information 1 |
| Functional diagram 2 |
| Pinning information 3 |
| Pinning |
| Pin description 4 |
| Functional description 4 |
| Limiting values 5 |
| Recommended operating conditions 5 |
| Static characteristics 6 |
| Graphs 7 |
| Dynamic characteristics 7 |
| Waveforms 9 |
| Package outline 12 |
| Abbreviations 13 |
| Revision history 13 |
| Legal information 14 |
| Data sheet status 14 |
| Definitions 14 |
| Disclaimers |
| Trademarks 15 |
| Contact information 15 |
| Contents 16 |
| |