National Semiconductor

MM54C915/MM74C915 7-Segment-to-BCD Converter

General Description

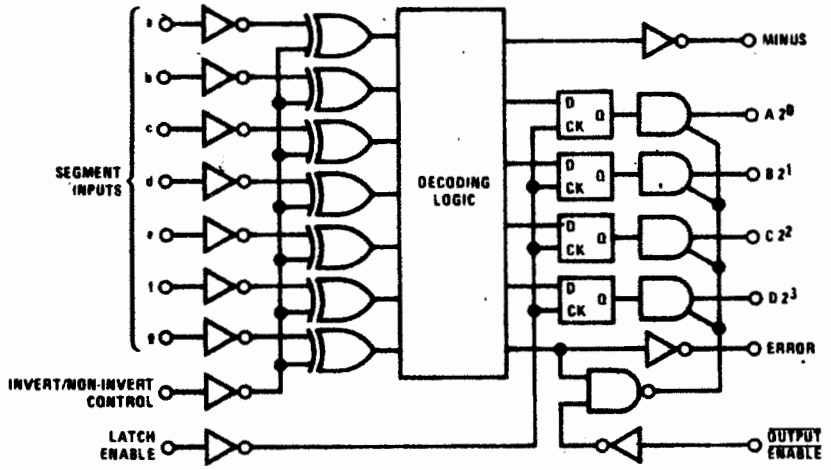
The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the **Invert/Non-invert** control pin. A logical **"0"** on the **Invert/Non-invert** control pin selects active high true decoding at the Segment inputs. A logical **"1"** on the **Invert/Non-invert** control pin selects active low true decoding at the Segment inputs. In addition to 4 **TTL** compatible BCD outputs, an Error output and Minus output are available. The **Error output** goes to an active "1" whenever a non-standard 7-segment code appears at the Segment inputs. The BCD outputs are forced into a TRI-STATE" condition when an error is detected. This allows the user to program hn own **error** code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ **500k**). The **BCD** outputs may also be **forced into** TRI-STATE by a logical "1" on output enable ($\overline{OE}$).

The Minus output goes to a logical "1" whenever a **minus** code is detected and is useful as a **microprocessor** interrupt. The BCD outputs are in a flow-though condition when Latch Enable **(LE)** is at a logical "0", and latched when LE is at a logical **"1"**. The inputs will not clamp signals to the positive supply, allowingsimple level translation from MOS to TTL.

Features

Wide supply range	3V–15V
■ High noise immunity	0.45 V_{CC} (typ.)
TTL compatible fan out	1 TTL load
Selectable active true inputs	
TRI-STATE outputs	
On-chip latch	
Error output	
Minus output	

Logic and Connection Diagrams



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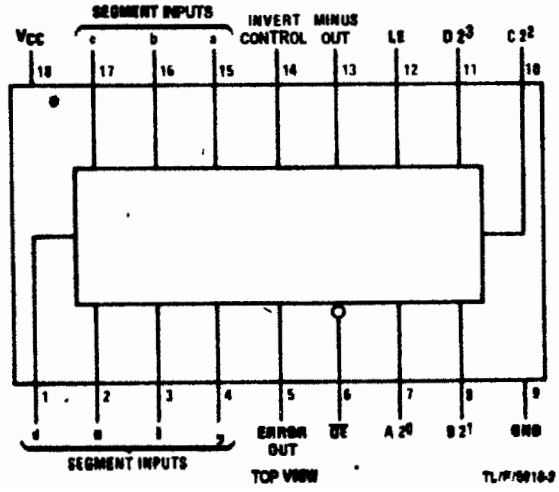
Dual-In-Line Package



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Order Number MM54C915J or MM74C915J
See NS Package J18A

Order Number MM54C915N or MM74C915N
See NS Package N18A

Absolute Maximum Ratings

Voltage at Any Output	$-0.3V$ to $V_{CC}+0.3V$	Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Voltage at Any Input	$-0.3V$ to 18V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	4.0V to 15V
MM54C915	$-55^{\circ}C$ to $+125^{\circ}C$	Maximum V_{CC}	18V
MM74C915	$-40^{\circ}C$ to $+85^{\circ}C$	Lead Temperature, (Soldering, 10 seconds)	$300^{\circ}C$

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5V$	3.5			V
		$V_{CC}=10V$	8			V
		$V_{CC}=15V$	12.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5V$			1.5	V
		$V_{CC}=10V$			2	V
		$V_{CC}=15V$			2.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN}=15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN}=0V$	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=10\mu A$				
		$V_{CC}=5V$	4.5			V
		$V_{CC}=10V$	9			V
		$V_{CC}=15V$	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=10\mu A$				
		$V_{CC}=5V$			0.5	V
		$V_{CC}=10V$			1	V
		$V_{CC}=15V$			1.5	V
I_{CC}	Supply Current	$V_{CC}=5V$		0.25	1	mA
		$V_{CC}=10V$		0.75	2.5	mA
		$V_{CC}=15V$		1.00	3	mA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C915	$V_{CC}=4.5V$	$V_{CC}-1.7$			V
	MM74C915	$V_{CC}=4.75V$	$V_{CC}-1.7$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C915	$V_{CC}=4.5V$			0.8	V
	MM74C915	$V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-360\mu A$				
	MM54C915	$V_{CC}=4.5V$	2.4			V
	MM74C915	$V_{CC}=4.75V$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA				
	MM54C915	$V_{CC}=4.5V$			0.4	V
	MM74C915	$V_{CC}=4.75V$			0.4	V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current P-Channel	$T_A=25^{\circ}C$, $V_O=0V$, (Note 2)				
		$V_{CC}=5V$	−1.75	−3.3		mA
		$V_{CC}=10V$	−8	−15		mA
		$V_{CC}=15V$	−15	−26		mA
I_{SINK}	Output Sink Current N-Channel	$T_A=25^{\circ}C$, $V_O=V_{CC}$ (Note 2)				
		$V_{CC}=5V$	5	8		mA
		$V_{CC}=10V$	20	30		mA
		$V_{CC}=15V$	30	50		mA

AC Electrical Characteristics $T_A = 25°C$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or a Logical "1"	C_L = 50 pF				
		V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_{0H}, t_{1H}	Propagation Delay Time From Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10 pF				
		V_{CC} = 5V		110	200	ns
		V_{CC} = 10V		75	130	ns
		V_{CC} = 15V		60	110	ns
t_{H0}, t_{H1}	Propagation Delay Time From High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF				
		V_{CC} = 5V		150	250	ns
		V_{CC} = 10V		80	140	ns
		V_{CC} = 15V		70	125	ns
t_s	Input Data Set-Up Time	C_L = 50 pF				
		V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_H	Input Data Hold Time	C_L = 50 pF				
		V_{CC} = 5V		−150	0	ns
		V_{CC} = 10V		−100	0	ns
		V_{CC} = 15V		−100	0	ns
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 3)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

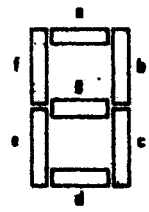
Note 3: Capacitance is guaranteed by periodic testing.

Truth Table

CHARACTER AT SEGMENT INPUTS	BCD OUTPUTS D 2^3	C 2^2	B 2^1	A 2^0	NON-BCD OUTPUTS ERROR	MINUS
0	0	0	0	0	0	0
1	0	0	0	1	0	0
I	0	0	0	1	0	0
2	0	0	1	0	0	0
3	0	0	1	1	0	0
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	0	0
9	1	0	0	1	0	0
	1	1	1	1	0	0
-	X	X	X	X	1	1
All other input combinations	X	X	X	X	1	0

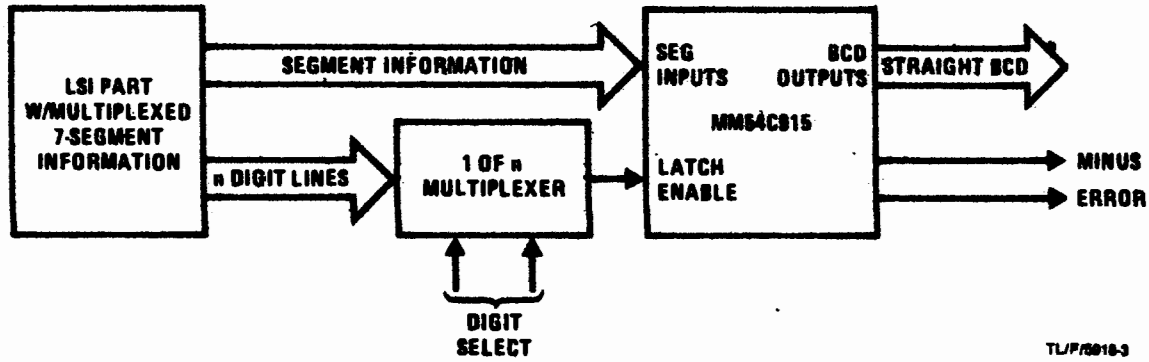
X = represents TRI-STATE condition

SEGMENT IDENTIFICATION



Typical Applications

Multiplex 7-Segment to Straight BCD



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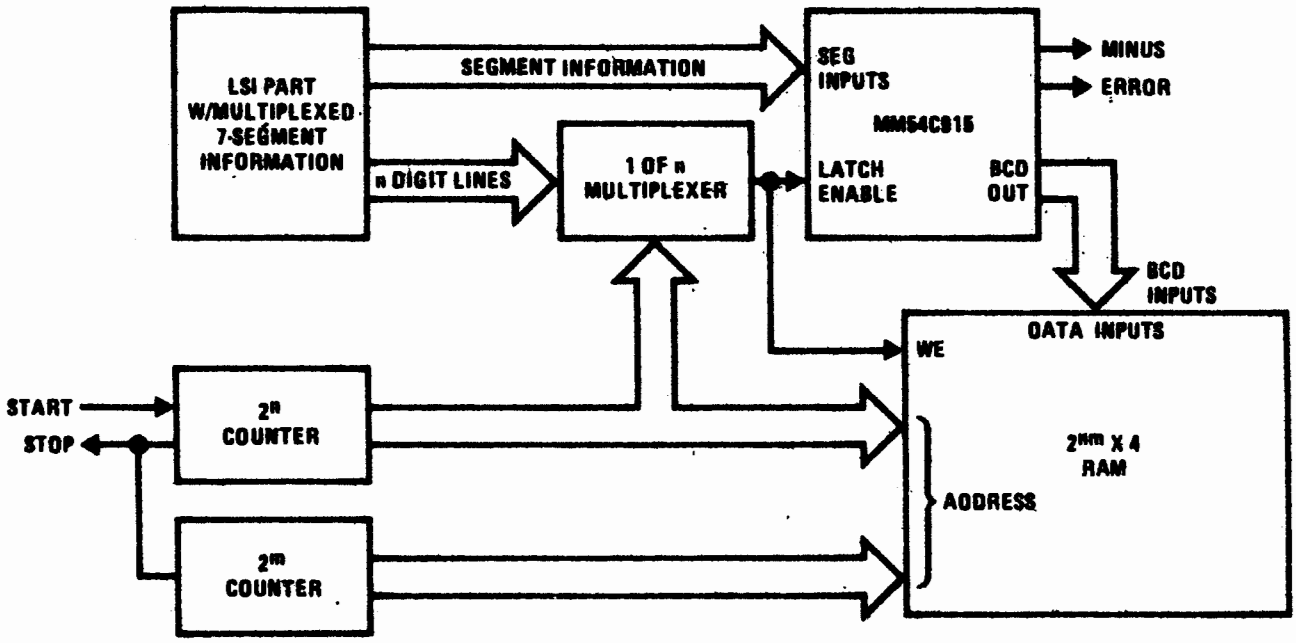
Memory Expansion from 7-Segment Outputs



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