

# DATA SHEET

## **74F195A**

4-bit parallel-access shift register

Product specification

1996 Mar 12

IC15 Data Handbook

## 4-bit parallel-access shift register

74F195A

## FEATURES

- Shift right and parallel load capability
- J –  $\bar{K}$  (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset
- Diode inputs

## DESCRIPTION

The 74F195A is a 4-Bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic Diagram and Function Table. This device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195A operates in two primary modes: shift right ( $Q_0 \rightarrow Q_1$ ) and parallel load, which are controlled by the state of the Parallel Enable ( $\bar{PE}$ ) input. Serial data enters the first flip-flop ( $Q_0$ ) via the J and  $\bar{K}$  inputs when the  $\bar{PE}$  input is High, and is shifted one bit in the direction  $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$  following each Low-to-High clock transition.

The J and  $\bar{K}$  inputs provide the flexibility of the J- $\bar{K}$  type input for special applications, and by tying the two together the simple D-type input is made for general applications.

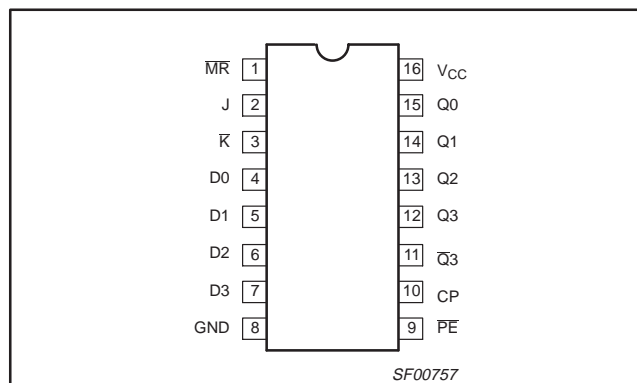
The device appears as four common clocked D flip-flops when the  $\bar{PE}$  input is Low. After the Low-to-High clock transition, data on the parallel inputs (D0–D3) is transferred to the respective  $Q_0$ – $Q_3$  outputs. Shift left operation ( $Q_3 \rightarrow Q_2$ ) can be achieved by tying the  $Q_n$  outputs to the  $D_{n-1}$  inputs and holding the  $\bar{PE}$  input Low.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F195A utilizes edge-triggering, therefore there is no restriction on the activity of the

J,  $\bar{K}$ ,  $D_n$ , and  $\bar{PE}$  inputs for logic operation, other than the set-up and hold time requirements.

A Low on the asynchronous Master Reset ( $\bar{MR}$ ) input sets all Q outputs Low, independent of any other input condition.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F195A	180MHz	40mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^\circ C$ to $+70^\circ C$	PKG. DWG. #
16-pin plastic DIP	N74F195AN	SOT 38-4
16-pin plastic SO	N74F195AD	SOT 109-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Data inputs	74F195	1.0/0.033
		74F195A	1.0/1.0
J, $\bar{K}$	J-K or D type serial inputs	74F195	1.0/0.033
		74F195A	1.0/1.0
CP	Clock Pulse input (active rising edge)	74F195	1.0/0.033
		74F195A	1.0/1.0
$\bar{MR}$	Master Reset input (active Low)	74F195	2.0/0.066
		74F195A	1.0/1.0
$Q_0$ – $Q_3$ , $\bar{Q}_3$	Data outputs	50/33	1.0mA/20mA

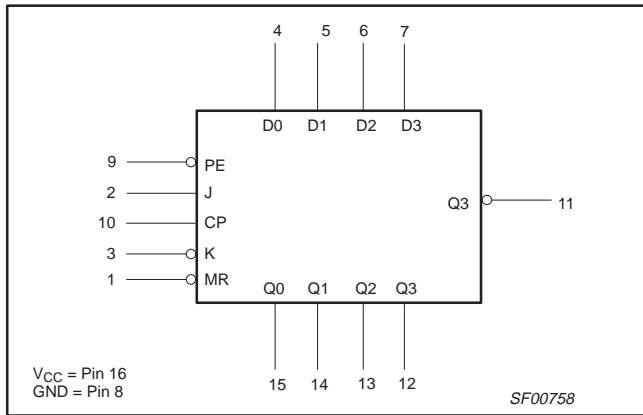
## NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

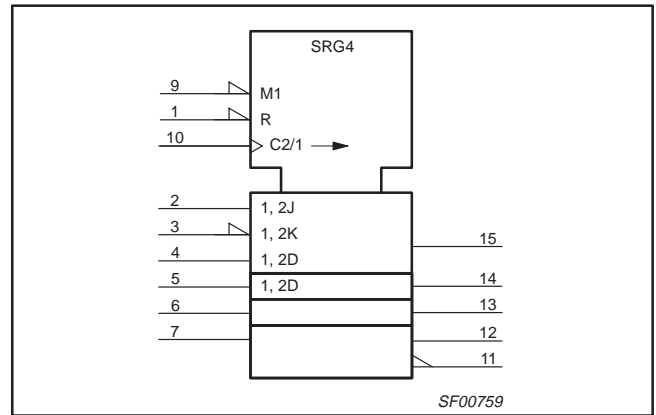
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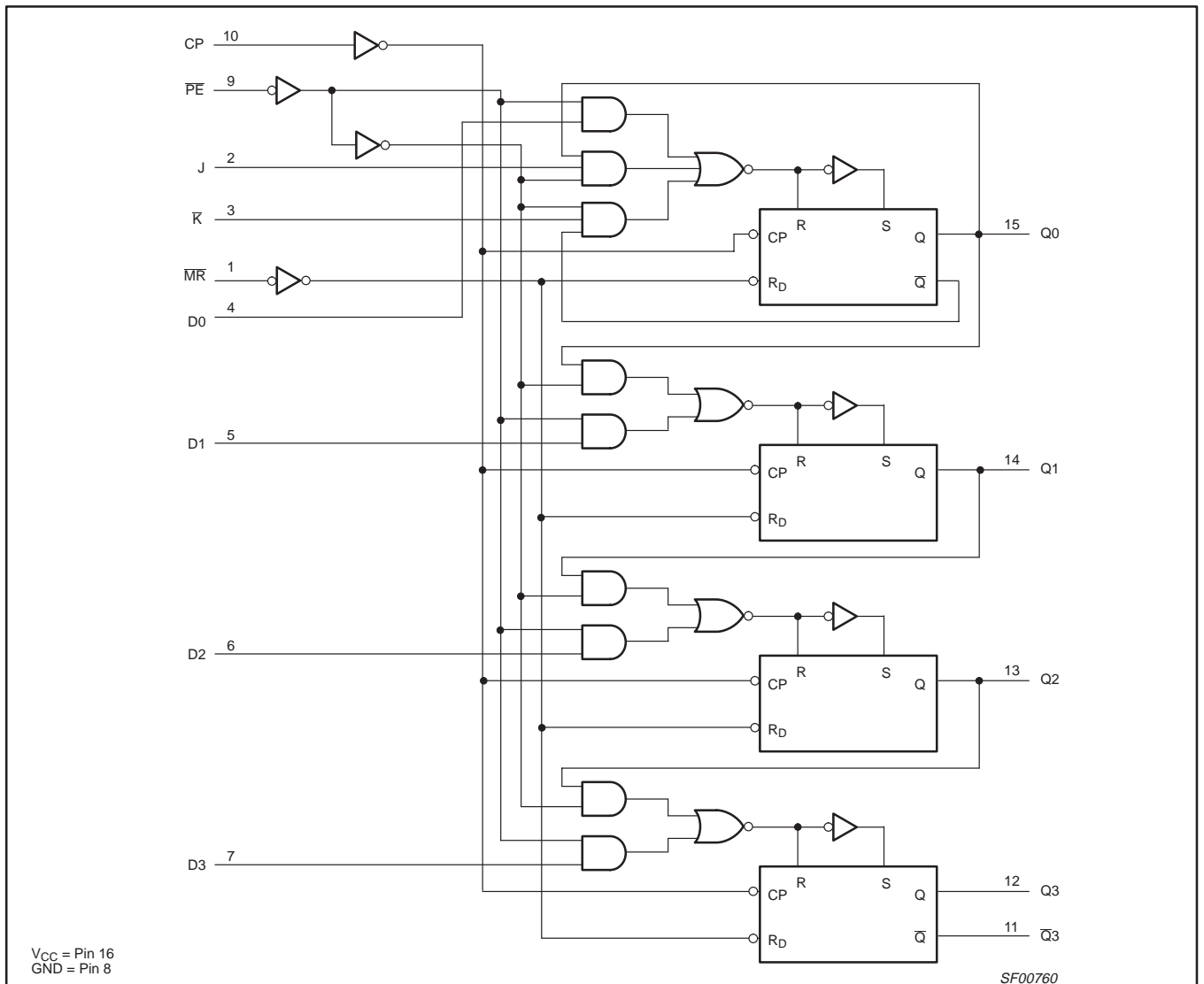
## LOGIC SYMBOL



## IEC/IEEE SYMBOL



## LOGIC DIAGRAM



## 4-bit parallel-access shift register

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## FUNCTION TABLE

INPUTS						OUTPUTS					OPERATING MODES
MR	CP	PE	J	$\bar{K}$	Dn	Q0	Q1	Q2	Q3	$\bar{Q}3$	
L	X	X	X	X	X	L	L	L	L	H	Reset (clear)
H	↑	h	h	h	X	H	q0	q1	q2	$\bar{q}2$	Shift, set First stage
H	↑	h	l	l	X	L	q0	q1	q2	$\bar{q}2$	Shift, reset First stage
H	↑	h	h	l	X	$\bar{q}0$	q0	q1	q2	$\bar{q}2$	Shift, toggle First stage
H	↑	h	l	h	X	q0	q0	q1	q2	$\bar{q}2$	Shift, retain First stage

H = High voltage level

h = High voltage level one setup time prior to Low-to-High clock transition

L = Low voltage level

l = Low voltage level one setup time prior to Low-to-High clock transition

X = Don't care

↑ = Low-to-High clock transition

dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

## 4-bit parallel-access shift register

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>	LIMITS			UNIT	
			MIN	TYP NO TAG	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
			±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.35	0.50	V
			±5%V <sub>CC</sub>		0.35	0.50	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V	74F195A			100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V	all others			20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V	74F195A			-600	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60		-150	mA
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX	74F195A		40	58	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**AC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Load mode	Waveform NO TAG	165	180		150		MHz
		Shift mode		180	190		170		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>		Waveform NO TAG	3.0 2.5	5.0 4.0	9.5 7.0	2.5 2.0	10.0 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>3</sub>		Waveform NO TAG	2.0 2.0	5.5 4.0	9.5 6.5	2.5 2.0	9.5 7.0	ns
t <sub>PHL</sub>	Propagation delay MR to Q <sub>n</sub>		Waveform 2	2.0	4.0	7.0	2.0	7.0	ns
t <sub>PLH</sub>	Propagation delay MR to Q <sub>3</sub>		Waveform 2	2.5	4.5	8.0	2.0	10.0	ns

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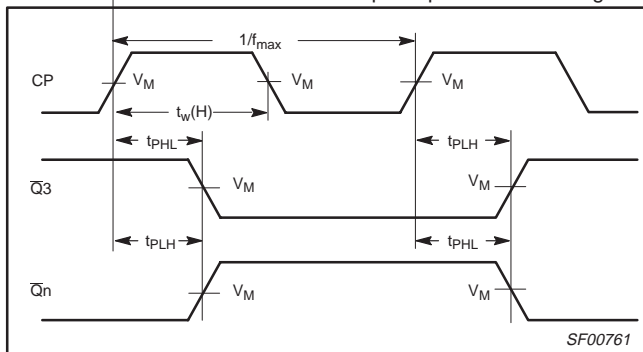
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_{S(H)}$ $t_{S(L)}$	Setup time, High or Low J, $\bar{K}$ and Dn to CP	Waveform 3	2.5 2.5			2.5 2.5		ns
$t_{H(H)}$ $t_{H(L)}$	Hold time, High or Low J, $\bar{K}$ and Dn to CP	Waveform 3	0.0 1.0			0.0 1.0		ns
$t_{S(H)}$ $t_{S(L)}$	Setup time, High or Low PE to CP	Waveform 4	2.0 2.5			2.0 2.5		ns
$t_{H(H)}$ $t_{H(L)}$	Hold time, High or Low PE to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_{W(H)}$	CP Pulse width High	Waveform NO TAG	4.5			4.5		ns
$t_{W(L)}$	MR Pulse width Low	Waveform 2	4.5			4.5		ns
$t_{REC}$	Recovery time MR to CP	Waveform 2	2.5			3.0		ns

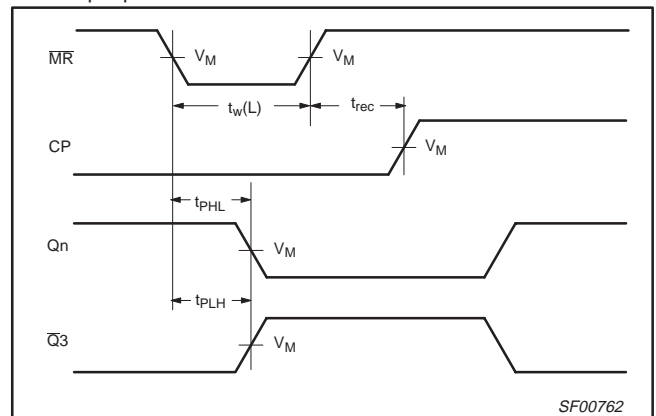
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

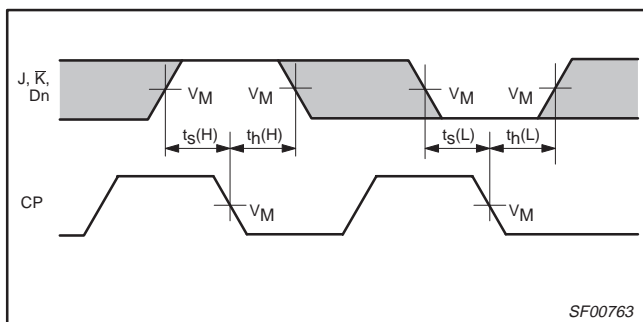
The shaded areas indicate when the input is permitted to change for predictable output performance.



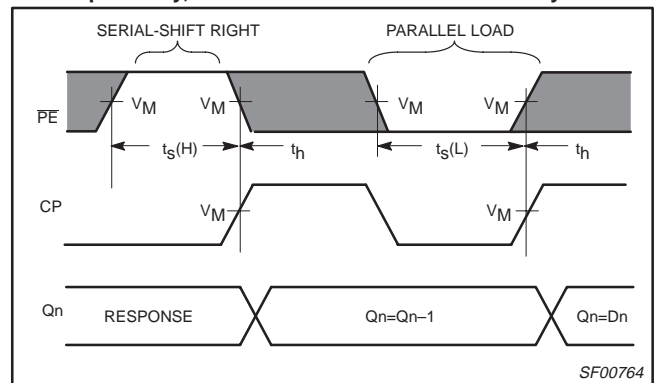
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



**Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time**



**Waveform 2. Data Setup and Hold Times**

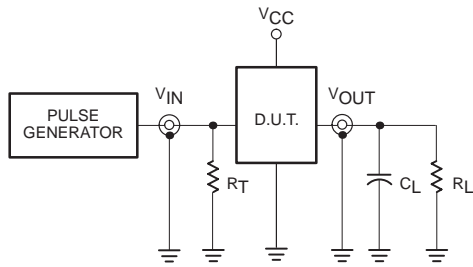


**Waveform 4. Setup and Hold Times, Parallel Enable to Clock**

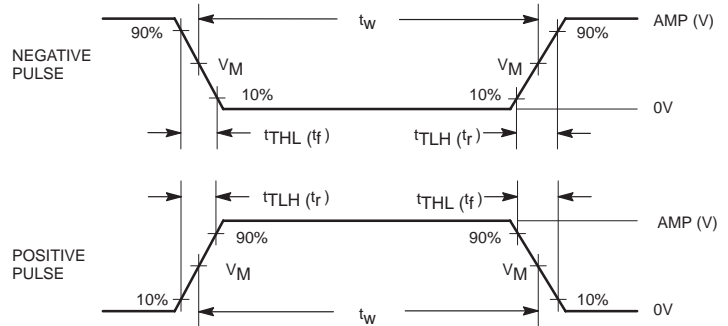
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### TEST CIRCUIT AND WAVEFORMS



**Test Circuit for Totem-Pole Outputs**



**Input Pulse Definition**

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

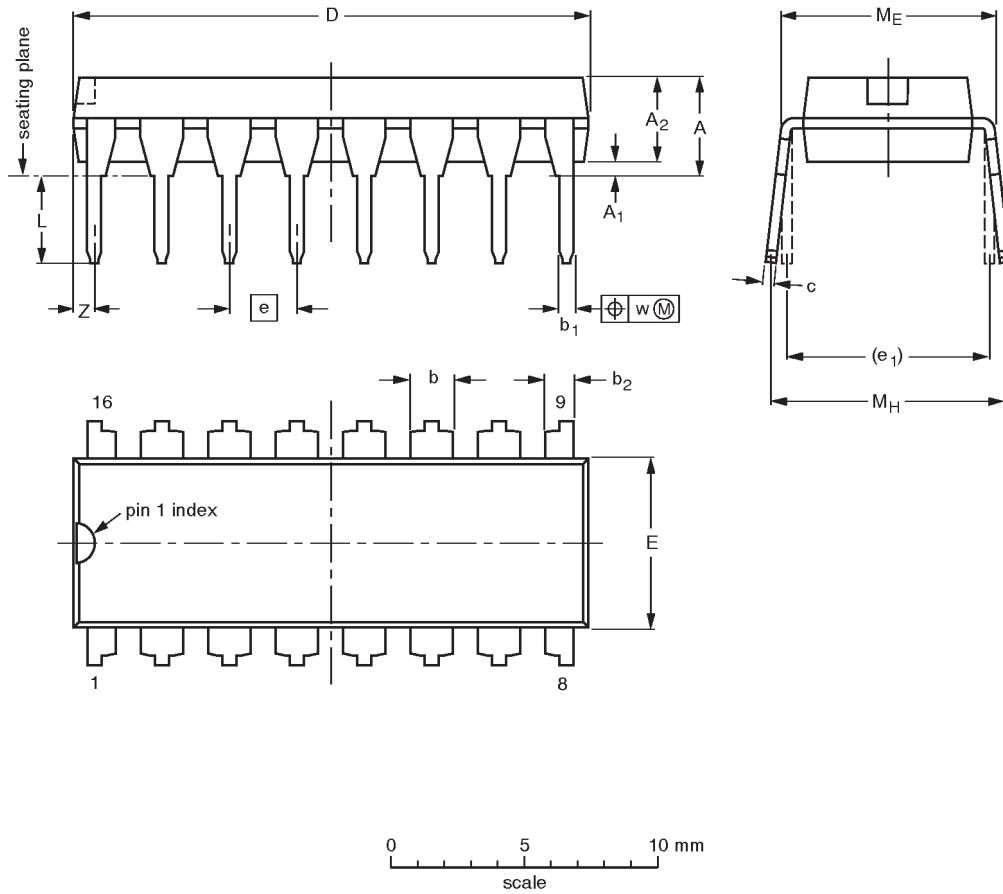
SF00006

# 4-bit parallel-access shift register

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14



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**NOTES**

## 4-bit parallel-access shift register

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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