

74F273 Octal D-Type Flip-Flop

General Description

The 74F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

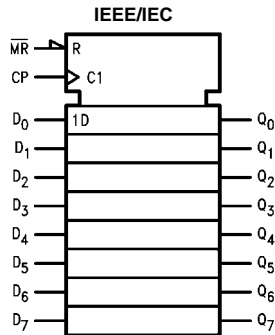
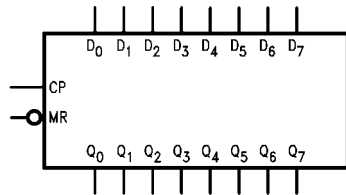
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 74F377 for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3-STATE version

Ordering Code:

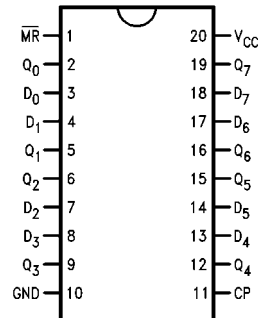
Order Number	Package Number	Package Description
74F273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

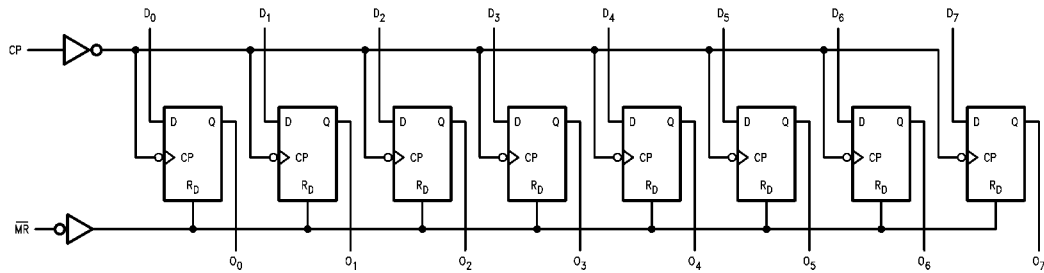
Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
D_0 – D_7	Data Inputs	1.0/1.0	$20\ \mu\text{A}/-0.6\ \text{mA}$
$\overline{\text{MR}}$	Master Reset (Active LOW)	1.0/1.0	$20\ \mu\text{A}/-0.6\ \text{mA}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	$20\ \mu\text{A}/-0.6\ \text{mA}$
Q_0 – Q_7	Data Outputs	50/33.3	$-1\ \text{mA}/20\ \text{mA}$

Mode Select-Function Table

Operating Mode	Inputs			Output
	$\overline{\text{MR}}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load "1"	H	↗	h	H
Load "0"	H	↗	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
↗ = LOW-to-HIGH clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (min)	4000V


Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

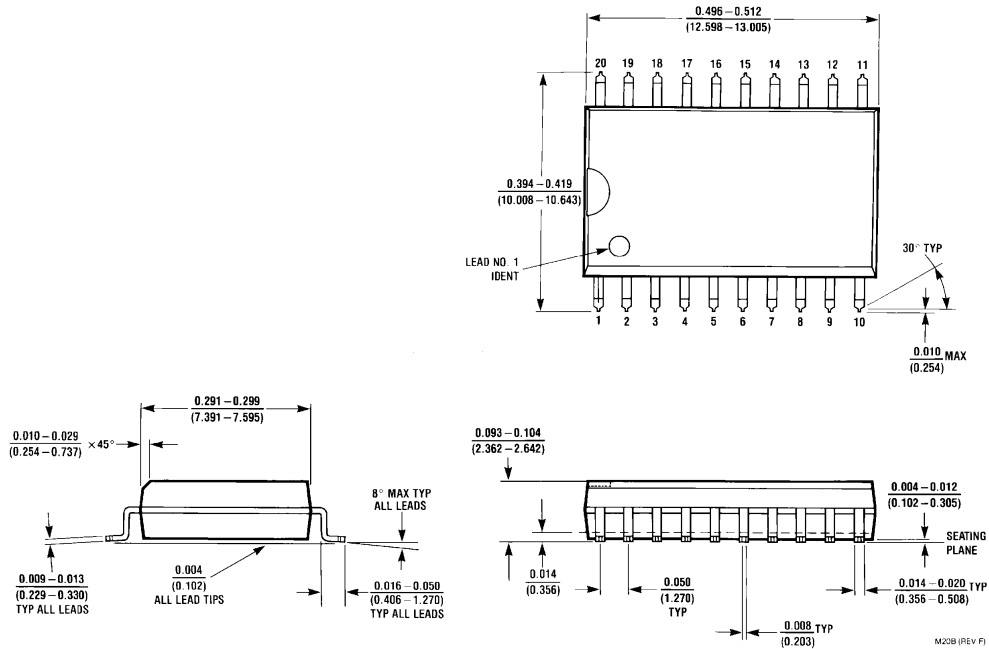
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

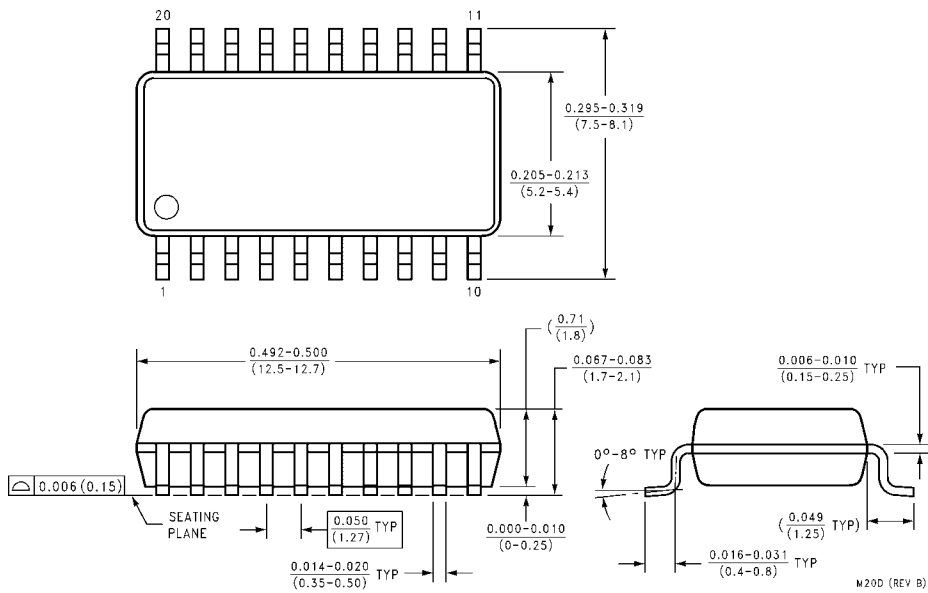
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}			V	Min	I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC} 5% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All other pins grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All other pins grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current			44	mA	Max	CP = 
I _{CCL}				56	mA	Max	D _n = $\overline{\text{MR}}$ = HIGH

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	160			95		130		MHz
t_{PLH}	Propagation Delay	3.0		7.0	2.5	9.5	2.5	7.5	ns
t_{PHL}	Clock to Output	4.0		9.00	3.0	11.0	3.5	9.0	
t_{PLH}	Propagation Delay	4.5		9.5	3.0	11.0	4.0	10.0	ns
t_{PHL}	$\overline{\text{MR}}$ to Output								
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns	
$t_S(L)$	Data to CP	3.5		4.0		3.5			
$t_H(H)$	Hold Time, HIGH or LOW	0.5		1.0		0.5		ns	
$t_H(L)$	Data to CP	1.0		1.0		1.0			
$t_W(L)$	$\overline{\text{MR}}$ Pulse Width, LOW	6.0		4.0		6.0		ns	
$t_W(H)$	CP Pulse Width	6.0		5.0		6.0		ns	
$t_W(L)$	HIGH or LOW	6.0		5.0		6.0			
t_{REC}	Recovery Time, $\overline{\text{MR}}$ to CP	3.0		4.5		3.5		ns	

Physical Dimensions inches (millimeters) unless otherwise noted

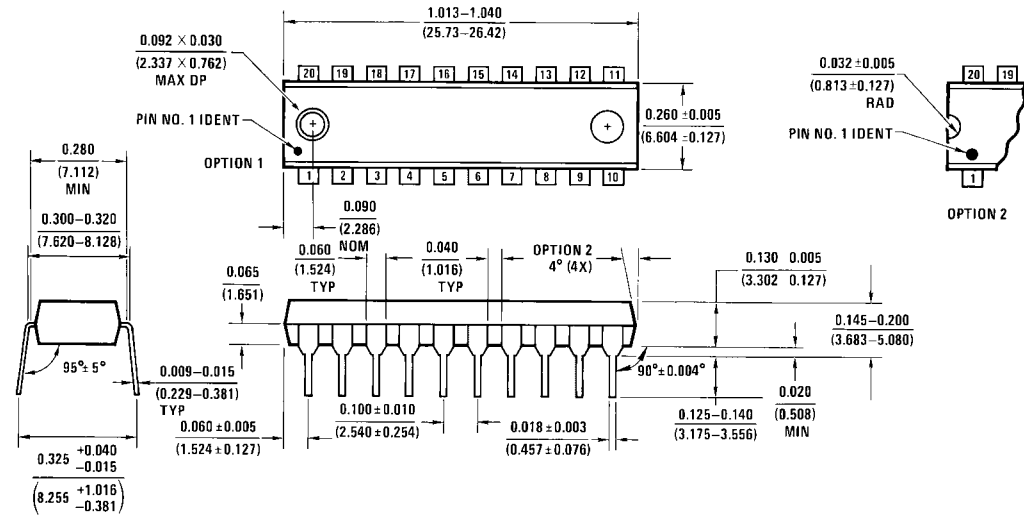


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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