

# DATA SHEET

**74F382**

Arithmetic Logic Unit

Product specification

1990 Jul 12

IC15 Data Handbook

# Arithmetic logic unit

# 74F382

## FEATURES

- Performs six arithmetic and logic functions
- Selectable Low (clear) and High (preset) functions
- Low-input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for Two's Complement arithmetic

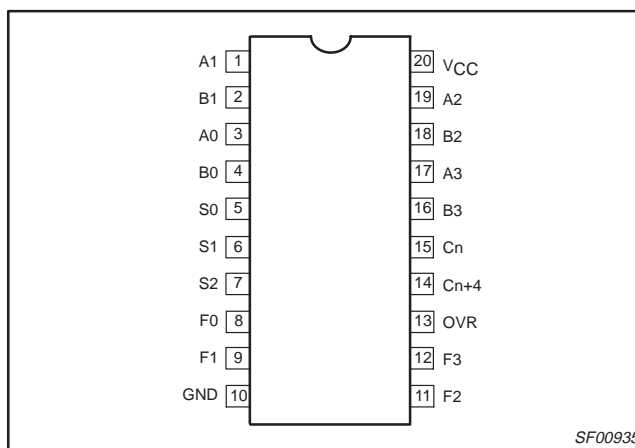
## DESCRIPTION

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select (S0–S2) input codes force the Function outputs Low or High. An overflow output is provided for convenience in Two's Complement arithmetic.

A carry output is provided for ripple expansion. For high-speed expansion using a carry look-ahead generator, refer to the 74F381 data sheet.

Signals applied to the Select inputs, S0–S2, determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the subtract operating modes, it is necessary to force a carry (High for active-High operands, Low for active-Low operands) into the Cn input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of Cn+3 and Cn+4; a High signal on OVR indicates overflow in Two's complement operation (See Table 2 for Two's complement arithmetic). Typical delays for Figure 1 are given in Table 1. When the 74F382 is cascaded to handle word lengths longer than 4 bits, only the most significant overflow (OVR) output is used.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0ns	54mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
20-pin plastic DIP	N74F382N	SOT146-1
20-pin plastic SO	N74F382D	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A3	A operand inputs	1.0/4.0	20 $\mu$ A/2.4mA
B0 – B3	B operand inputs	1.0/4.0	20 $\mu$ A/2.4mA
S0 – S2	Function select inputs	1.0/1.0	20 $\mu$ A/0.6mA
Cn	Carry input	1.0/5.0	20 $\mu$ A/3.0mA
Cn+4	Carry output	50/33	1.0mA/20mA
OVR	Overflow output	50/33	1.0mA/20mA
F0–F3	Outputs	50/33	1.0mA/20mA

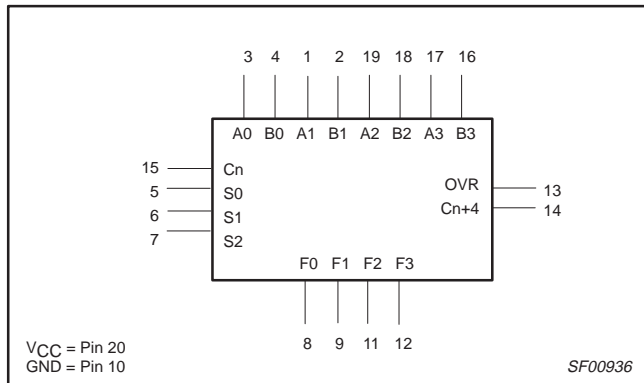
### NOTE:

One (1.0) FAST unit load is defined as 20 $\mu$ A in the High state and 0.6mA in the Low state.

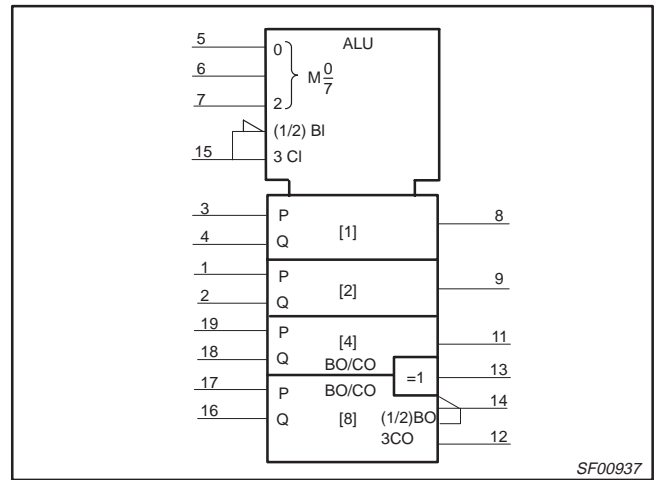
# Arithmetic logic unit

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## LOGIC SYMBOL



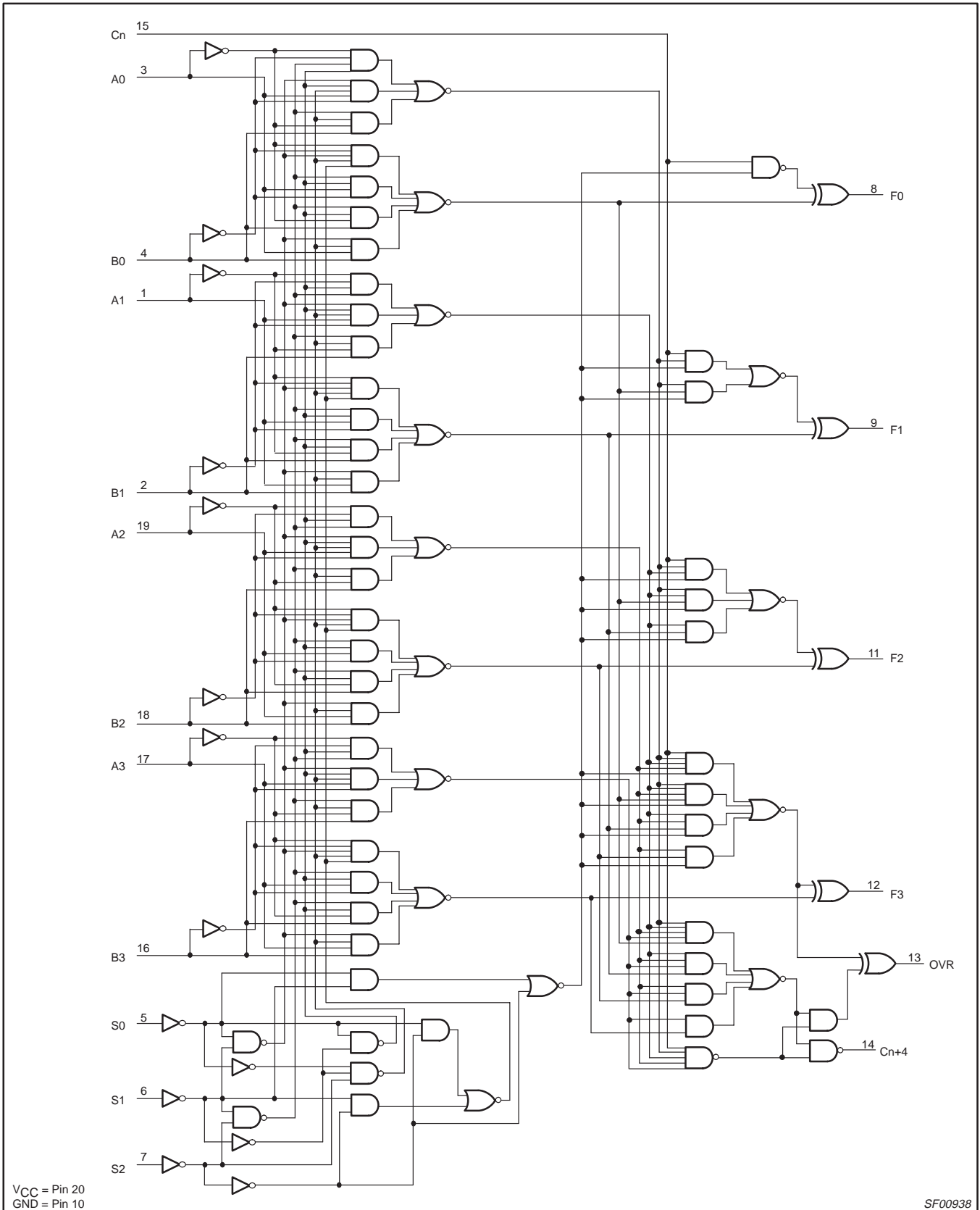
## IEC/IEEE SYMBOL



# Arithmetic logic unit

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## LOGIC DIAGRAM



SF00938

# Arithmetic logic unit

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## FUNCTION TABLE

INPUTS						OUTPUTS						OPERANDS	OPERATING MODE
S0	S1	S2	Cn	An	Bn	F0	F1	F2	F3	OVR	Cn+4		
L	L	L	L	X	X	L	L	L	L	H	H		Clear
L	L	L	H	X	X	L	L	L	L	H	H		
H	L	L	L	L	L	H	H	H	H	L	L	Active-Low	B minus A
H	L	L	L	L	H	L	H	H	H	L	H		
H	L	L	L	H	L	L	L	L	L	L	L		
H	L	L	L	H	H	H	H	H	H	L	L		
H	L	L	H	L	L	L	L	L	L	L	H	Active-High	
H	L	L	H	L	H	H	H	H	H	L	H		
H	L	L	H	H	L	H	L	L	L	L	L		
H	L	L	H	H	H	L	L	L	L	L	H		
L	H	L	L	L	L	H	H	H	H	L	L	Active-Low	A minus B
L	H	L	L	L	H	L	L	L	L	L	L		
L	H	L	L	H	L	L	H	H	H	L	H		
L	H	L	L	H	H	H	H	H	H	L	L		
L	H	L	H	L	L	L	L	L	L	L	H	Active-High	
L	H	L	H	L	H	H	L	L	L	L	L		
L	H	L	H	H	L	H	H	H	H	L	H		
L	H	L	H	H	H	L	L	L	L	L	H		
H	H	L	L	L	L	L	L	L	L	L	L	A Plus B	
H	H	L	L	L	H	H	H	H	H	L	L		
H	H	L	L	H	L	H	H	H	H	L	L		
H	H	L	L	H	L	L	L	L	L	L	H		
H	H	L	L	H	L	L	L	L	L	L	H		
H	H	L	L	H	H	H	H	H	H	L	H		
H	H	L	L	H	H	L	L	L	L	L	H		
H	H	L	L	H	H	H	H	H	H	L	H		
L	L	H	X	L	L	L	L	L	L	L	L	A ⊕ B	
L	L	H	X	L	H	H	H	H	H	L	L		
L	L	H	L	H	L	H	H	H	H	L	L		
L	L	H	X	H	H	L	L	L	L	H	H		
L	L	H	H	H	L	H	H	H	H	H	H		
H	L	H	X	L	L	L	L	L	L	L	L	A + B	
H	L	H	X	L	H	H	H	H	H	L	L		
H	L	H	X	H	L	H	H	H	H	L	L		
H	L	H	L	H	H	H	H	H	H	L	L		
H	L	H	H	H	H	H	H	H	H	H	H		
L	H	H	X	L	L	L	L	L	L	H	H	AB	
L	H	H	X	L	H	L	L	L	L	L	L		
L	H	H	X	H	L	L	L	L	L	H	H		
L	H	H	L	H	H	H	H	H	H	L	L		
L	H	H	H	H	H	H	H	H	H	H	H		
H	H	H	X	L	L	H	H	H	H	L	L	Preset	
H	H	H	X	L	H	H	H	H	H	L	L		
H	H	H	X	H	L	H	H	H	H	L	L		
H	H	H	L	H	H	H	H	H	H	L	L		
H	H	H	H	H	H	H	H	H	H	H	H		

H = High voltage level  
 L = Low voltage level  
 X = Don't care

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## FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S0	S1	S2	
L	L	L	Clear
H	L	L	B minus A
L	H	L	A minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level  
L = Low voltage level

**Table 1. 16-Bit Delay Tabulation**

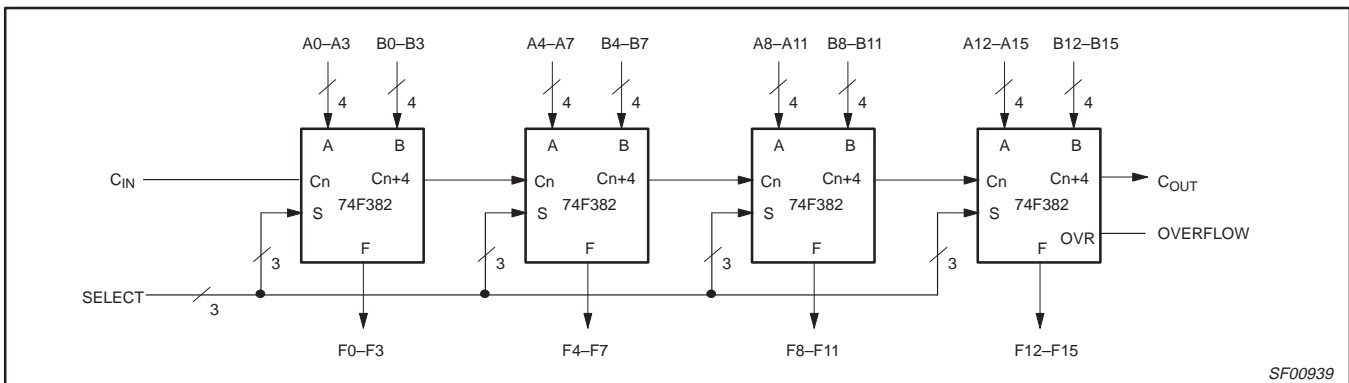
PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
Ai or Bi to Cn+4	6.5ns	6.5ns
Cn to Cn+4	6.3ns	6.3ns
Cn to Cn+4	6.3ns	6.3ns
Cn to F	8.1ns	—
Cn to Cn+4, OVR	—	8.0ns
Total Delay	27.2ns	27.1ns

**Table 2. Two's Complement Arithmetic**

MSB			LSB	Numerical Values
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	-8
H	L	L	H	-7
H	L	H	L	-6
H	L	H	H	-5
H	H	L	L	-4
H	H	L	H	-3
H	H	H	L	-2
H	H	H	H	-1

H = High voltage level  
L = Low voltage level

## APPLICATION



**Figure 1. 16-bit Look-ahead Carry ALU Expansion**

## Arithmetic logic unit

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +1	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER SYMBOL	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX,	±10%V <sub>CC</sub>	2.5		V	
		V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX,	±10%V <sub>CC</sub>		0.30	0.50	V
		V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	C <sub>n</sub>			-3.0	mA	
		A0-A3, B0-B3	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-2.4	mA
		S0, S1, S2				-0.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60		-150	mA
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX			54	81	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

# Arithmetic logic unit

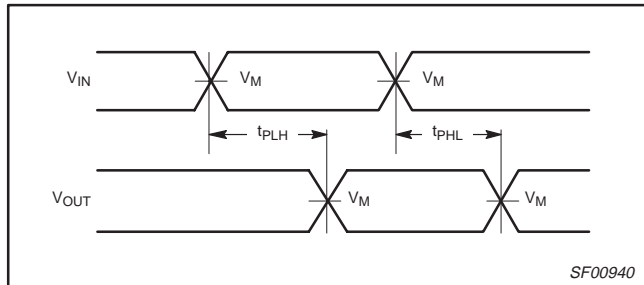
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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay C <sub>n</sub> to F <sub>n</sub>	Waveform 1	3.0 2.5	7.0 4.5	12.0 6.5	2.5 2.5	13.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> or B <sub>n</sub> to F <sub>n</sub>	Waveform 1	3.5 3.0	8.0 6.0	13.5 10.0	3.5 2.5	17.0 11.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>i</sub> to F <sub>i</sub>	Waveform 1	5.5 5.5	9.0 7.5	15.0 10.5	5.5 5.5	16.0 12.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>i</sub> to B <sub>i</sub> to C <sub>n+4</sub>	Waveform 1	3.5 3.5	7.0 6.5	10.5 9.5	3.5 3.5	11.5 10.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>i</sub> to OVR or C <sub>n+4</sub>	Waveform 1	7.0 5.0	10.5 8.0	14.5 11.0	6.5 5.0	17.0 12.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay C <sub>n</sub> to C <sub>n+4</sub>	Waveform 1	3.0 3.5	4.5 5.0	6.0 6.5	2.5 3.5	6.5 7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay C <sub>n</sub> to OVR	Waveform 1	4.5 3.0	9.0 5.0	13.5 6.5	4.0 3.0	15.0 7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>i</sub> or B <sub>i</sub> to OVR	Waveform 1	6.0 3.5	9.0 6.5	12.5 9.0	5.5 3.5	16.5 10.0	ns

## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.



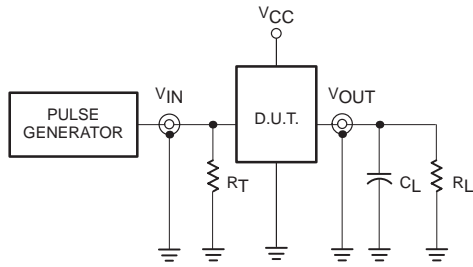
Waveform 1. Propagation Delay for Non-Inverting or Inverting paths



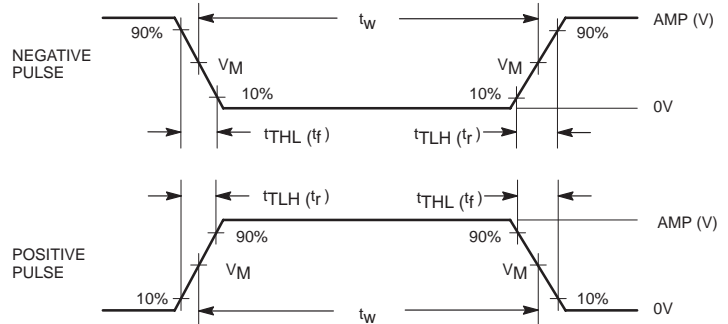
# Arithmetic logic unit

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## TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

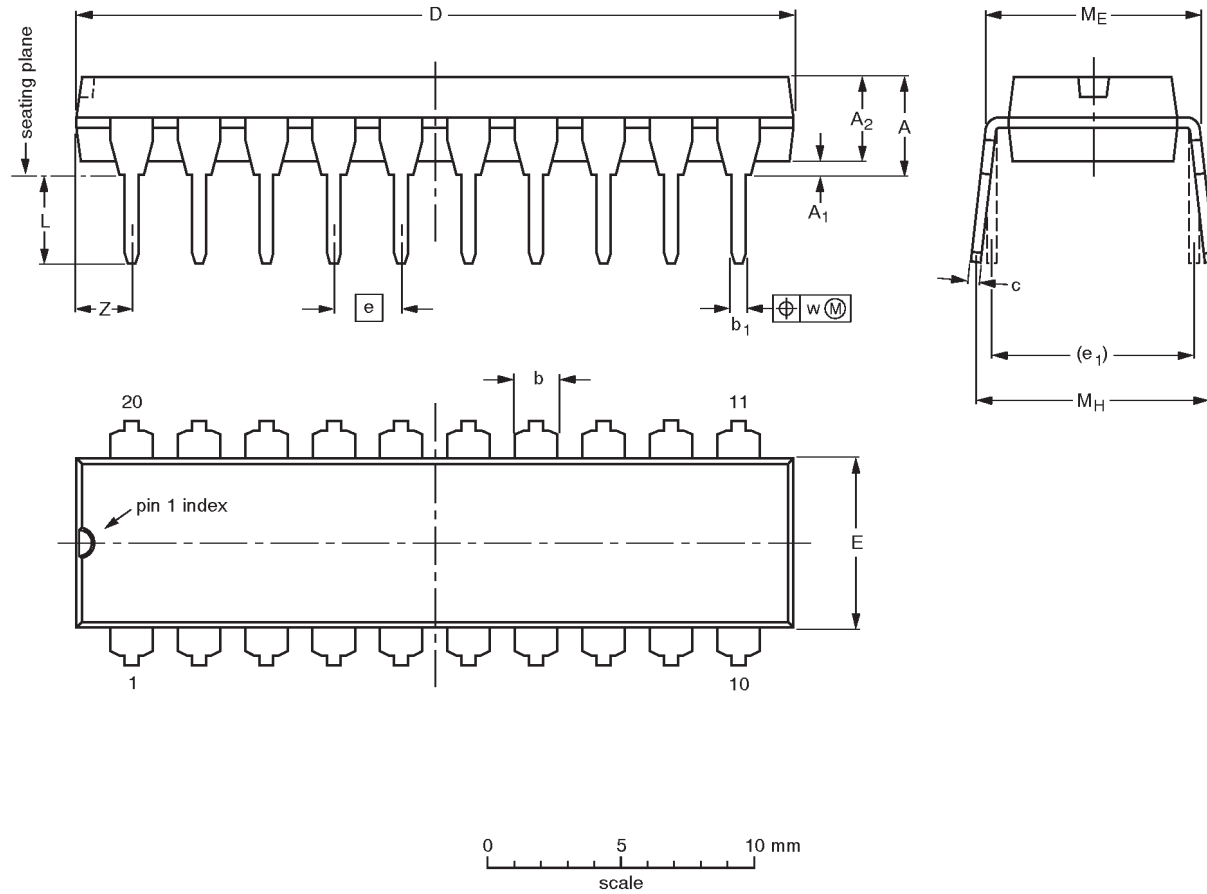
SF00006

# Arithmetic Logic Unit

# 74F382

**DIP20: plastic dual in-line package; 20 leads (300 mil)**

**SOT146-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

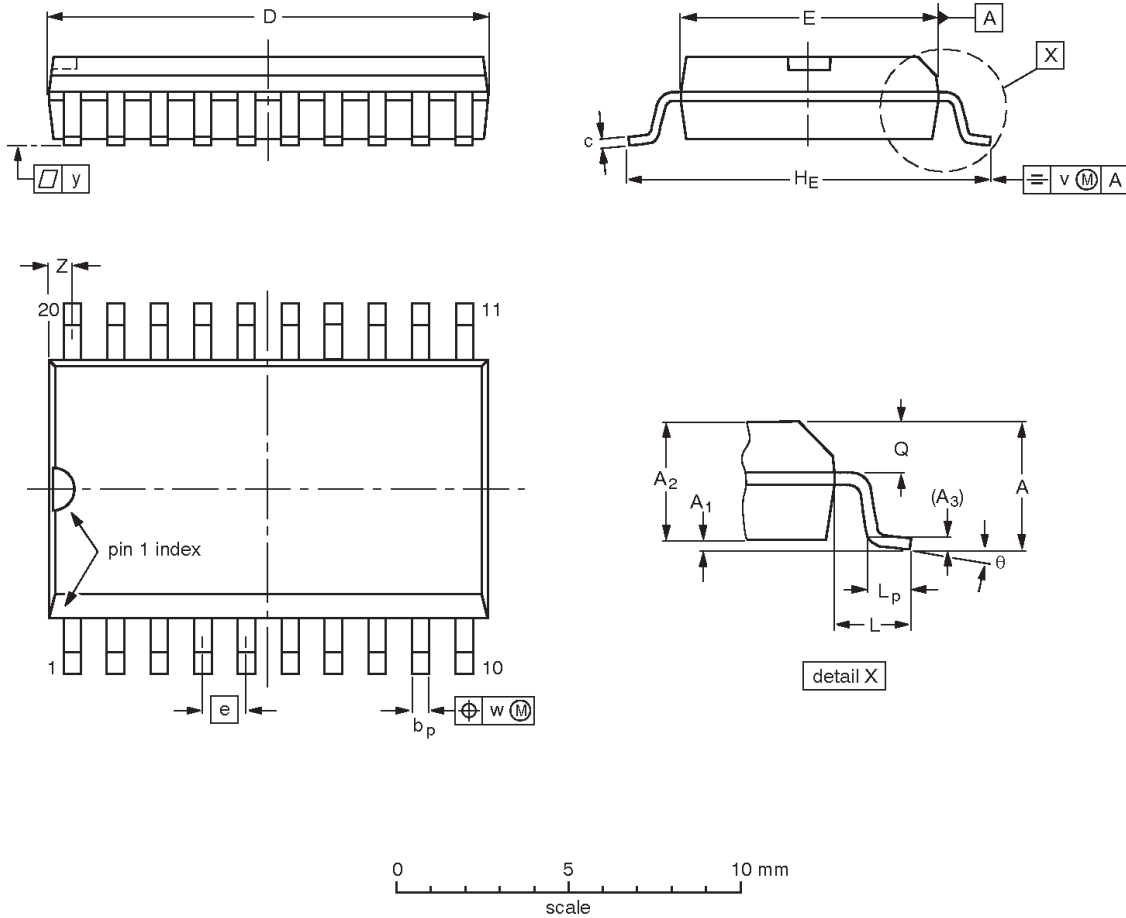
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Arithmetic Logic Unit

# 74F382

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

## Arithmetic Logic Unit

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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