

# DATA SHEET

**74F3893**

Quad futurebus backplane transceiver

Product specification

1991 Jan 18

IC15 Data Handbook

# Quad Futurebus backplane transceiver

## 74F3893

### FEATURES

- Quad backplane transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- Futurebus drivers sink 100mA
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 and IEEE 1194.1 Futurebus Standards
- Built-in precision band-gap (BG) reference provides accurate receiver thresholds and improved noise immunity
- Glitch-free power up/power down operation on all outputs
- Pin and function compatible with NSC DS3893

### DESCRIPTION

The 74F3893 is a quad backplane transceivers and is intended to be used in very high speed bus systems.

The 74F3893 interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 5pF).

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is

much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F3893 has four TTL outputs ( $R_n$ ) on the receiver side with a common receiver enable input ( $\overline{RE}$ ). It has four data inputs ( $D_n$ ) which are also TTL. These data inputs are NANDed with the data enable input (DE). The four I/O pins (bus side) are futurebus compatible, sink a minimum of 100mA, and are designed to drive heavily loaded backplanes with load impedances as low as 10 ohms. All outputs are designed to be glitch-free during power up and down.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT( TOTAL)
74F3893	3.0ns	55mA

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	
20-pin PLCC	N74F3893A	SOT380-1

### INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/0.067	20 $\mu$ A/40 $\mu$ A
DE	Data enable input	1.0/0.33	20 $\mu$ A/200 $\mu$ A
$\overline{RE}$	Receiver enable input	1.0/0.067	20 $\mu$ A/40 $\mu$ A
I/O0 – I/O3	Bus inputs	5.0/0.033	100 $\mu$ A/20 $\mu$ A
I/O0 – I/O3	Bus outputs	OC/166.7	OC/100mA
R0 – R7	Receiver outputs	150/40	3mA/24mA

#### Notes to input and output loading and fan out table

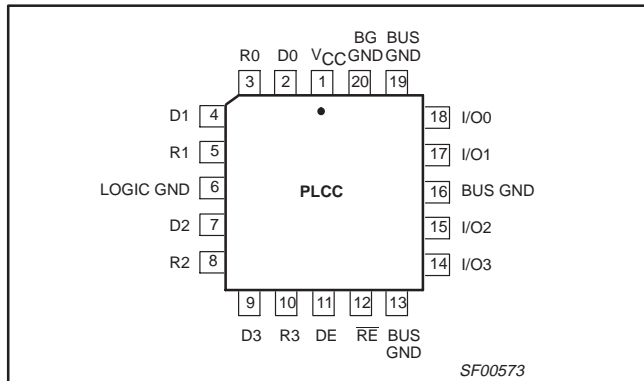
One (1.0) FAST unit load is defined as: 20 $\mu$ A in the high state and 0.6mA in the low state.

OC= Open collector.

# Quad Futurebus backplane transceiver

74F3893

## PIN CONFIGURATION



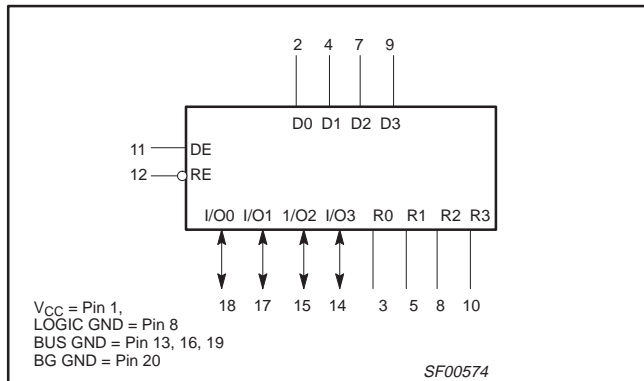
## FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	OPERATING MODE
DE	RE	Dn	I/On	Rn	
H	L	L	H	L	Transmit to bus
H	L	H	L	H	
H	H	Dn	$\bar{D}n$	Z	Receiver 3-state, transmit to bus
L	H	X	H	Z	
L	L	X	H	L	Receive, I/On = inputs
L	L	X	L	H	

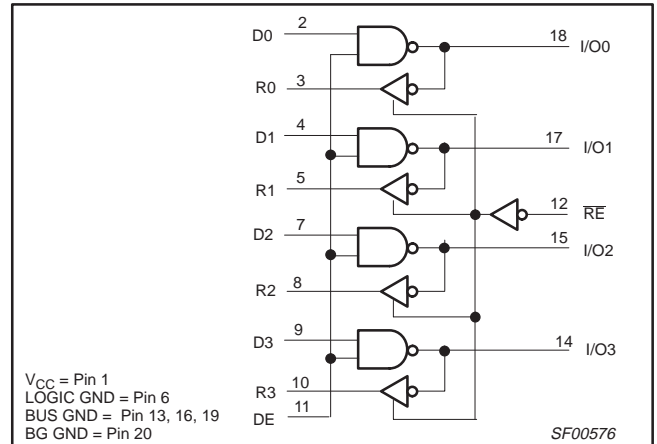
### Notes to function table

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

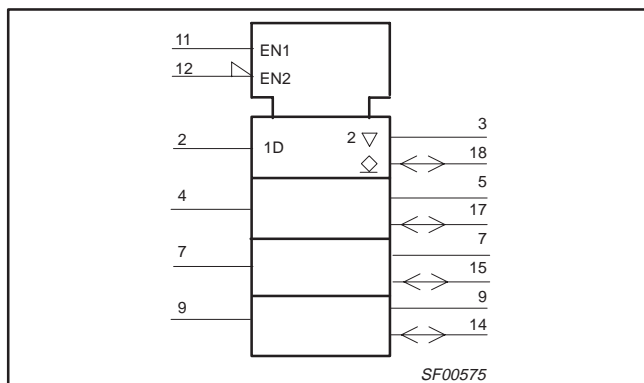
## LOGIC SYMBOL



## LOGIC DIAGRAM



## IEC/IEEE SYMBOL



## Quad Futurebus backplane transceiver

74F3893

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-1.5 to +6.5	V
V <sub>IN</sub>	Input voltage	-1.5 to +6.5	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state	-0.5 to 5.5	V
I <sub>OUT</sub>	Current applied to output in low output state	200	mA
T <sub>amb</sub>	Operating free air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	Dn, DE, RE	2.0			V
V <sub>IL</sub>	Low-level input voltage					
I <sub>Ik</sub>	Input clamp current				-18	mA
V <sub>TH</sub>	Bus input threshold	I/On only	1.475	1.55	1.625	mA
I <sub>OH</sub>	High-level output current	Rn only			-3	mA
I <sub>OL</sub>	Low-level output current				100	mA
T <sub>amb</sub>	Operating free air temperature range		0		+70	°C

## Quad Futurebus backplane transceiver

74F3893

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
				MIN	TYP <sup>2</sup>	MAX		
$I_{OH}$	High-level output current	I/On	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 1.5\text{V}$		10	100	$\mu\text{A}$	
$V_{OH}$	High-level output voltage	Rn	$V_{CC} = \text{MAX}, V_{IL} = 1.3\text{V}, \overline{RE} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.5			V	
$V_{OHB}$	High-level output bus voltage	I/On	$V_{CC} = \text{MAX}, D_n = DE = 0.8\text{V}, V_T = 2.0\text{V}, R_T = 10\Omega, \overline{RE} = 2.0\text{V}$	2.5			V	
$V_{OL}$	Low-level output voltage	Rn	$V_{CC} = \text{MIN}, V_{IN} = 1.8\text{V}, \overline{RE} = 0.8\text{V}, I_{OL} = 6\text{mA}$		0.35	0.5	V	
$V_{OLB}$	Low-level output bus voltage	I/On	$D_n = DE = V_{IH}, I_{OL} = 100\text{mA}$	0.75	1.0	1.2	V	
			$D_n = DE = V_{IH}, I_{OL} = 80\text{mA}$	0.75	1.0	1.1	V	
$V_{OCB}$	Driver output positive clamp voltage	I/On	$V_{CC} = \text{MAX or } 0\text{V},$			2.9	V	
			$D_n = DE = 0.8\text{V}, \overline{RE} = 2.0\text{V}$	I/On = 1mA	1.9		2.9	V
				I/On = 10mA	2.3		3.2	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage		$V_{CC} = \text{MAX}, V_I = 7.0\text{V}, DE = \overline{RE} = D_n = V_{CC}$			100	$\mu\text{A}$	
$I_{IH}$	High-level input current	$D_n, \overline{RE}, DE$	$V_{CC} = \text{MAX}, DE = \overline{RE} = D_n = 5.5\text{V}$			20	$\mu\text{A}$	
$I_{IHB}$	High-level I/O bus current (power off)	I/On	$V_{CC} = 0\text{V}, D_n = DE = 0.8\text{V}, I_{On} = 1.2\text{V}, \overline{RE} = 0\text{V}$			100	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$D_n, \overline{RE}$	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}, DE = 4.5\text{V}$			-40	$\mu\text{A}$	
		DE	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}, D_n = 4.5\text{V}$			-200	$\mu\text{A}$	
$I_{ILB}$	Low-level I/O bus current (power on)	I/On	$V_{CC} = \text{MAX}, D_n = DE = 0.8\text{V}, I_{On} = 0.75\text{V}, \overline{RE} = 0\text{V}$	-20		20	$\mu\text{A}$	
$I_{OZH}$	Off-state output current, high-level voltage applied	Rn	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}, \overline{RE} = 2\text{V}$			20	$\mu\text{A}$	
$I_{OZL}$	Off-state output current, low-level voltage applied		$V_{CC} = \text{MAX}, V_I = 0.5\text{V}, \overline{RE} = 2\text{V}$			-20	$\mu\text{A}$	
$I_{OS}$	Short circuit output current <sup>3</sup>	Rn	$V_{CC} = \text{MAX}$	-60		-150	mA	
$I_{CC}$	Supply current <sup>4</sup> (total)		$V_{CC} = \text{MAX}, (\overline{RE} = V_{IH} \text{ or } V_{IL})$		55	80	mA	

**Notes to DC electrical characteristics**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}, T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

## Quad Futurebus backplane transceiver

74F3893

## AC ELECTRICAL CHARACTERISTICS FOR DRIVER AND DRIVER ENABLE

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>D</sub> = 50pF, R <sub>T</sub> = 10Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>D</sub> = 50pF, R <sub>T</sub> = 10Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to I/On	Waveform 1	1.0 1.5	2.0 3.0	5.0 5.5	1.0 1.5	5.5 6.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay DE to I/On	Waveform 1	1.0 1.5	2.0 3.0	4.5 5.5	1.0 1.5	5.5 6.0	ns
t <sub>TLH</sub> t <sub>THL</sub>	Dn to I/O transition time 10% to 90%, 90% to 10%	Waveform 1	1.0 1.0		4.0 4.0	1.0 1.0	5.0 5.0	ns
t <sub>sk(o)</sub>	Skew between drivers in same package			1.0				ns

## AC ELECTRICAL CHARACTERISTICS FOR RECEIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I/On to Rn	Waveform 2	1.0 3.6	2.0 5.5	4.5 7.5	1.0 3.6	5.5 8.5	ns

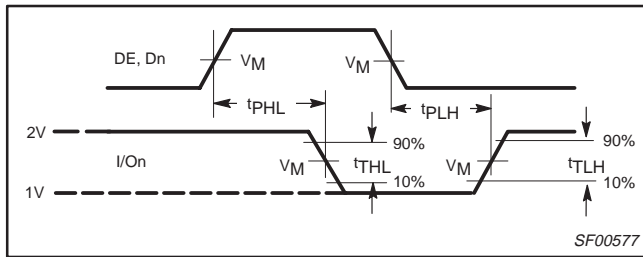
## AC ELECTRICAL CHARACTERISTICS FOR RECEIVER ENABLE

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level, RE to Rn	Waveform 3, 4	1.5 2.5	3.0 4.0	5.5 7.0	1.5 2.0	6.0 7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level, RE to Rn	Waveform 3, 4	1.5 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.5 6.0	ns

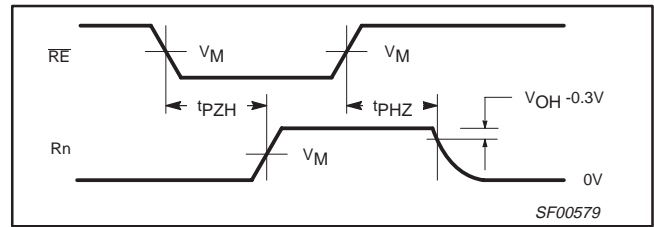
# Quad Futurebus backplane transceiver

74F3893

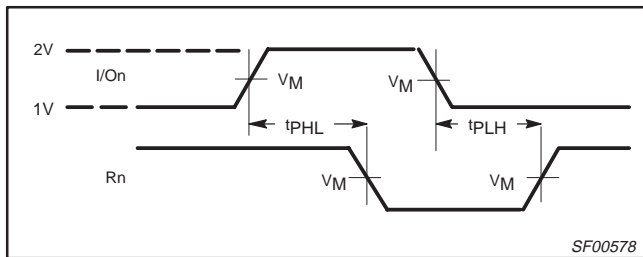
## AC WAVEFORMS



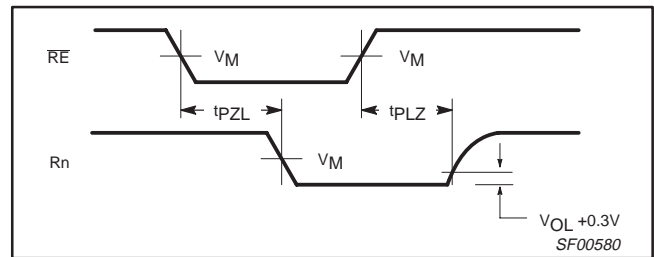
Waveform 1. Propagation delay for driver



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 2. Propagation delay for receiver



Waveform 4. 3-state output enable time to low level and output disable time from low level

### Notes to AC waveforms

- For all waveforms,  $V_M = 1.5V$ .
- The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUITS AND WAVEFORMS

TEST	SWITCH
$t_{PZL}$ , $t_{PZL}$	closed
All other	open

Test circuit for 3-state outputs on D port

Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
D port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
I/O port	2.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

Test circuit for outputs on I/O port

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_U$  = Pull up resistor; see AC Electrical Characteristics for value.  
 $C_D$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

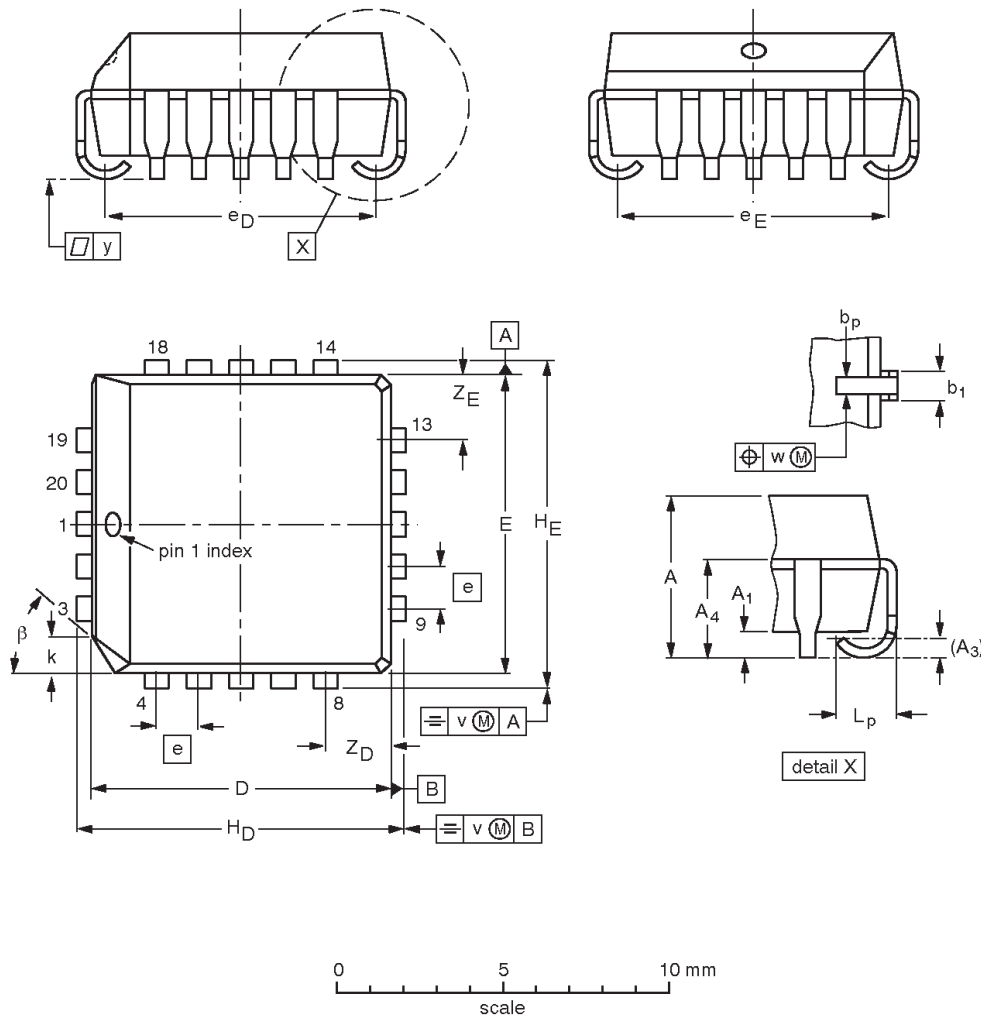
SF00581

# Quad futurebus backplane transceiver

74F3893

PLCC20: plastic leaded chip carrier; 20 leads

SOT380-1



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup> max.	Z <sub>E</sub> <sup>(1)</sup> max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT380-1		MO-047AA			95-02-25 97-12-16



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74F3893

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**NOTES**

## Quad futurebus backplane transceiver

74F3893

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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