National Semiconductor

August 1995

54F/74F410 Register Stack—16 x 4 RAM TRI-STATE® Output Register

General Description

The 'F410 is a register-oriented high-speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. TRI-STATE outputs are provided for maximum versatility. The 'F410 is fully compatible with all TTL families.

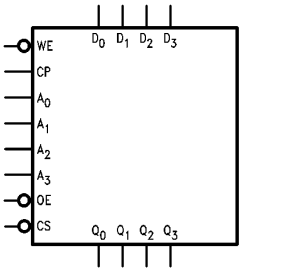
Features

- Edge-triggered output register
- Typical access time of 35 ns
- TRI-STATE outputs
- Optimized for register stack operation
- 18-pin package
- 9410 replacement

Commercial	Military	Package Number	Package Description
74F410PC		N18A	18-Lead (0.300″ Wide) Molded Dual-In-Line
	54F410DM (Note 1)	J18A	18-Lead Ceramic Dual-In-Line
74F410SC		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
54F410LM		W20A	20-Lead Cerpak

Note 1: Military grade device with environmental and burn-in processing. Use suffix = DMQB, LMQB

Logic Symbol



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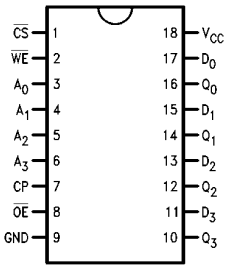
Connection Diagrams

Pin Assignment for DIP and SOIC



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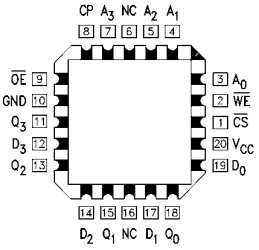
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	Address Inputs	1.0/1.0	20 μA/ $-$0.6 mA
D_0-D_3	Data Inputs	1.0/1.0	20 μA/ $-$0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/2.0	20 μA/ $-$1.2 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 μA/ $-$0.6 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 μA/ $-$0.6 mA
CP	Clock Input (Outputs Change on LOW-to-HIGH Transition)	1.0/2.0	20 μA/ $-$1.2 mA
Q_0-Q_3	TRI-STATE Outputs	150/40 (33.3)	$-$3 mA/24 mA (20 mA)

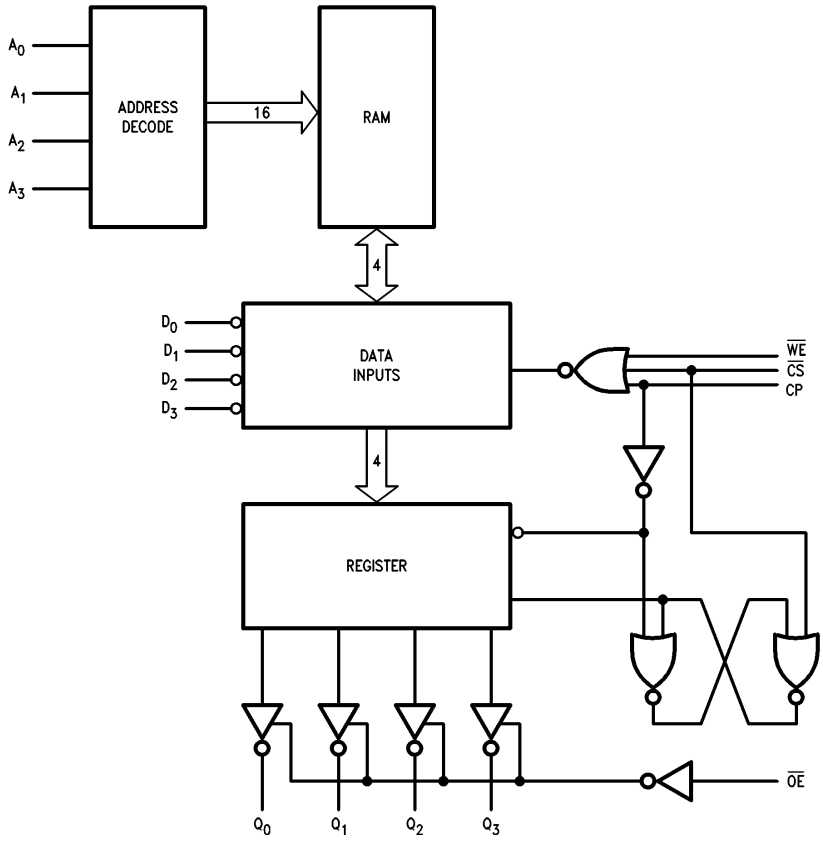
Functional Description

Write Operation—When the three control inputs, Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the data inputs (D_0-D_3) is written into the memory location selected by the address inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

Read Operation—Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs (A_0-A_3) are edge-triggered into the Output Register.

The ($\overline{OE}$) input controls the output buffers. When $\overline{OE}$ is HIGH the four outputs (Q_0-Q_3) are in a high impedance or OFF state; when $\overline{OE}$ is LOW, the outputs are determined by the state of the Output Register.

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (A_n, D_n, $\overline{OE}$, $\overline{WE}$)
					−1.2			V_{IN} = 0.5V ($\overline{CS}$, CP)
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{CCH}	Power Supply Current		47	70	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		47	70	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		47	70	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V C_L = 50 pF		54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay CP to Q	3.0 3.5	8.5 9.0	2.5 3.0	11.0 12.0	2.5 3.0	9.5 10.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to Q	3.0 3.5	8.0 9.0	2.5 3.0	10.5 13.0	2.5 3.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to Q	2.5 2.5	6.5 7.0	2.0 2.0	8.5 9.5	2.0 2.0	7.5 8.0	

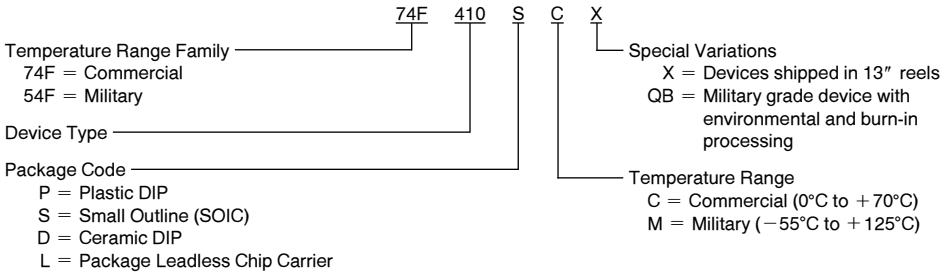
AC Operating Requirements

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
READ MODE								
t_s(H) t_s(L)	Setup Time, HIGH or LOW A_n to CP	15.0 15.0		23 23		17.0 17.0		ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW A_n to CP	0 0		0 0		0 0		ns
WRITE MODE								
t_s(H) t_s(L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0		0 0		0 0		ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0		0 0		0 0		ns
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	5.0 5.0		8.5 8.5		6.0 6.0		ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0		2.5 2.5		0 0		ns
t_w	$\overline{WE}$ Pulse Width Required to Write	7.5		9.5		8.5		ns
t_w	$\overline{CS}$ Pulse Width Required to Write	7.5		9.5		8.5		ns
t_w	CP Pulse Width Required to Write	7.5		9.5		8.5		ns

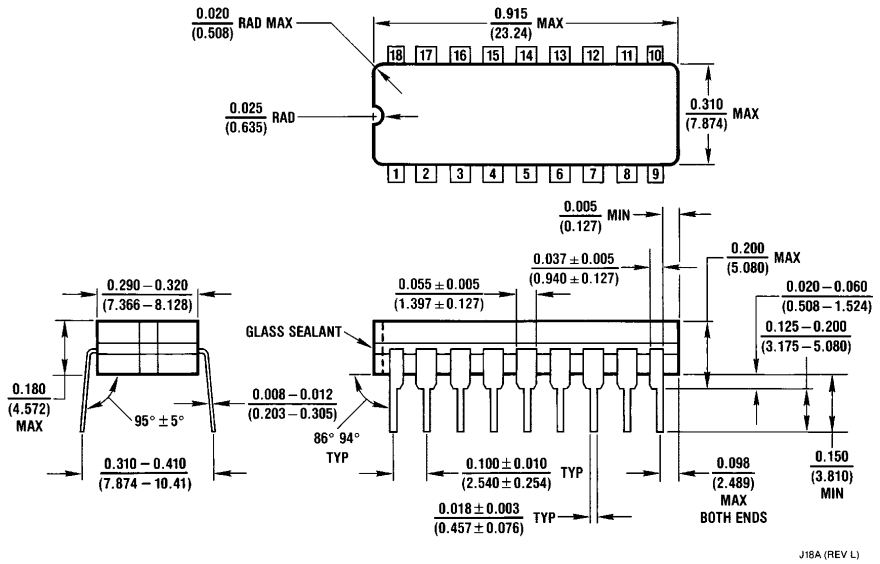
Note: Military temperature range for this device is −40°C to +85°C.

Ordering Information

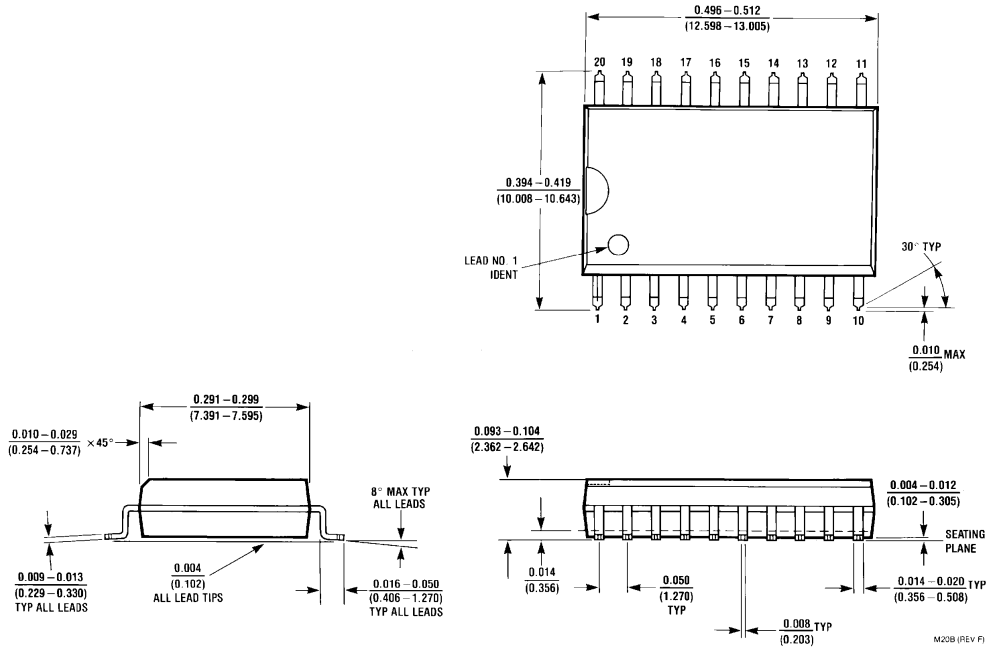
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

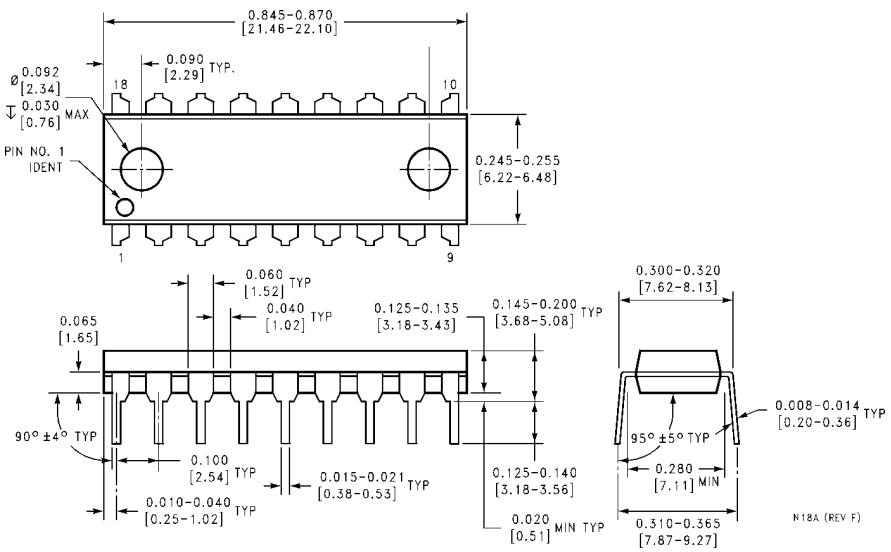


18-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J18A



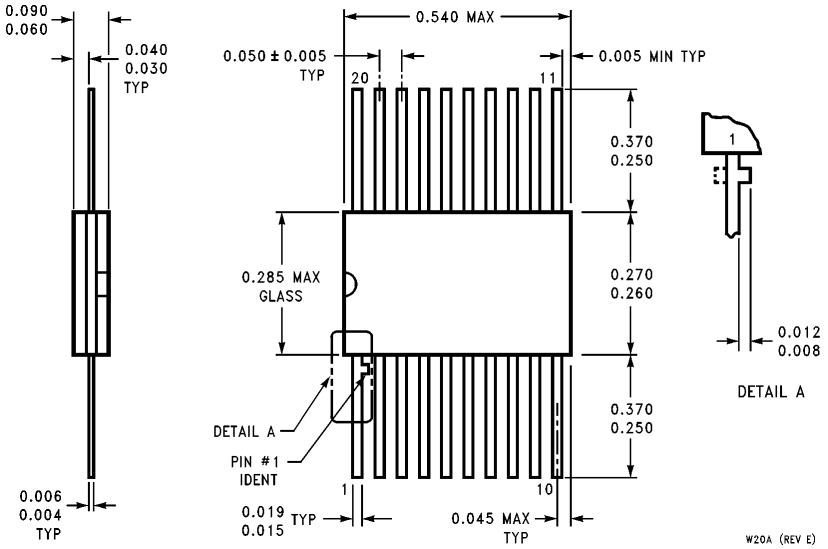
20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



18-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N18A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Cerpack
NS Package Number W20A

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