National Semiconductor

August 1995

74F525
Programmable Counter

General Description

The 'F525 is a multi-function 28-pin device. It consists of a 16-bit count-down counter, logic to control the counter, logic to control the state of the outputs and a PLA to decode the particular function selected by the user. The list of high-speed timing applications include:

Features

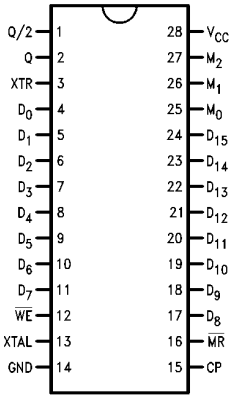
- Baud rate generator
- Digitally programmed monostable
- Variable system frequency generator
- Digital filter variable sampling rate
- 16-bit data path
- External trigger
- Extremely accurate one shot w/pulse widths from 50 ns to 3.27 ms @CP = 40 MHz

Commercial	Package Number	Package Description
74F525QC (Note 1)	V28A	28-Lead Molded Plastic Leaded Chip Carrier
74F525SC (Note 1)	M28B	28-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F525PC	N28B	28-Lead (0.600″ Wide) Molded Dual-In-Line Package

Note 1: Devices also available in 13″ reel. Use suffix = SCX and QCX.

Connection Diagrams

Pin Assignment DIP and SOIC



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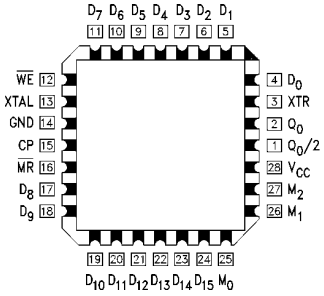
Pin Assignment for PCC



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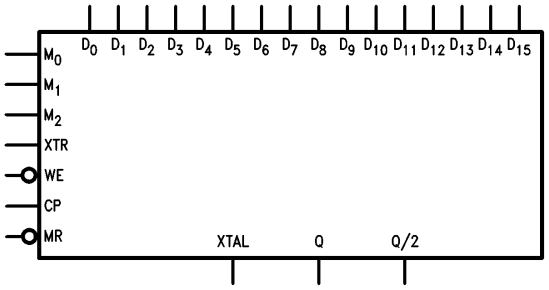
RRD-B30M105/Printed in U. S. A.

Logic Symbol



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Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
Q	Ouput (Primarily indicates when the counter has reached zero)	50/33.3	−1 mA/20 mA
Q/2	Output (Divides Q by 2)	50/33.3	−1 mA/20 mA
M_0–M_2	Status Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{MR}$	Master Reset	1.0/1.0	20 μA/−0.6 mA
CP	Clock Pulse	1.0/2.0	20 μA/−1.2 mA
D_0–D_{15}	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{WE}$	Write Enable Input	1.0/1.0	20 μA/−0.6 mA
XTR	External Trigger Input	1.0/2.0	20 μA/−1.2 mA
XTAL	Crystal Output	1.0/1.0	20 μA/−0.6 mA

Functional Description

The multi-function aspect of the device consists of eight different modes of operation. An explanation of the operation of the device in each of the modes follows. However, there is one operation that is independent of the selected mode: the loading of data. Data is latched into a set of data latches when $\overline{WE}$ is brought from a LOW to a HIGH state. The latches are transparent when $\overline{WE}$ is held LOW.

Operation Notes:

1. Device should be reset before operation.
2. The XTR input acts as a select line for the clock.
3. With XTR low, the clock goes into the counter.
4. With XTR high, the clock loads the counter.
5. In mode 4 and 5, during counting, the counter cannot be reloaded. XTR high freezes the count.
6. Mode 7 is the only auto-reload mode, all other modes require and XTR pulse to begin.
7. Loading 0 into the latches idles the device.

MODE 0: Interval Timer with Level Output

While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally LOW, is brought HIGH and Q/2 toggles state. Taking XTR HIGH at any time enables the data in the data latches to be loaded into the counter on the rising edge of CP and clears Q. See *Figure 1*.

MODE 1: Interval Timer with Inverted Level Output

The operation is exactly the same as in Mode 0 except that Q is normally HIGH and goes LOW when the count reaches zero. Q/2 toggles on the negative-edge of Q. See *Figure 1*.

MODE 2: Interval Timer with Pulse Output

While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally LOW, is brought HIGH for a single period of CP. Q/2 toggles state on the positive edge of Q. Taking XTR HIGH at any time causes the data in the data latches to be loaded into the counter on the rising edge of CP and clears Q. See *Figure 2*.

MODE 3: Interval Timer with Inverted Pulse Output

The operation is exactly the same as in Mode 2 except that Q is normally HIGH and goes LOW for a single period of CP. Q/2 toggles on the negative edge of Q. See *Figure 2*.

Functional Description (Continued)

Function Table

M_2	M_1	M_0	Function
0	0	0	Mode 0
0	0	1	Mode 1
0	1	0	Mode 2
0	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5
1	1	0	Mode 6
1	1	1	Mode 7

MODE 4: Interval Timer, Pulse Output with Count Hold

While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally low, is brought HIGH for a single period of CP. Q/2 toggles state on the positive edge of Q. Taking XTR HIGH before the counters reach zero, stops the count-down from the point where it was held. Data cannot be reloaded into the counter until a count of zero is reached. See *Figure 3*.

MODE 5: Interval Timer, Inverted Pulse Output with Count Hold

The operation is exactly the same as Mode 4 except that Q is normally HIGH and goes LOW for a single period of CP. Q/2 toggles on the negative-edge of Q. See *Figure 3*.

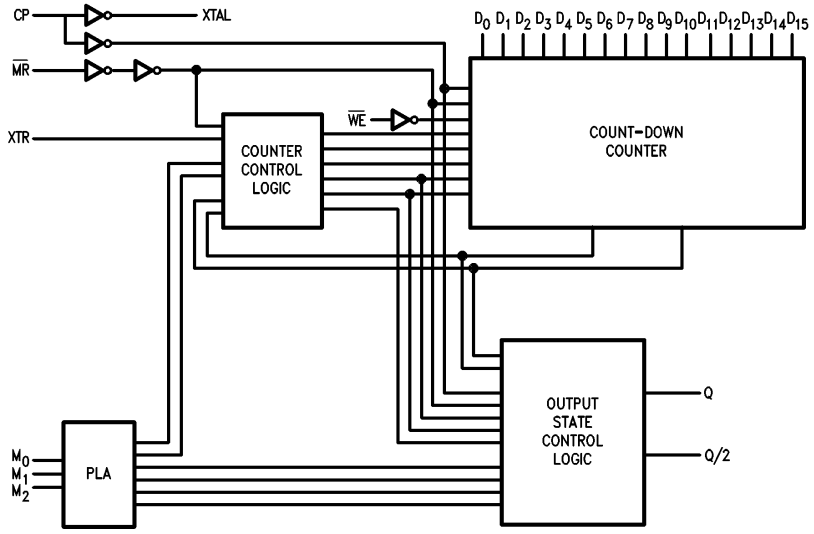
MODE 6: Retriggerable Synchronous One-Shot

When XTR is HIGH, the data in the data latches is loaded into the counter upon the positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP, wehre Q, normally LOW, is then brought HIGH and the counter is decremented when the count reaches zero, Q is brought LOW, and Q/2 is toggled. Bringing XTR HIGH during the count-down will allow the data in the data latches to be loaded into the counter with the next positive edge of CP, but will not affect Q. See *Figure 4*. NOTE that the pulse width of Q will be N-1 clock cycles, where N is the number loaded into the counter. N = 1 should not be used as this may cause unpredictable results.

MODE 7: Frequency Generator

When XTR is HIGH, the data in the data latches is loaded into the counter upon the positive edge of CP. The negative edge of XTR enables the count-down to begin with the next positive edge of CP. When the count reaches zero, Q, normally LOW, is brought HIGH for a single period of CP and Q/2 is toggled. The same clock edge that brings Q HIGH, also loads the data in the data latches into the counter. The counter will start to count on the next positive edge of CP. This mode will run continuously after an initial XTR until stopped by MR. Taking XTR HIGH at any time causes the data in the data latches to be loaded into the counter and Q output to be cleared with the next positive edge of CP. See *Figure 5*.

Block Diagram



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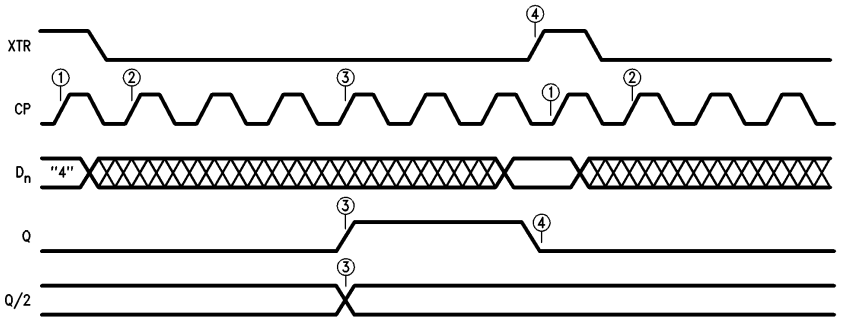
Timing Diagrams



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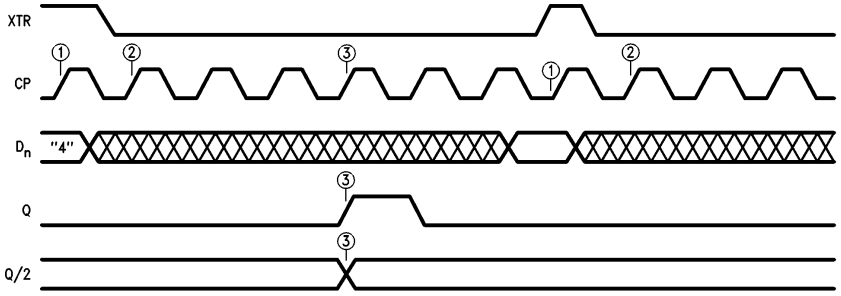
①With XTR HIGH, the rising edge of CP loads data from the latches to the counter.
②With XTR LOW, the rising edge of CP begins count-down cycle.
③When the count reaches zero, Q goes HIGH, and Q/2 toggles state.
④The next occurrence of XTR clears Q.

FIGURE 1. MODE 0 and MODE 1 (Inverse Output of Mode 0)
$\overline{M}_n$ = 000, 001



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①With XTR HIGH, the rising edge of CP loads data from the latches to the counter.
②With XTR LOW, the rising edge of CP begins the count-down cycle.
③When the count reaches zero, Q goes HIGH for one period of CP, and Q/2 toggles state.

FIGURE 2. MODE 2 and MODE 3 (Inverse Output of Mode 2)
$\overline{M}_n$ = 010, 011

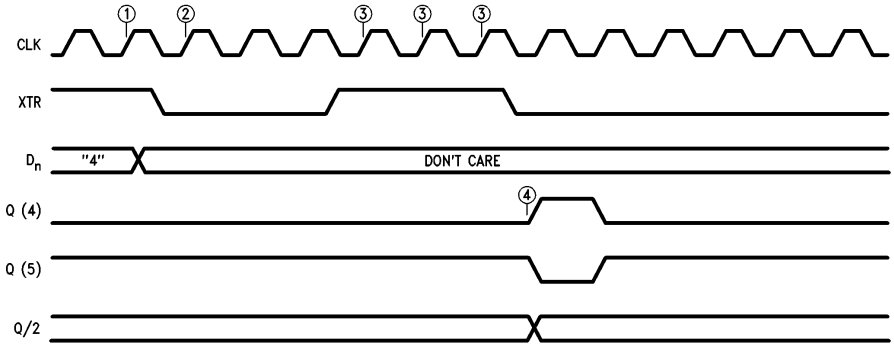

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FIGURE 3. MODE 4 and MODE 5
$\overline{M}_n$ = 100, 101

①With XTR HIGH, the rising edge of CP loads data from the latches into the counter.
②With XTR LOW, the rising edge of CP begins the count-down.
③With XTR HIGH, during count-down, the rising edge of CP does nothing.
④When the count reaches zero, Q goes HIGH for one clock cycle and Q/2 toggles state.
Note: Once the count reaches zero, the counter can be reloaded with XTR HIGH.

Timing Diagrams (Continued)

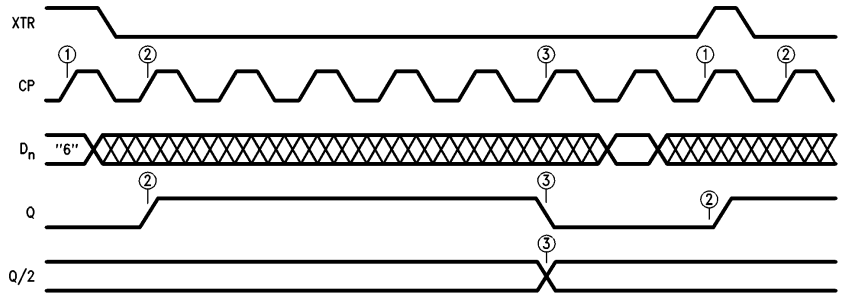

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FIGURE 4. MODE 6
$\overline{M}_n$ = 110

①With XTR HIGH, the rising edge of CP loads data from the latches to the counter.

②With XTR LOW, the rising edge of CP begins the count, and Q goes HIGH.

③When the count reaches zero, Q goes LOW, and Q/2 toggles state. Bringing XTR HIGH before count reaches zero will reload the counter, but not affect Q.

Notes:

Loading N = 0 halts counter; loading N = 1 will result in undefined operation.

Pulse width = (2/CP) * (N − 1)

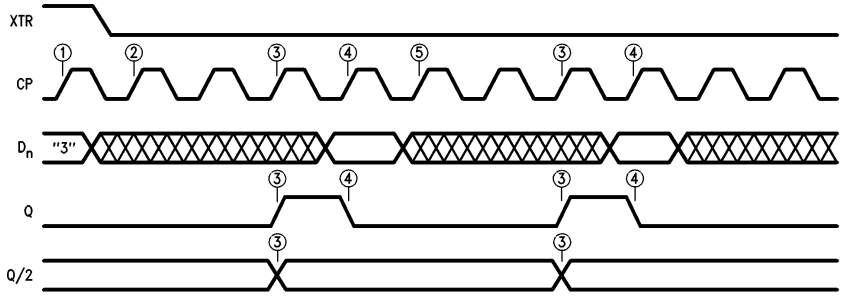

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FIGURE 5. MODE 7
$\overline{M}_n$ = 111

①With XTR HIGH, the rising edge of CP, loads data from the latches to the counter.

②On the falling edge of XTR, the rising edge of CP begins count-down.

③When count reaches zero, Q goes HIGH for one period of CP, and Q/2 toggles on the Q rising edge.

④On the rising edge of CP on which Q goes LOW, the counters are reloaded.

⑤Count-down begins again.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC} 74F 5% V_{CC}	2.5 2.7			V	Min	I_{OH} = −1 mA I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6 −1.2	mA	Max	V_{IN} = 0.5V (D0–D15) V_{IN} = 0.5V (CP, XTR)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			106	160	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			106	160	mA	Max	V_O = LOW

AC Electrical Characteristics

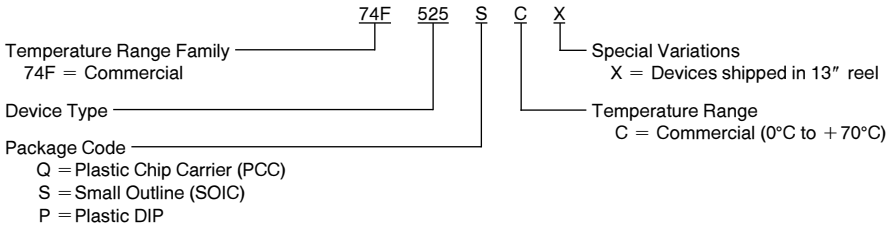
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	50	60		40		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q	9.0 8.0	16.0 12.0	20.5 15.5	8.0 7.0	22.5 17.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q/2	9.0 10.0	15.5 15.5	20.0 20.0	8.0 9.0	22.0 22.0	ns
t_{PLH} t_{PHL}	Propagation Delay XTR to Q	8.5 6.0	12.0 10.5	15.5 13.5	7.5 5.0	17.5 15.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Q	11.5 9.0	16.5 12.5	21.0 16.0	10.5 8.0	23.0 18.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$to Q/2	8.0 7.0	14.0 10.5	17.5 13.5	7.0 6.0	19.5 15.0	ns
t_{PLH} t_{PHL}	Propagation Delay M_n to Q	10.0 10.5	15.0 17.0	19.0 21.5	9.0 9.5	21.0 23.5	ns

AC Operating Requirements

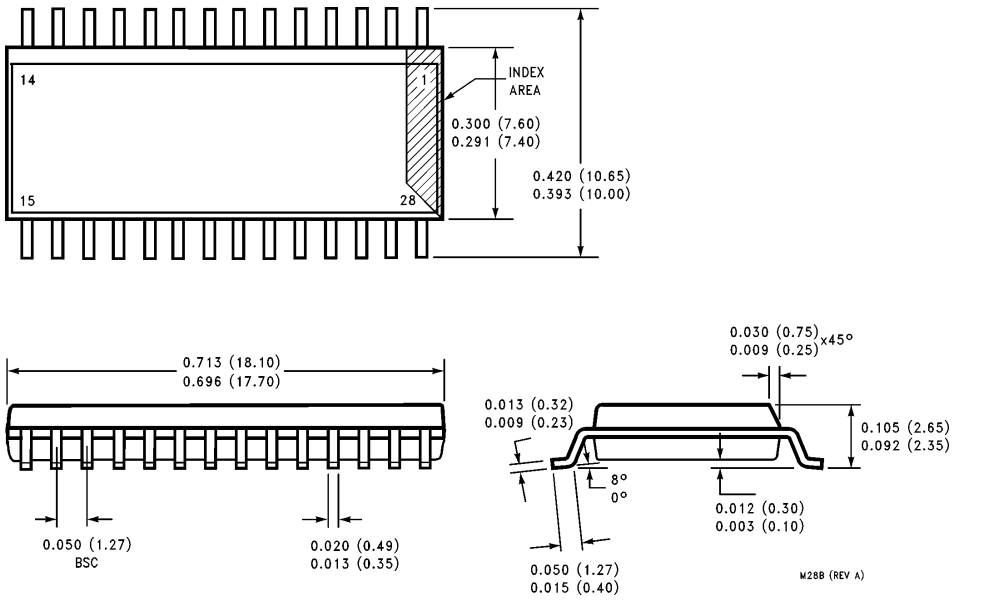
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{WE}$	2.0 4.0		2.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 2.0		0 2.5		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	9.0 10.5		10.0 12.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0 0		0 0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW XTR to CP	7.0 8.0		8.0 9.0		ns
$t_h(H)$	Hold Time, HIGH or LOW XTR to CP	0		0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Mode to CP	33.5 33.5		35.5 35.5		ns
$t_w(H)$	XTR Pulse Width, HIGH	11.5		13.0		ns
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	7.0		8.0		ns
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	4.5		5.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	3.5 9.5		4.0 10.5		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0		6.0		ns
t_{rec}	Recovery Time Mode to CP	30.0		32.0		ns

Ordering Information

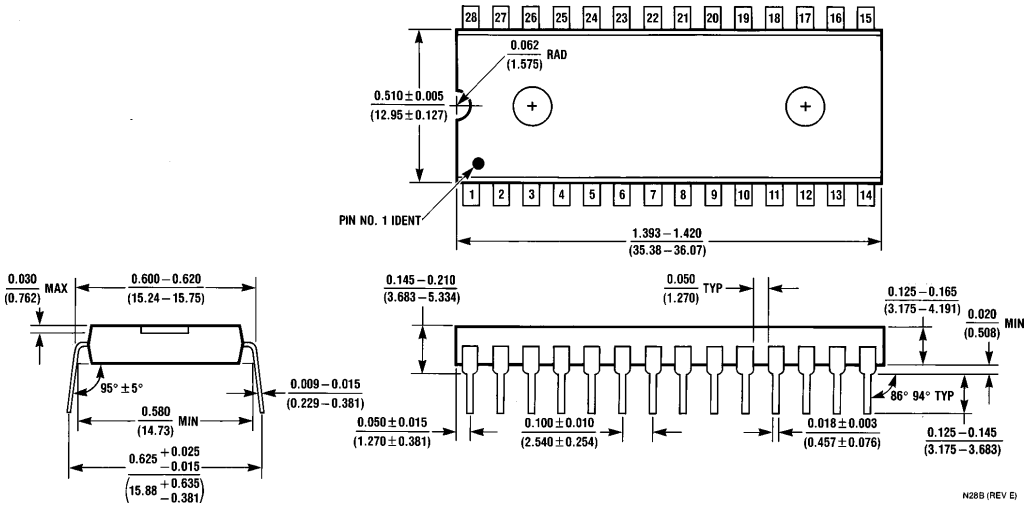
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

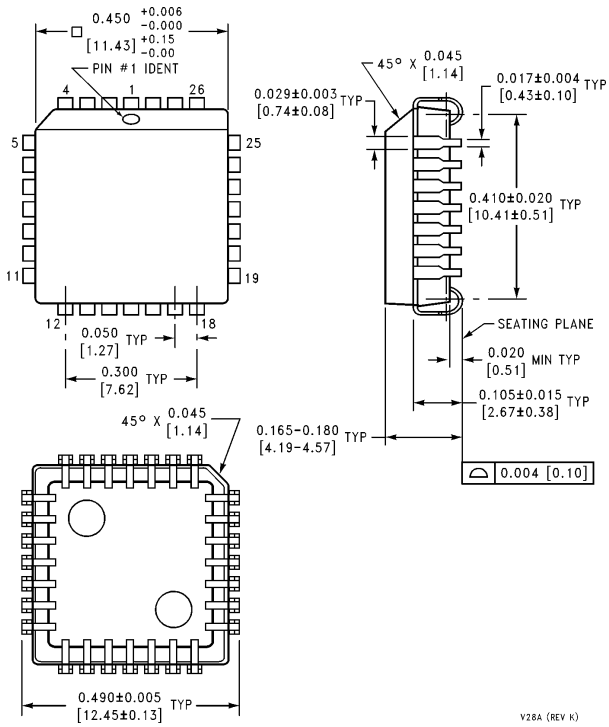


28-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M28B



28-Lead (0.600″ Wide) Molded Dual-In-Line Package, (P)
NS Package Number N28B

Physical Dimensions inches (millimeters) (Continued)



28-Lead Molded Plastic Leaded Chip Carrier (Q)
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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