DATA SHEET

~~74F533~~*,74F534
Latch/flip-flop

** Discontinued part. Please see the Discontinued Product List.*

Product specification
Supersedes data of 1989 May 11
IC15 Data Handbook

1999 Jan 08

Philips Semiconductors

PHILIPS

Latch/flip-flop

~~74F533,~~* 74F534

74F533 Octal Transparent Latch, Inverting (3-State)
74F534 Octal D Flip-Flop, Inverting (3-State)

FEATURES

- 8-bit positive edge-triggered register – 74F534
- 3-State inverting output buffers
- Common 3-State Output register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74F533 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance “off” state, which means they will neither drive nor load the bus.

The 74F534 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop’s $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance “off” state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	5.5ns	41mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F534N	SOT146-1
20-Pin Plastic SOL	N74F534D	SOT163-1

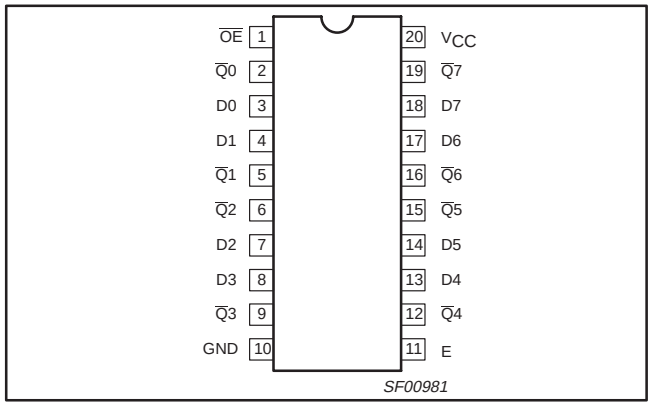
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20µA/0.6mA
E (74F533)	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP (74F534)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q}$0 - $\overline{Q}$7	Data outputs	150/40	3.0mA/24mA

** Discontinued part. Please see the Discontinued Products List.*

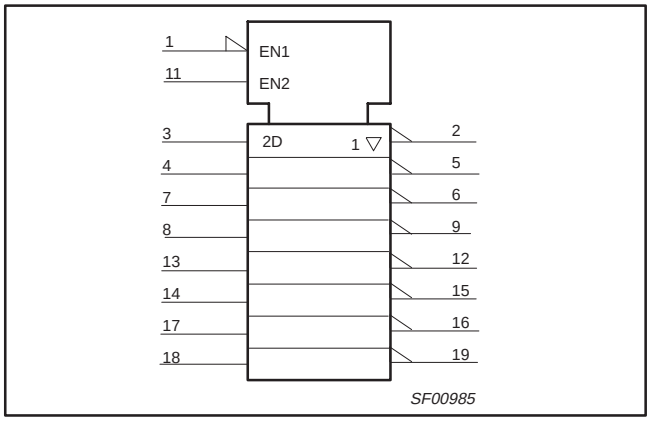
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION – 74F533



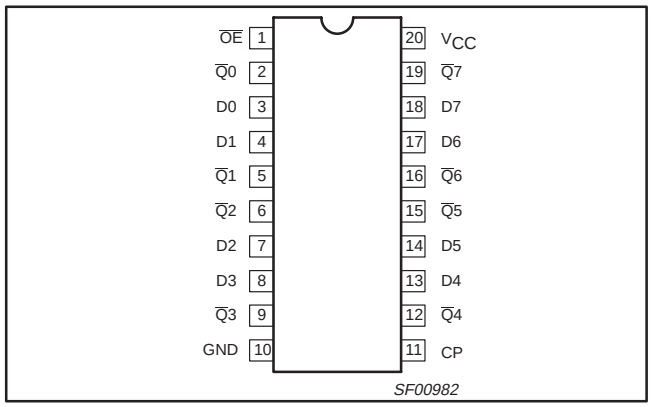
SF00981

LOGIC SYMBOL (IEEE/IEC) – 74F533



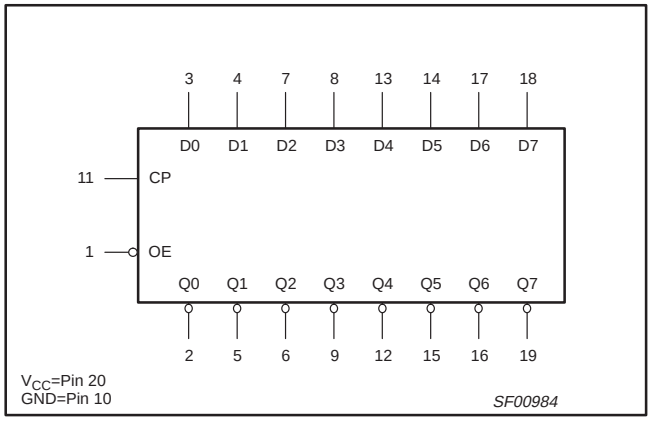
SF00985

PIN CONFIGURATION – 74F534



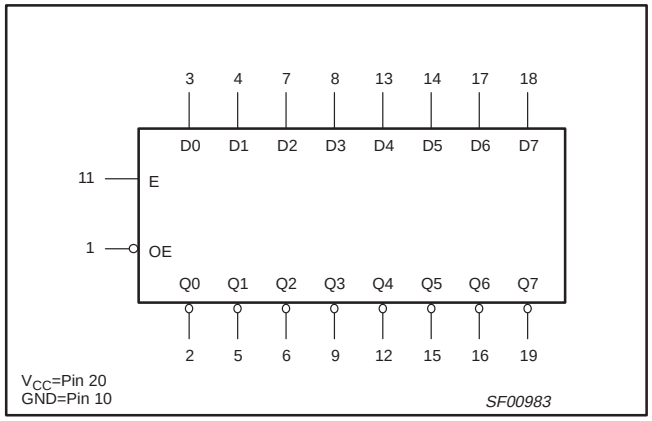
SF00982

LOGIC SYMBOL – 74F534



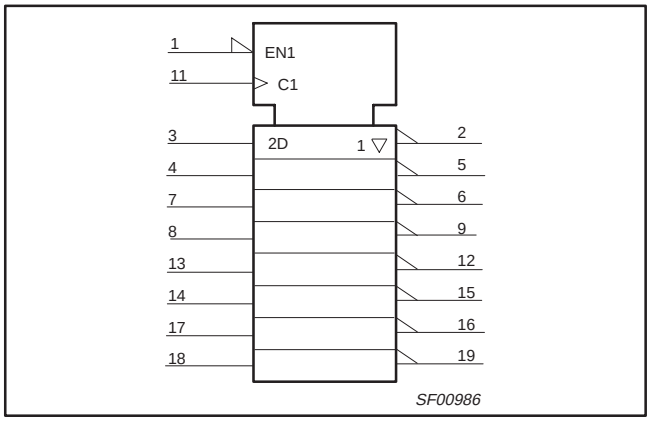
SF00984

LOGIC SYMBOL – 74F533



SF00983

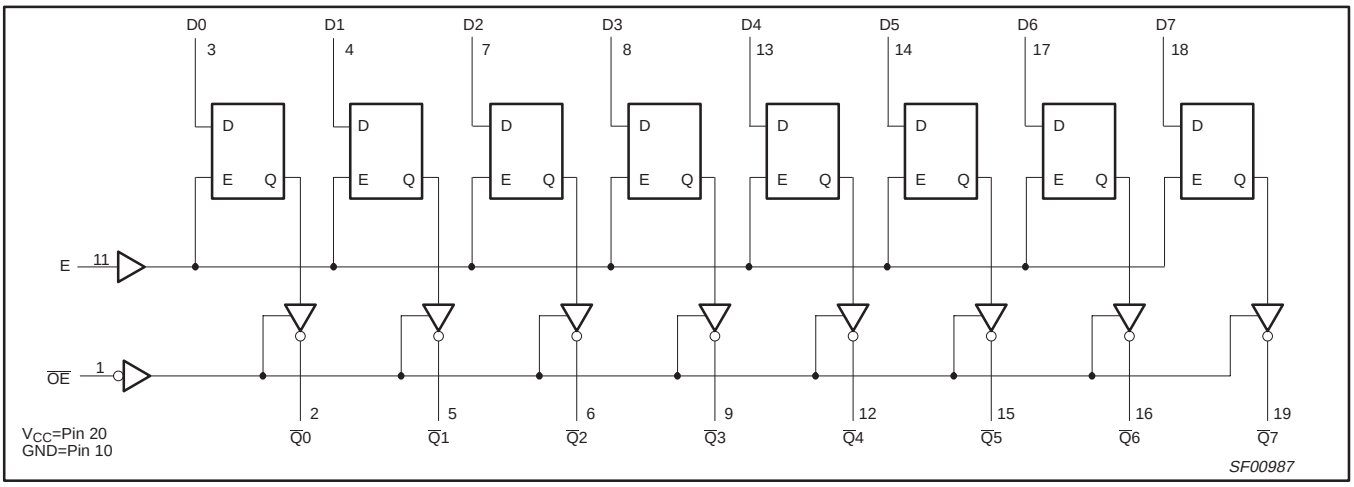
LOGIC SYMBOL (IEEE/IEC) – 74F534



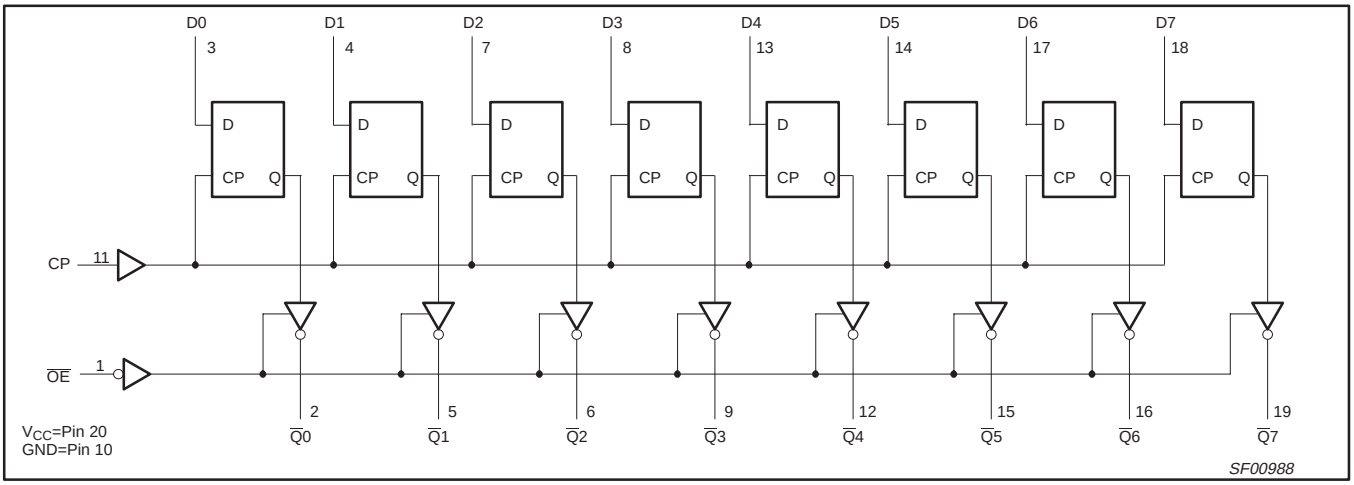
SF00986

** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F533



LOGIC DIAGRAM – 74F534



FUNCTION TABLE – 74F533

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	$\overline{E}$	Dn		$\overline{Q0}$ – $\overline{Q7}$	
L	H	L	L	H	Load and read register
L	H	H	H	L	
L	↓	l	L	H	Enable and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

** Discontinued part. Please see the Discontinued Products List.*

FUNCTION TABLE – 74F534

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	CP	Dn		$\overline{Q0}$ – $\overline{Q7}$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↧	X	NC	NC	Hold
H	↧	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

** Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	74F533	V_{CC} = MAX	$\overline{OE}$=4.5V, Dn=E=GND		41	61	mA
		74F534		$\overline{OE}$=4.5V, Dn=GND		51	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS T_{amb}= +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74F533	Waveform 2	4.0 3.0	6.0 4.5	8.5 7.0	4.0 3.0	9.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}$n		Waveform 3	5.0 3.0	6.5 4.5	9.5 7.0	5.0 3.0	10.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.0 7.0	2.0 2.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.0	6.0 5.5	2.0 2.0	7.0 6.5	ns
f_{MAX}	Maximum Clock frequency	74F534	Waveform 1	150	165		135		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n		Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns

** Discontinued part. Please see the Discontinued Products List.*

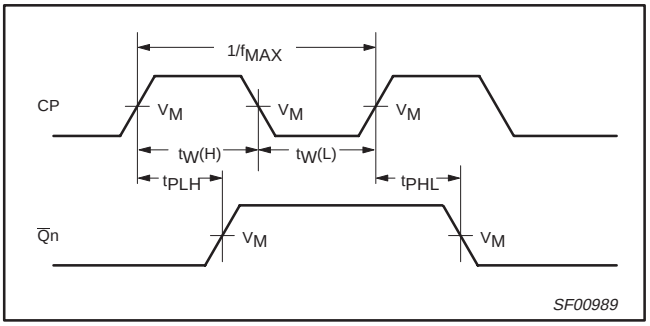
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb}= +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, Dn to E	74F533	Waveform 4	1.5 0			1.5 0		ns
$t_h(H)$ $t_h(L)$	Hold time, Dn to E		Waveform 4	2.5 2.5			2.5 2.5		ns
$t_w(H)$	E Pulse width, High		Waveform 3	3.0			3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, Dn to CP	74F534	Waveform 5	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, Dn to CP		Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		Waveform 1	3.0 3.5			3.5 4.0		ns

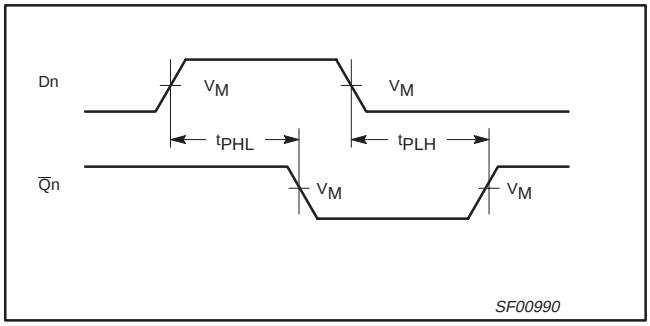
AC WAVEFORMS

For all waveforms, V_M = 1.5V

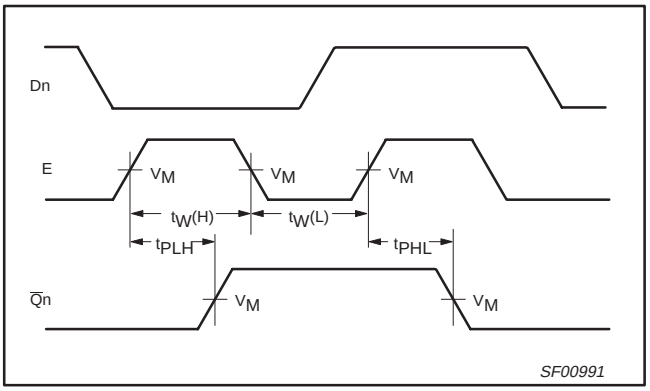
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



Waveform 2. Propagation Delay for Data to Output



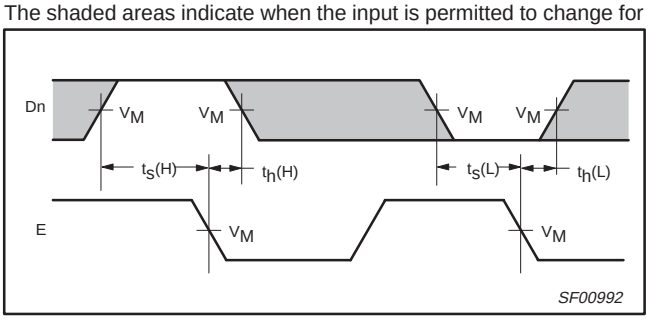
Waveform 3. Propagation Delay, Enable Input to Output, and Enable Pulse Width

** Discontinued part. Please see the Discontinued Products List.*

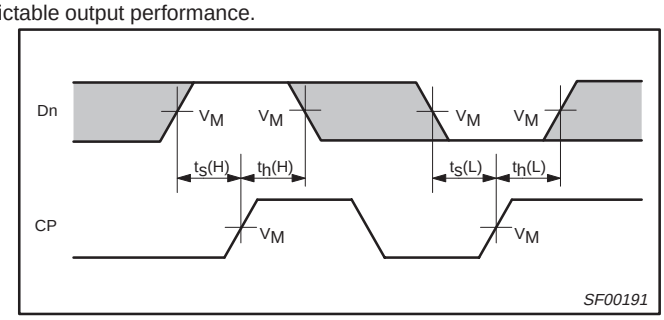
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V

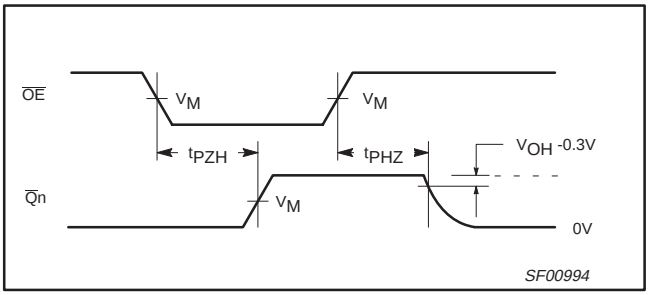
The shaded areas indicate when the input is permitted to change for predictable output performance.



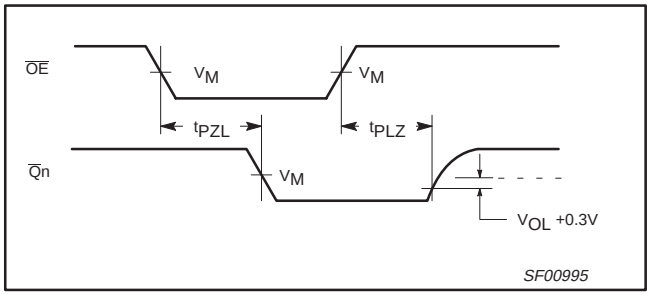
Waveform 4. Data Setup and Hold Times



Waveform 5. Data Setup and Hold Times

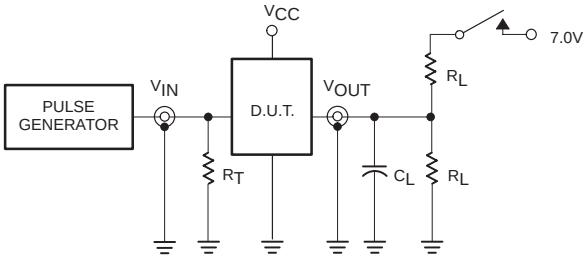


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level

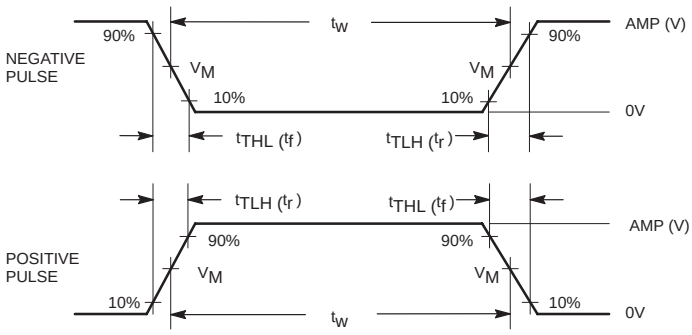


Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

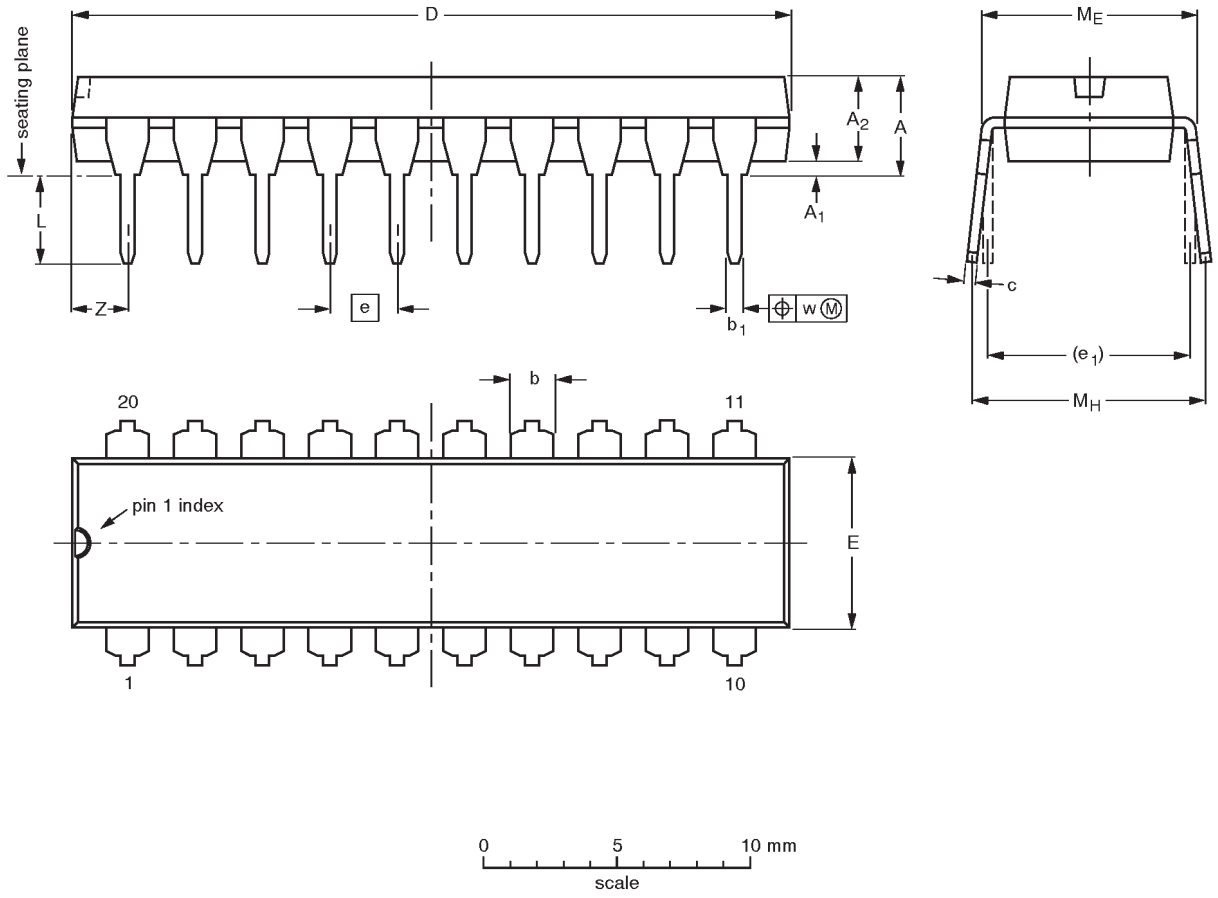
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

** Discontinued part. Please see the Discontinued Products List.*

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

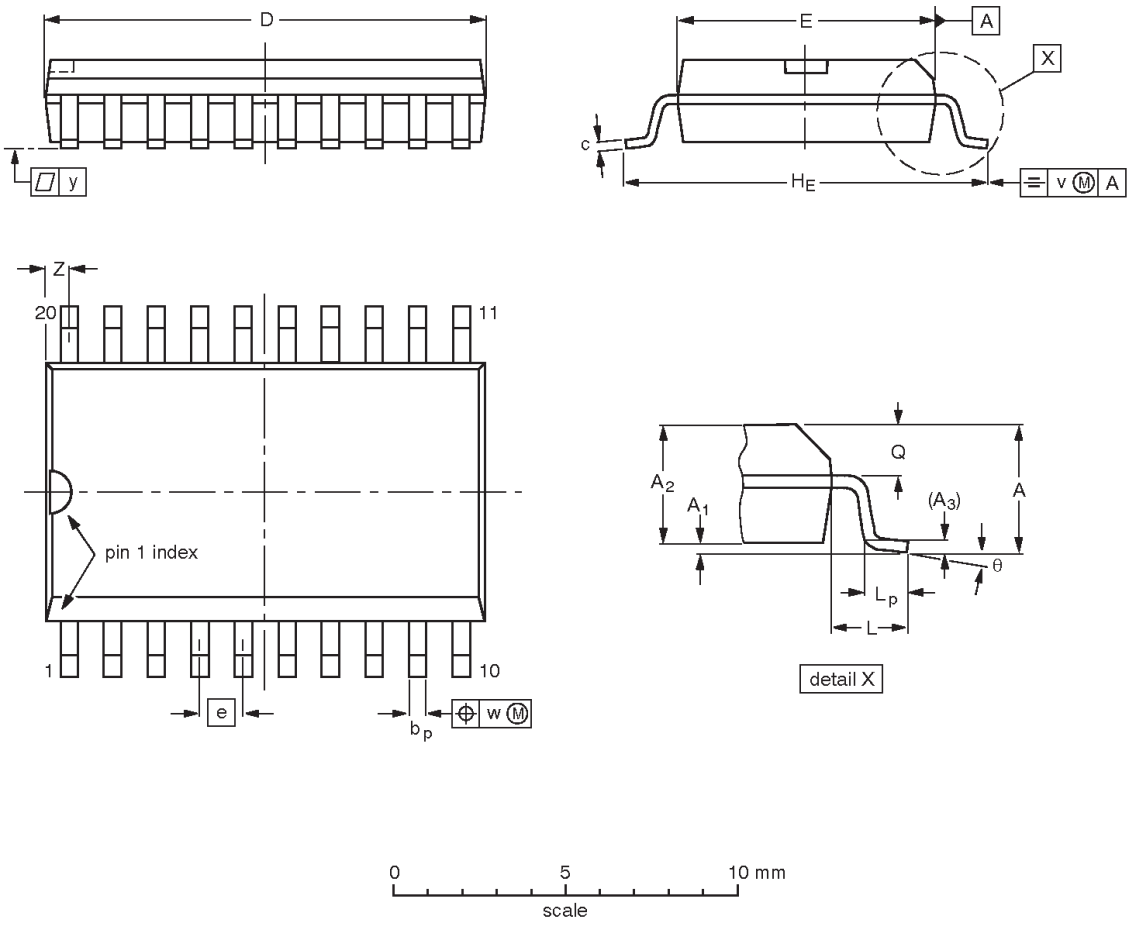
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

** Discontinued part. Please see the Discontinued Product List.*

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

** Discontinued part. Please see the Discontinued Product List.*

NOTES

** Discontinued part. Please see the Discontinued Product List.*

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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print code Date of release: 10-98

Document order number: 9397-750-05132

** Discontinued part. Please see the Discontinued Product List.*

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