

54F/74F544 Octal Registered Transceiver

General Description

The 'F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil). The 'F544 inverts data in both directions.

Features

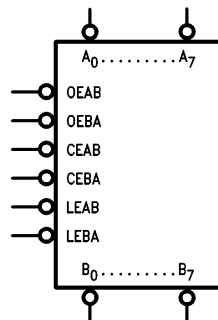
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil), B outputs sink 64 mA (48 mA Mil)
- 300 mil slim PDIP

Commercial	Military	Package Number	Package Description
74F544SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F544DM (Note 2)	J24A	24-Lead Ceramic Dual-In-Line
	54F544SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F544SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F544MSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II
	54F544FM (Note 2)	W24C	24-Lead Cerpack
	54F544LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

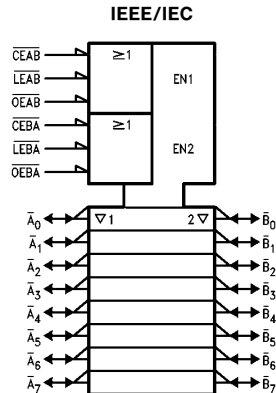
Note 1: Devices also available in 13" reel. Use suffix = SCX and MSAX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

Logic Symbols



TL/F/9555-2

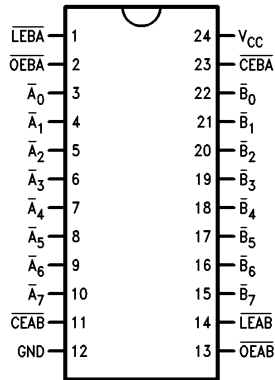


TL/F/9555-1

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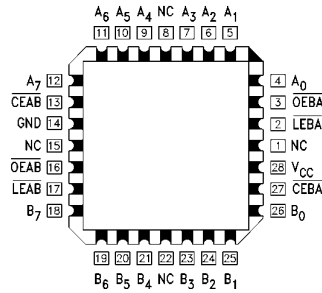
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



TL/F/9555-3

Pin Assignment
for LCC



TL/F/9555-4

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{CEAB}	A-to-B Enable Input (Active LOW)	1.0/2.0	20 μ A/ -1.2 mA
\overline{CEBA}	B-to-A Enable Input (Active LOW)	1.0/2.0	20 μ A/ -1.2 mA
\overline{LEAB}	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{LEBA}	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
$\overline{A_0}-\overline{A_7}$	A-to-B Data Inputs or B-to-A TRI-STATE Outputs	3.5/1.083 150/40(33.3)	70 μ A/ -650 μ A -3 mA/24 mA (20 mA)
$\overline{B_0}-\overline{B_7}$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs	3.5/1.083 600/106.6(80)	70 μ A/ -650 μ A -12 mA/64 mA (48 mA)

Functional Description

The 'F544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{CEAB}) input must be LOW in order to enter data from $\overline{A_0}-\overline{A_7}$ or take data from $\overline{B_0}-\overline{B_7}$, as indicated in the Data I/O Control Table. With \overline{CEAB} LOW, a LOW signal on the A-to-B Latch Enable (\overline{LEAB}) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LEAB} signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{CEAB} and \overline{OEAB} both LOW, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the \overline{CEBA} , \overline{LEBA} and \overline{OEBA} inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

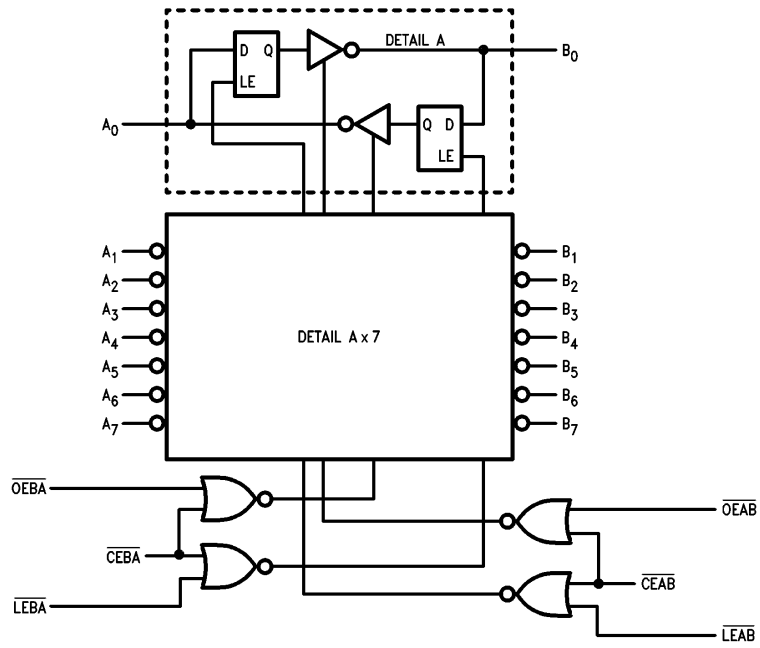
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} and \overline{OEBA}

Logic Diagram



TL/F/9555-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA, (except \bar{A}_n, \bar{B}_n)
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7		V	Min	I _{OH} = -1 mA (\bar{A}_n) I _{OH} = -3 mA (\bar{A}_n, \bar{B}_n) I _{OH} = -12 mA (\bar{B}_n) I _{OH} = -1 mA (\bar{A}_n) I _{OH} = -3 mA (\bar{A}_n, \bar{B}_n) I _{OH} = -15 mA (\bar{B}_n) I _{OH} = -1 mA (\bar{A}_n) I _{OH} = -3 mA (\bar{A}_n, \bar{B}_n)
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC}		0.5 0.55 0.5 0.55	V	Min	I _{OL} = 20 mA (\bar{A}_n) I _{OL} = 48 mA (\bar{B}_n) I _{OL} = 24 mA (\bar{A}_n) I _{OL} = 64 mA (\bar{B}_n)
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V (except \bar{A}_n, \bar{B}_n)
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V (except \bar{A}_n, \bar{B}_n)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V _{IN} = 5.5V (\bar{A}_n, \bar{B}_n)
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 250	μA	Max	V _{OUT} = V _{CC} (\bar{A}_n, \bar{B}_n)
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V ($\overline{OEAB}, \overline{OEBA}$) V _{IN} = 0.5V ($\overline{CEAB}, \overline{CEBA}$)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (\bar{A}_n, \bar{B}_n)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (\bar{A}_n, \bar{B}_n)

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{OS}	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V _{OUT} = 0V (\bar{A}_n) V _{OUT} = 0V (\bar{B}_n)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (\bar{A}_n, \bar{B}_n)
I _{CCH}	Power Supply Current		70	105	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		85	130	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		83	125	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

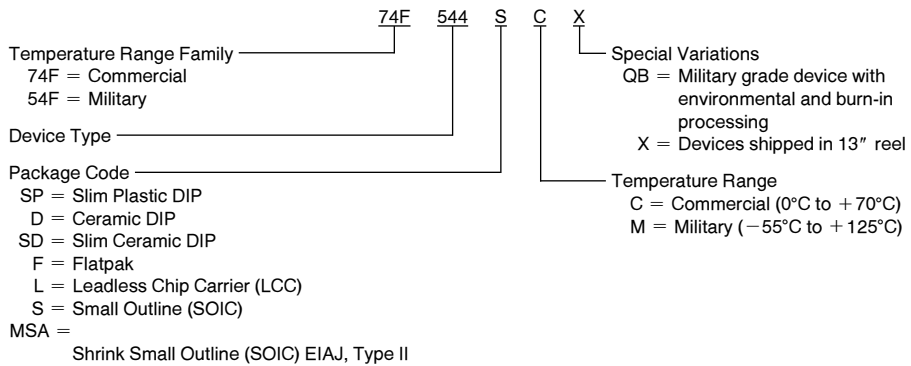
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode \bar{A}_n to \bar{B}_n or \bar{B}_n to \bar{A}_n	3.0 3.0	7.0 5.0	9.5 6.5	3.0 2.5	12.0 8.5	3.0 3.0	10.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to \bar{A}_n	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	18.0 11.5	6.0 4.0	14.5 10.5	ns
t _{PLH} t _{PHL}	Propagation Delay \bar{LEAB} to \bar{B}_n	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	18.0 11.5	6.0 4.0	14.5 10.5	ns
t _{PZH} t _{PZL}	Output Enable Time \bar{OEBA} or \bar{OEAB} to \bar{A}_n or \bar{B}_n CEBA or CEAB to \bar{A}_n or \bar{B}_n	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	11.0 13.0	3.0 4.0	10.0 12.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time \bar{OEBA} or \bar{OEAB} to \bar{A}_n or \bar{B}_n CEBA or CEAB to \bar{A}_n or \bar{B}_n	1.0 2.5	6.0 5.5	8.0 10.5	2.0 2.0	10.0 9.5	1.0 2.5	9.0 11.5	ns

AC Operating Requirements

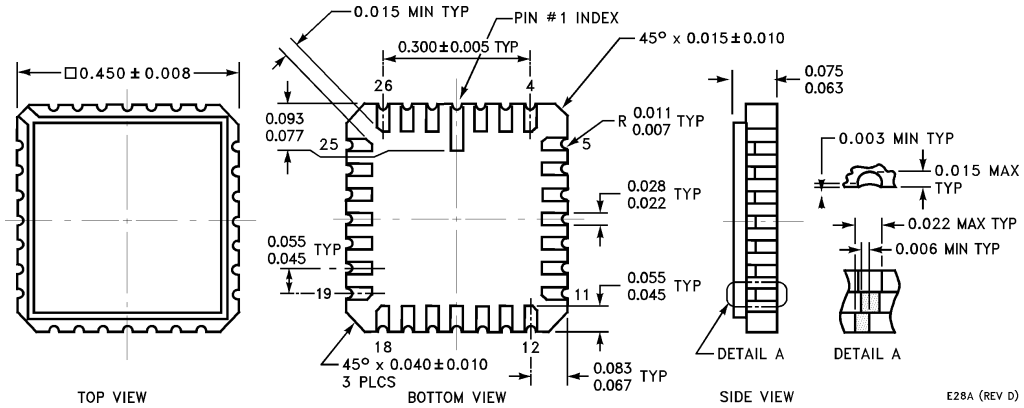
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW \bar{A}_n or \bar{B}_n to \bar{LEBA} or \bar{LEAB}	3.0 3.0		3.0 3.0		3.0 3.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW \bar{A}_n or \bar{B}_n to \bar{LEBA} or \bar{LEAB}	3.0 3.0		3.0 3.0		3.0 3.0		ns
t _w (L)	Latch Enable, B to A Pulse Width, LOW	6.0		9.0		7.5		ns

Ordering Information

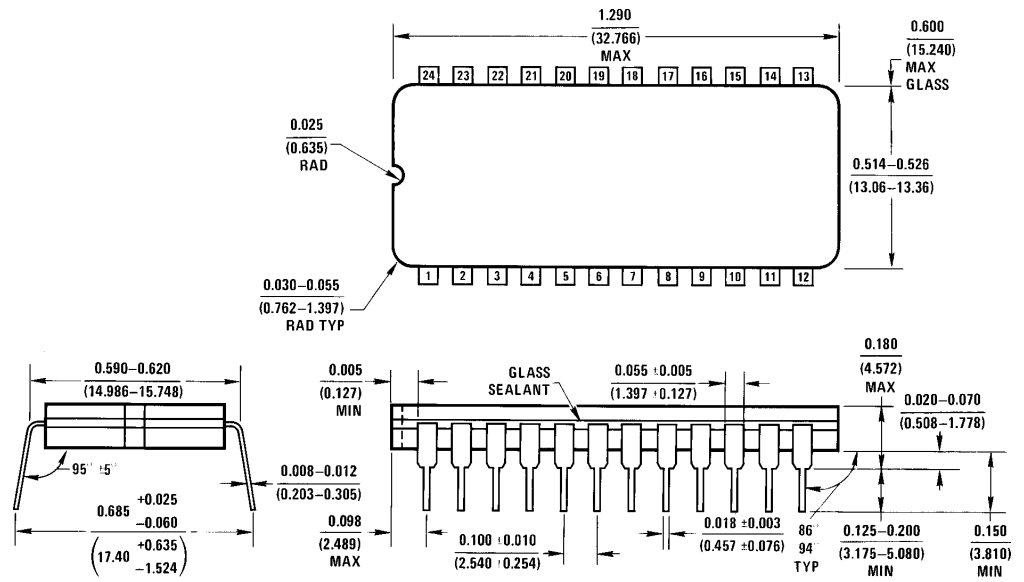
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

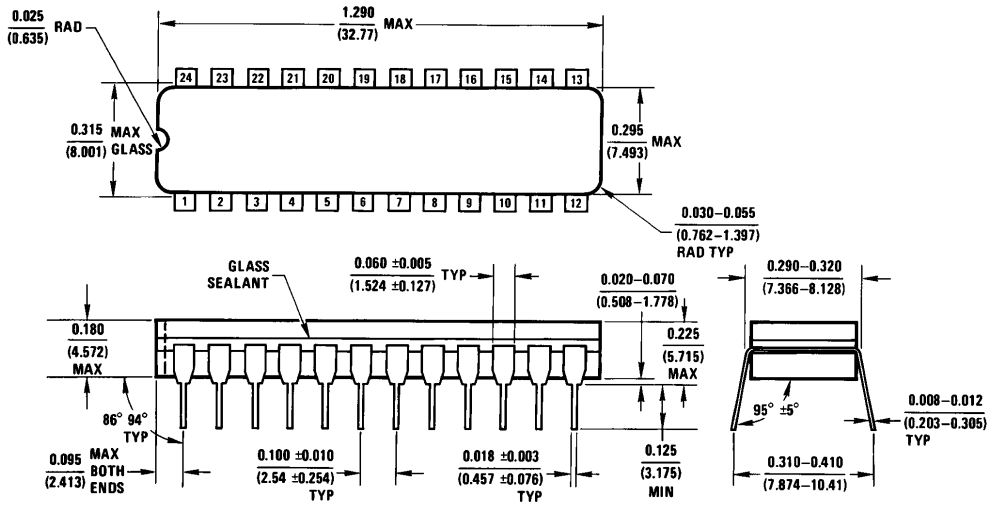


28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



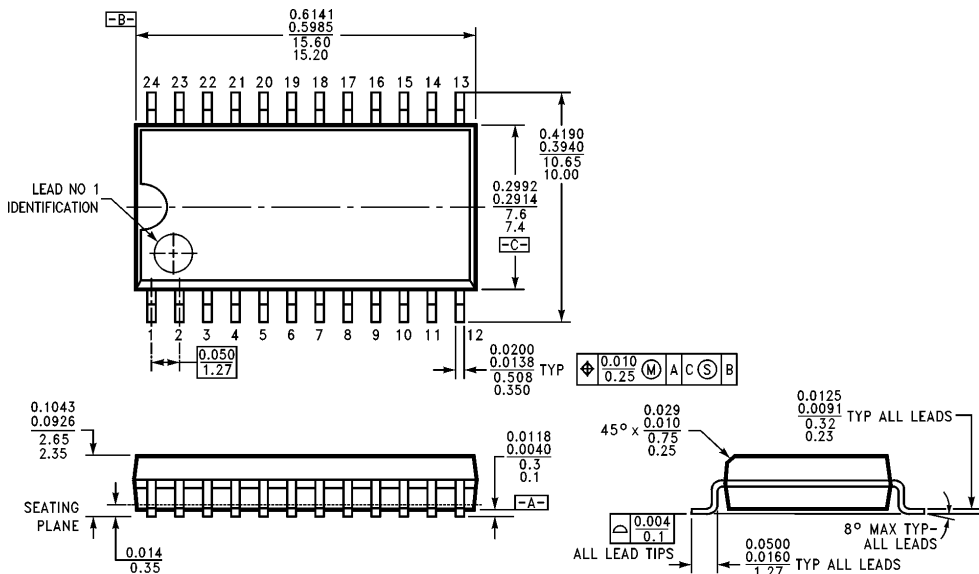
24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24A

Physical Dimensions inches (millimeters) (Continued)



24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
 NS Package Number J24F

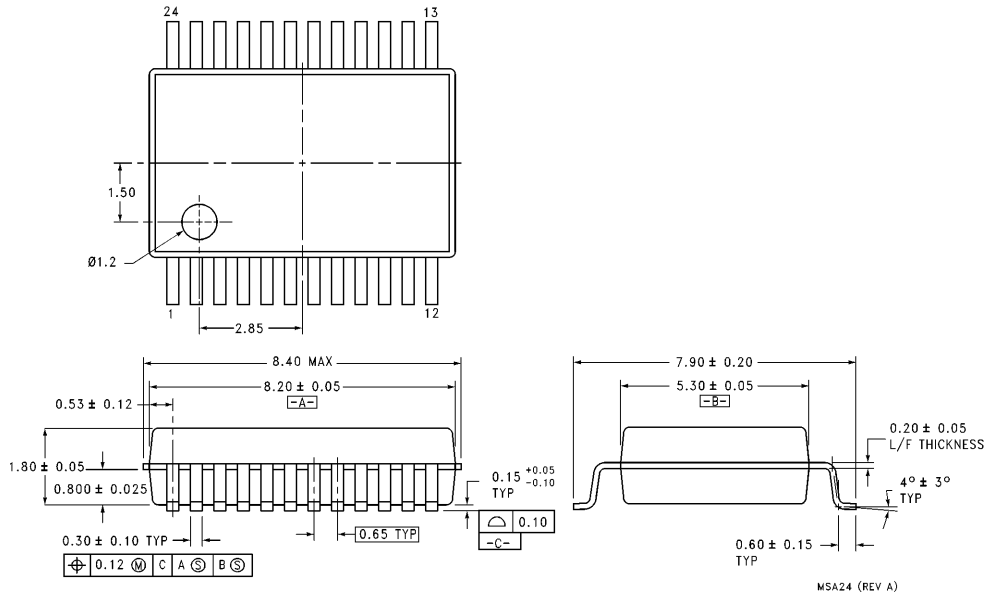
J24F (REV G)



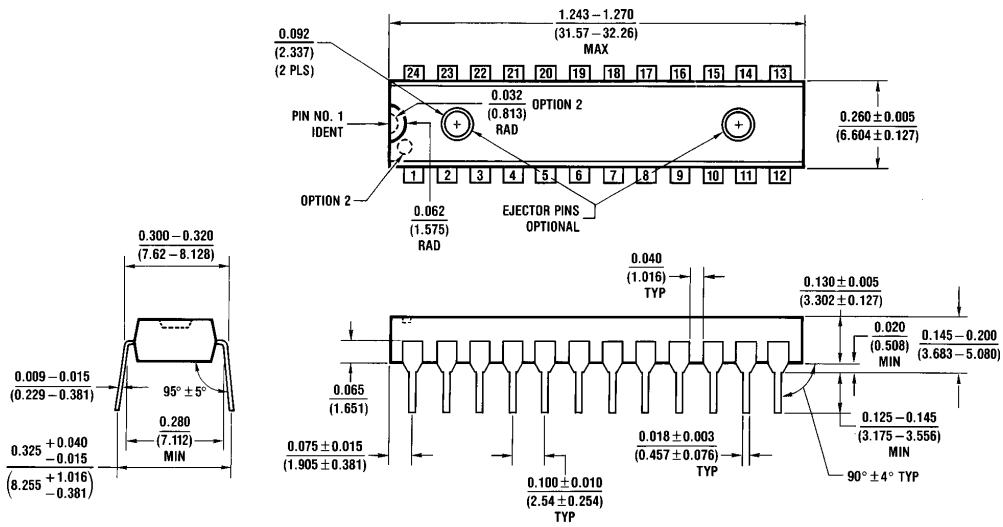
24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
 NS Package Number M24B

M24B (REV F)

Physical Dimensions inches (millimeters) (Continued)

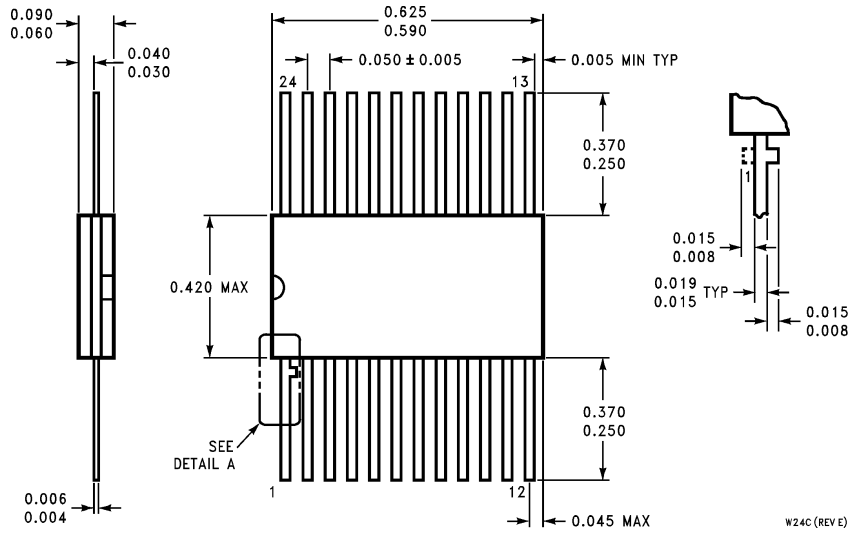


24-Lead Molded Shrink Small Outline, EIAJ, Type II (MSA)
NS Package Number MSA24



24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



**24-Lead Ceramic Flatpak (F)
NS Package Number W24C**

W24C (REV E)

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livny-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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