

DATA SHEET

74F676

16-bit serial/parallel-in, serial-out shift register (3-State)

Product specification

1989 Apr 18

IC15 Data Handbook

16-bit serial/parallel-in, serial-out shift register (3-State)

74F676

FEATURES

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Power supply current 48mA typical
- Shift frequency 110MHz typical
- Available in 300mil-wide 24-pin Slim DIP package

DESCRIPTION

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the mode (M) input is High, information present on the parallel data (D0–D15) inputs is entered on the falling edge of the clock pulse (\overline{CP}) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the serial (SI) input shifts into the least significant bit position. A High signal on the chip select (\overline{CS}) input prevents both parallel and serial operations.

The 16 bit shift register operates in one of three modes, as indicated in the shift register Function Table.

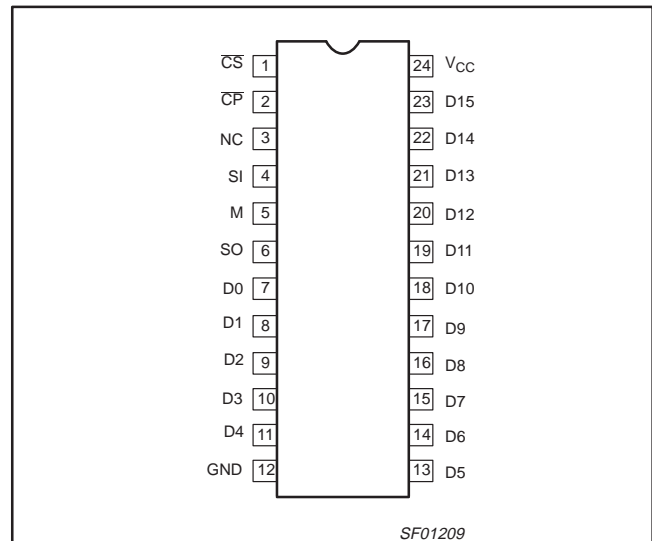
Hold: A High signal on the Chip Select (\overline{CS}) input prevents clocking and data is stored in the 16 registers.

Serial load: Data present on the SI pin shifts into the register on the falling edge of \overline{CP} . Data enters the Q0 position and shifts toward Q15 on successive clocks finally appearing on the SO pin.

Parallel load: Data present on D0–D15 is entered into the register on the falling edge of \overline{CP} . The SO output represents the Q15 register output.

To prevent false clocking, \overline{CP} must be Low during a Low-to-High transition of \overline{CS} .

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
24-Pin Plastic Slim DIP (300mil)	N74F676N	SOT222-1
24-Pin Plastic SOL	N74F676D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

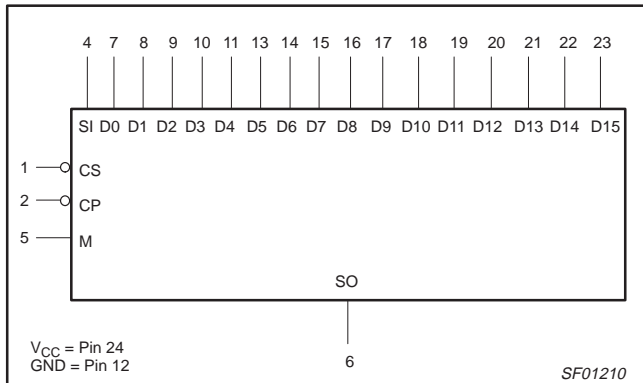
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D15	Parallel data inputs	1.0/1.0	20 μ A/0.6mA
SI	Serial data input	1.0/1.0	20 μ A/0.6mA
\overline{CS}	Chip Select input (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{CP}	Clock Pulse input (active falling edge)	1.0/1.0	20 μ A/0.6mA
M	Mode select input	1.0/1.0	20 μ A/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

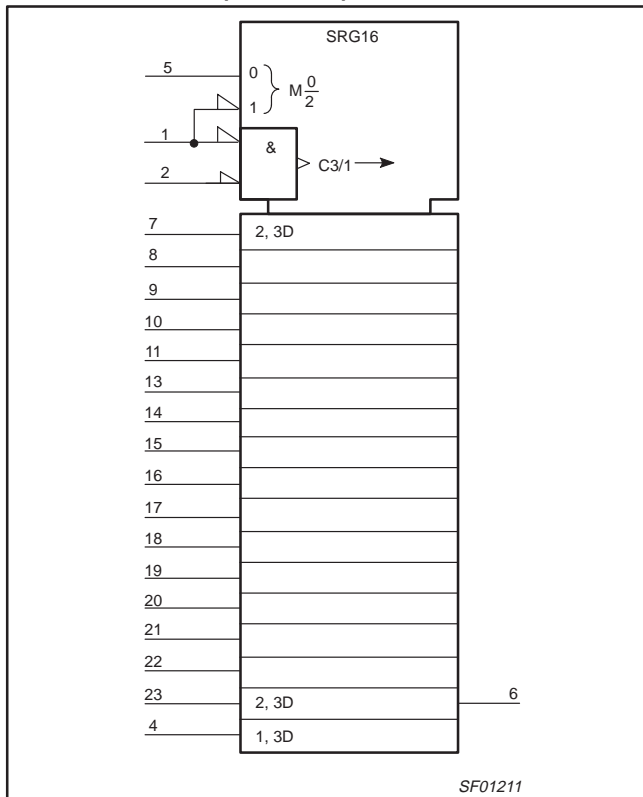
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

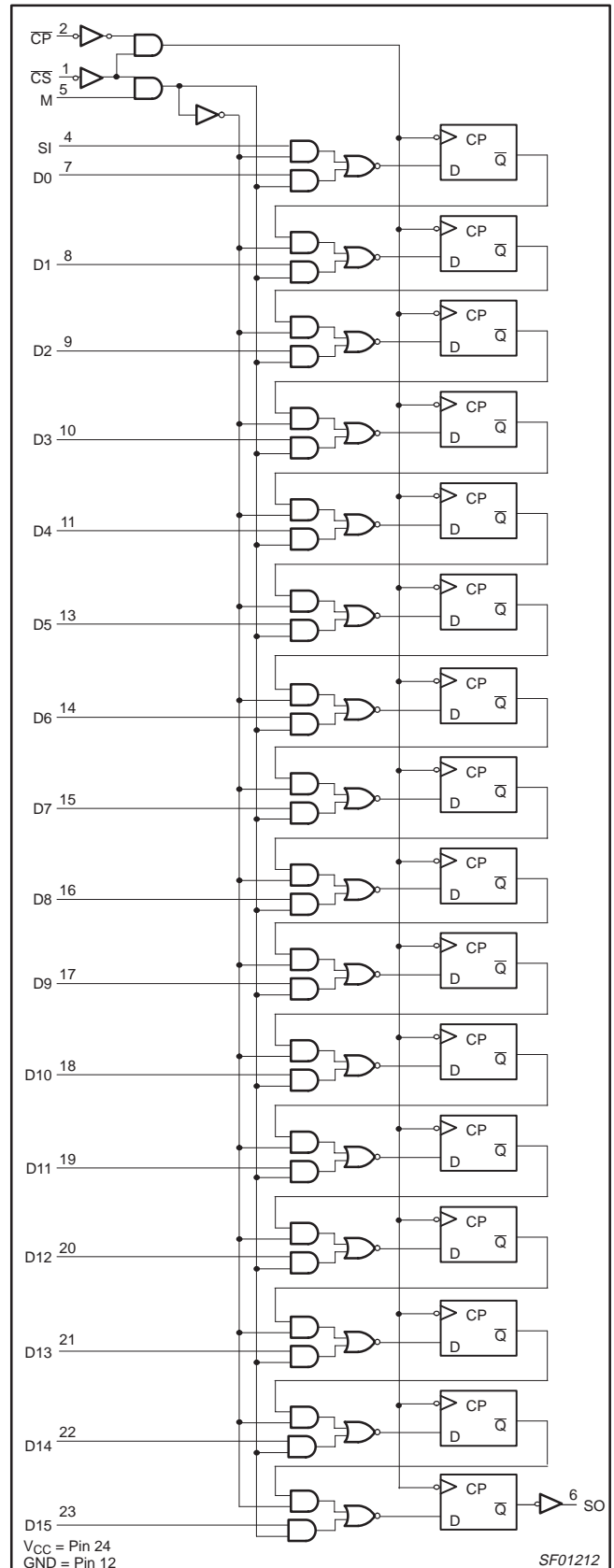


FUNCTION TABLE

CONTROL INPUTS			OPERATING MODE
CS	M	CP	
H	X	X	Hold
L	L	↓	Shift/Serial load
L	H	↓	Parallel load

H = High voltage level
 L = Low voltage level
 X = Don't care
 ↓ = High-to-Low transition of clock input

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ^{NO TAG}	LIMITS			UNIT	
			MIN	TYP NO TAG	MAX		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V	
			$\pm 5\%V_{CC}$	2.7	3.4	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.30	0.50	V
			$\pm 5\%V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
I_{OS}	Short-circuit output current ^{NO TAG}	$V_{CC} = \text{MAX}$	-60		-150	mA	
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$		48	72	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ C$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform NO TAG	100	110		90		MHz
t _{PLH} t _{PHL}	Propagation delay CP to SO	Waveform NO TAG	4.5 5.0	8.0 7.0	11.0 12.5	4.5 5.0	12.0 13.5	ns ns

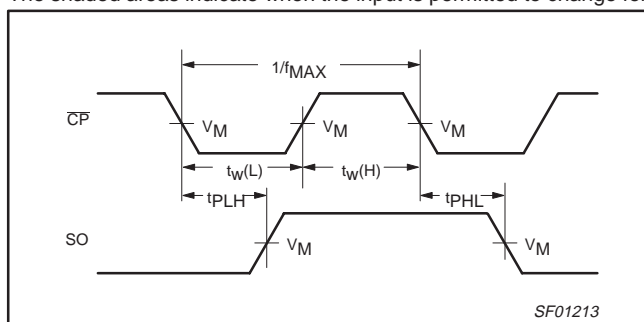
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low SI to CP	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low SI to CP	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t _s (H) t _s (L)	Setup time, High or Low Dn to CP	Waveform 2	3.0 3.0			3.0 3.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low Dn to CP	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t _s (H) t _s (L)	Setup time, High or Low M to CP	Waveform 2	8.0 8.0			8.0 8.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low M to CP	Waveform 2	2.0 2.0			2.0 2.0		ns ns
t _s (L)	Setup time, Low CS to CP	Waveform 2	10.0			10.0		ns
t _h (H)	Hold time, High CS to CP	Waveform 2	10.0			10.0		ns
t _w (H) t _w (L)	CP Pulse width, High or Low	Waveform NO TAG	4.0 6.0			4.0 6.0		ns ns

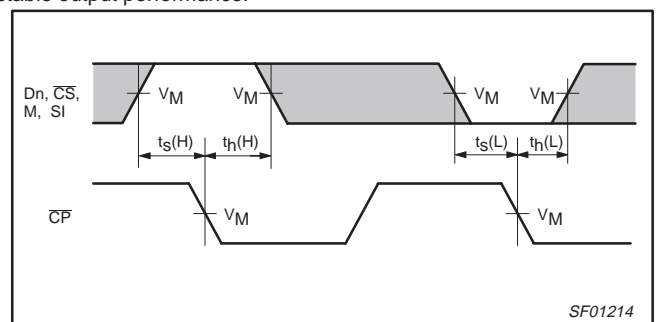
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

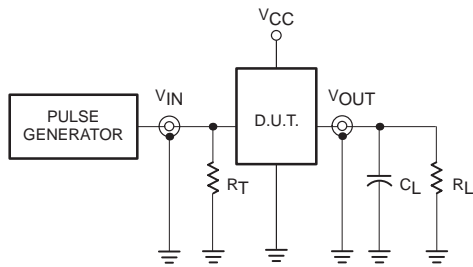


Waveform 2. Setup and Hold Times

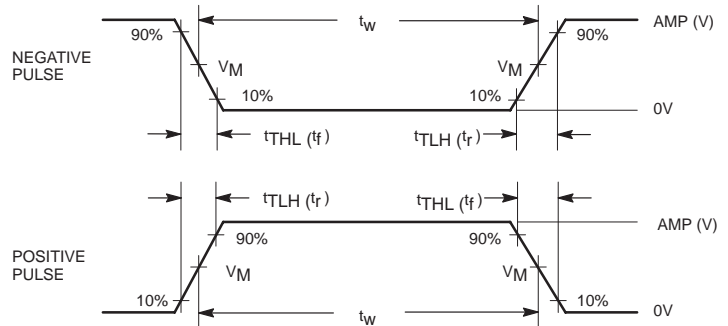
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TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

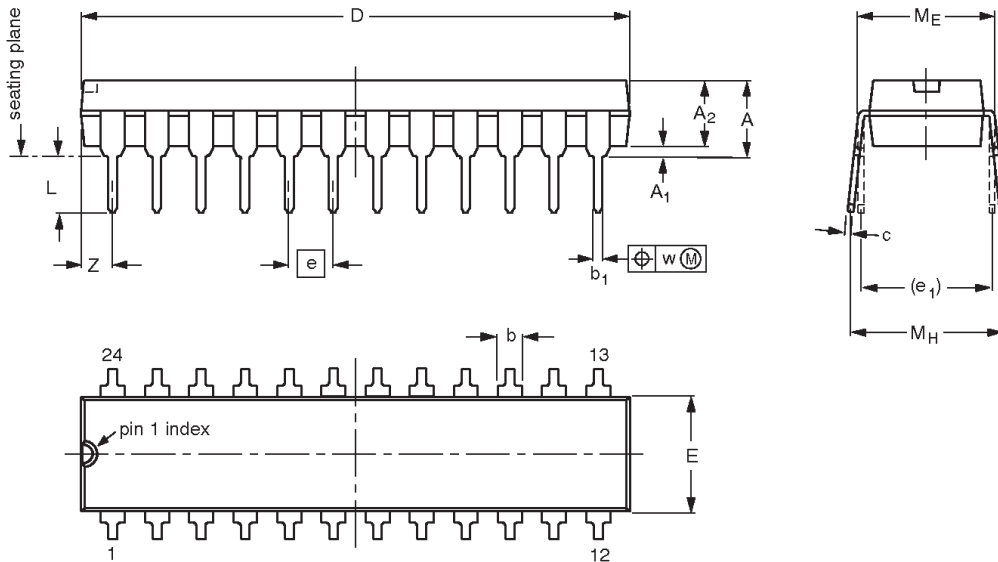
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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

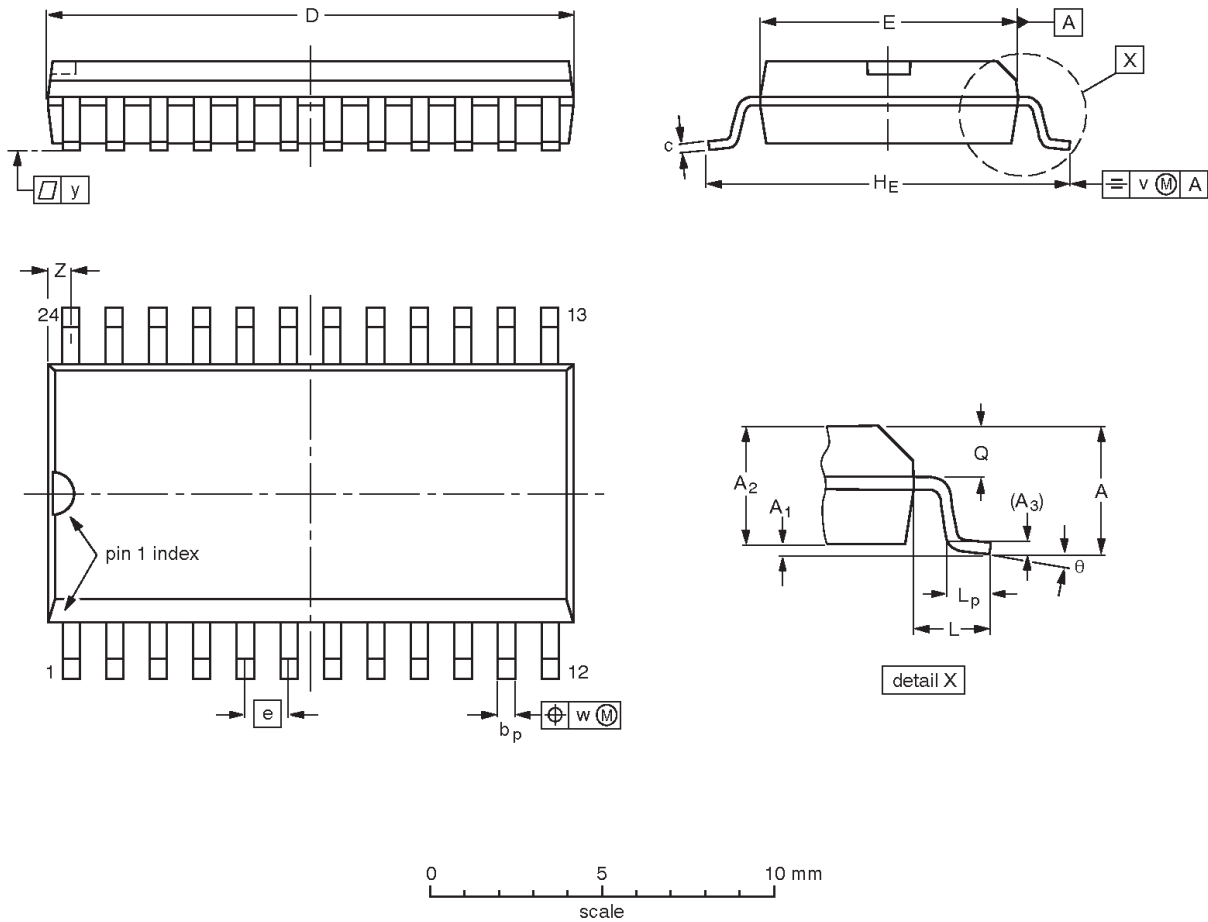
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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