

DATA SHEET

74F777

Triple bidirectional latched bus
transceiver (3-State + open collector)

Product specification

1992 May 19

IC15 Data Handbook

Triple bidirectional latched bus transceiver (3-State + Open Collector)

74F777

FEATURES

- Latching transceiver
- High drive Open Collector output current with minimum output swing
- Compatible with Test Mode (TM) bus specification
- Controlled output ramp
- Multiple package options
- Industrial temperature range available (-40°C to $+85^{\circ}\text{C}$)

DESCRIPTION

The 74F777 is a triple bidirectional latched bus transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristics impedance

range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with Open Collector B and 3-State A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC} .

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F777	7.0ns	45mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	
20-pin plastic DIP (300 mil)	N74F777N	I74F777N	SOT146-1
20-pin PLCC	N74F777A	I74F777A	SOT380-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	PNP latched inputs	3.5/0.117	70 μA /70 μA
B0 – B2	Data inputs with threshold circuitry	5.0/0.167	100 μA /100 μA
OEA0 – OEA2	A output enable inputs (active-High)	1.0/0.033	20 μA /20 μA
$\overline{\text{OEB0}} - \overline{\text{OEB2}}$	B output enable inputs (active-Low)	1.0/0.033	20 μA /20 μA
$\overline{\text{LE0}} - \overline{\text{LE2}}$	Latch enable inputs (active-Low)	1.0/0.033	20 μA /20 μA
A0 – A2	3-State outputs	150/40	3mA/24mA
B0 – B2	Open Collector outputs	OC/166.7	OC/100mA

Note to input and output loading and fan out table

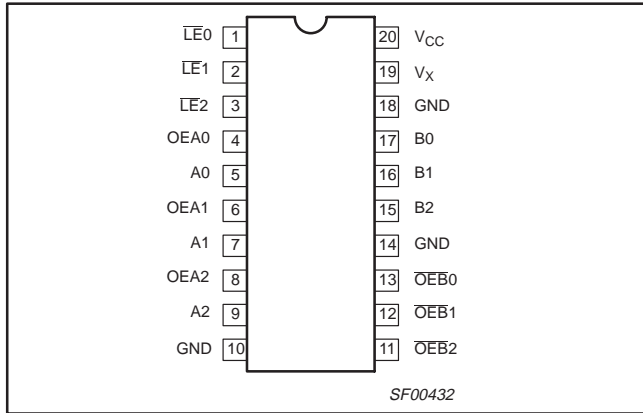
One (1.0) FAST unit load is defined as: 20 μA in the High state and 0.6mA in the Low state.

OC = Open Collector.

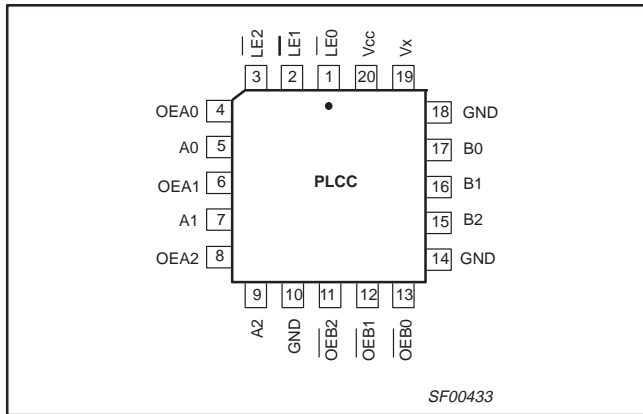
Triple bidirectional latched bus transceiver (3-State + Open Collector)

74F777

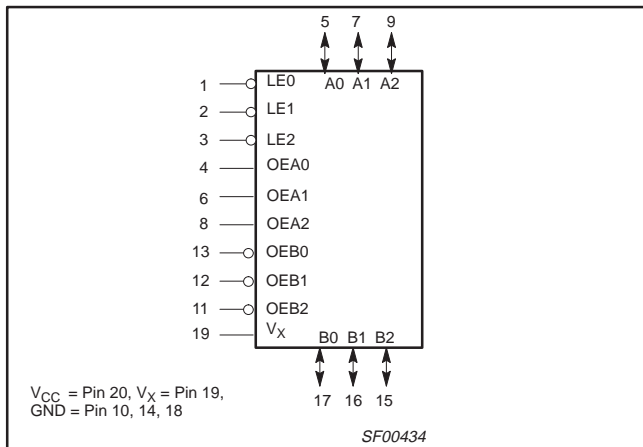
PIN CONFIGURATION



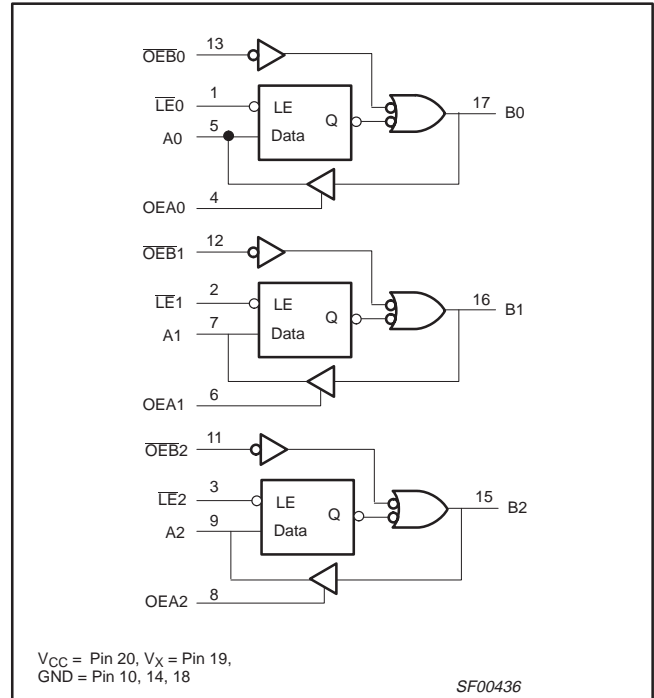
PIN CONFIGURATION PLCC



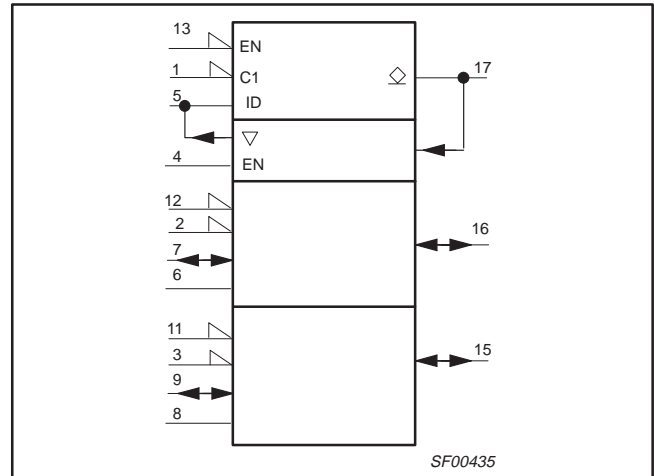
LOGIC SYMBOL



LOGIC DIAGRAM



IEC/IEEE SYMBOL



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74F777

FUNCTION TABLE

INPUTS					LATCH STATE	OUTPUTS		OPERATING MODE
An	Bn*	\overline{LEn}	OEA _n	\overline{OEBn}		An	Bn	
H	X	L	L	L	H	Z	H**	A 3-State, data from A to B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Q _n	Z	Q _n	A 3-State, latched data to B
–	–	L	H	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	H (2)	L	Z(2)	
–	–	H	H	L	Q _n	Q _n	Q _n	Latch state to A and B
H	X	L	L	H	H	Z	Z	B and A 3-State
L	X	L	L	H	L	Z	Z	
X	X	H	L	H	Q _n	Z	Z	
–	H	L	H	H	H	H	Z	B 3-State, data from B to A
–	L	L	H	H	L	L	Z	
–	H	H	H	H	Q _n	H	Z	
–	L	H	H	H	Q _n	L	Z	

Notes to function table

H = High voltage level

L = Low voltage level

X = Don't care

– = Input not externally driven

Z = High impedance (off) state

Q_n = High or Low voltage level one setup time prior to the Low-to-High \overline{LE} transition.

(1) = Condition will cause a feedback loop path: A to B and B to A.

(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB0}$ and $\overline{OEB1}$ are Low and \overline{LE} is High.B_n* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.

H** = Goes to level of pull-up voltage.

Each latch is independent. The latches may be run in any combination of modes.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	–0.5 to +7.0	V
V _X	Threshold control	–0.5 to +7.0	V
V _{IN}	Input voltage	\overline{OEBn} , OEA _n , \overline{LEn}	–0.5 to +7.0
		A0 – A2, B0 – B2	–0.5 to +5.5
I _{IN}	Input current	–30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	–0.5 to V _{CC}	V
I _{OUT}	Current applied to output in	A0 – A2	48
	Low output state	B0 – B2	200
T _{amb}	Operating free air temperature range	Commercial range	0 to +70
		Industrial range	–40 to +85
T _{stg}	Storage temperature range	–65 to +150	°C

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74F777

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5.0	5.5	V
V _{IH}	High-level input voltage	Except B0 – B2	2.0			V
		B0 – B2	1.6			V
V _{IL}	Low-level input voltage	Except B0 – B2			0.8	V
		B0 – B2			1.43	V
I _{Ik}	Input clamp current	Except A0 – A2			-18	mA
		A0 – A2			-40	mA
I _{OH}	High-level output current	Except A0 – A2			-3	mA
I _{OL}	Low-level output current	A0 – A2			24	mA
		B0 – B2			100	mA
T _{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	-40		+85	°C

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74F777

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT
				MIN	TYP ²	MAX	
I_{OH}	High-level output current	B0 – B2	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA
I_{OFF}	Power-off output current	B0 – B2	$V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA
V_{OH}	High-level output voltage	A0 – A2 ⁴	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OH} = -3\text{mA}, V_X = V_{CC}$	2.5	V_{CC}	V
				$I_{OH} = -4\text{mA}, V_X = 3.13\text{V}$ and 3.47V	2.5	V_X	V
V_{OL}	Low-level output voltage	A0 – A2 ⁴	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OL} = 20\text{mA}, V_X = V_{CC}$		0.50	V
		B0 – B2		$I_{OL} = 100\text{mA}$		1.15	V
				$I_{OL} = 4\text{mA}$	0.40		V
V_{IK}	Input clamp voltage	A0 – A2	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.5	V
		Except A0 – A2	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.2	V
I_I	Input current at maximum input voltage	$\overline{\text{OEBn}}, \text{OEAn}, \text{LEn}$	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	μA
		A0 – A2, B0 – B2	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1	mA
I_{IH}	High-level input current	$\overline{\text{OEBn}}, \text{OEAn}, \text{LEn}$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}, B_n - A_n = 0\text{V}$			20	μA
		B0 – B2	$V_{CC} = \text{MAX}, V_I = 2.1\text{V}$			100	μA
I_{IL}	Low-level input current	$\overline{\text{OEBn}}, \text{OEAn}, \text{LEn}$	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-20	μA
		B0 – B2	$V_{CC} = \text{MAX}, V_I = 0.3\text{V}$			-100	μA
$I_{OZH} + I_{IH}$	Off-state output current, High level voltage applied	A0 – A2	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$			70	μA
$I_{OZL} + I_{IL}$	Off-state output current, Low level voltage applied	A0 – A2	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-70	μA
I_X	High level control current		$V_{CC} = \text{MAX}, V_X = V_{CC}, \text{LE} = \text{OEAn} = \overline{\text{OEBn}} = 2.7\text{V}, A0 - A2 = 2.7\text{V}, B0 - B2 = 2.0\text{V},$	-100		100	μA
			$V_{CC} = \text{MAX}, V_X = 3.13 \text{ \& } 3.47\text{V}, \text{LE} = \text{OEAn} = 2.7\text{V}, \overline{\text{OEBn}} = A0 - A2 = 2.7\text{V}, B0 - B2 = 2.0\text{V}$	-10		10	μA
I_{OS}	Short circuit output current ³	A0 – A2 only	$V_{CC} = \text{MAX}, B_n = 1.8\text{V}, \text{OEAn} = 2.0\text{V}, \overline{\text{OEBn}} = 2.7\text{V}$	-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		40	60	mA
		I_{CCL}	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		55	80	mA
		I_{CCZ}	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		45	67	mA

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, $V_X = V_{CC}$ for all test condition.
- All typical values are at $V_{CC} = 5\text{V}, T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Due to test equipment limitations, actual test conditions are for $V_{IH} = 1.8\text{V}$ and $V_{IL} = 1.3\text{V}$.

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74F777

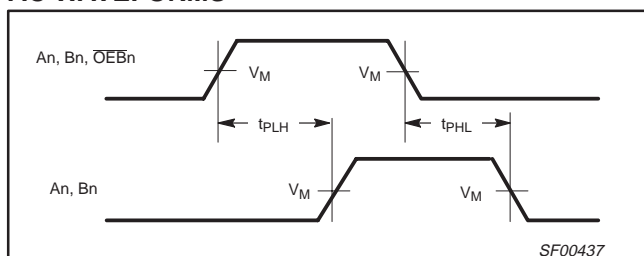
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS								UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 30pF, R _L = 9Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ±10% C _L = 30pF, R _L = 9Ω		T _{amb} = -40°C to +85°C V _{CC} = +5.0V ±10% C _L = 30pF, R _L = 9Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay Bn to An	Waveform 1	8.5 7.5	10.5 9.5	13.0 12.0	8.0 7.5	14.5 12.5	8.0 7.5	14.5 12.5	ns	
t _{PZH} t _{PZL}	Output enable time to High or Low OEAn to An	Waveform 3, 4	8.0 9.0	10.0 11.0	13.0 14.0	7.0 8.0	14.5 15.5	7.0 8.0	14.5 15.5	ns	
t _{PHZ} t _{PLZ}	Output Disable time from High or Low OEAn to An	Waveform 3, 4	1.5 1.5	3.0 3.0	6.0 6.0	1.0 1.0	6.5 6.0	1.0 1.0	6.5 6.0	ns	
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS								UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _D = 30pF, R _U = 9Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _D = 30pF, R _U = 9Ω		T _{amb} = -40°C to +85°C V _{CC} = +5.0V ±10% C _D = 30pF, R _U = 9Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay An to Bn	Waveform 1	3.0 5.0	4.5 6.5	7.0 9.0	2.5 4.5	8.0 10.0	2.5 4.5	8.0 10.0	ns	
t _{PLH} t _{PHL}	Propagation delay LEn to Bn	Waveform 1	3.5 5.5	5.5 7.5	8.0 10.5	3.0 5.0	9.0 11.5	3.0 5.0	9.0 11.5	ns	
t _{PLH} t _{PHL}	Enable/disable time OEBn to An	Waveform 1	3.0 6.0	5.0 8.0	7.5 10.5	3.0 5.5	8.0 12.0	3.0 5.5	8.0 12.0	ns	
t _{TLH} t _{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuits and Waveforms	0.5 0.5	4.0 2.0	4.5 4.5	0.5 0.5	7.0 4.5	0.5 0.5	7.0 4.5	ns	

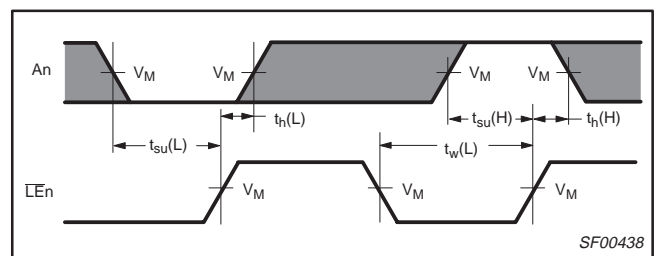
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _D = 30pF, R _U = 9Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _D = 30pF, R _U = 9Ω		T _{amb} = -40°C to +85°C V _{CC} = +5.0V ±10% C _D = 30pF, R _U = 9Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{su} (H) t _{su} (L)	Setup time An to LEn	Waveform 2	4.0 4.5			4.5 4.5			4.5 4.5	ns	
t _h (H) t _h (L)	Hold time An to LEn	Waveform 2	0.0 0.0			0.0 0.0			0.0 0.0	ns	
t _w (L)	LEn pulse width, Low	Waveform 2	5.5			6.5			6.5	ns	

AC WAVEFORMS



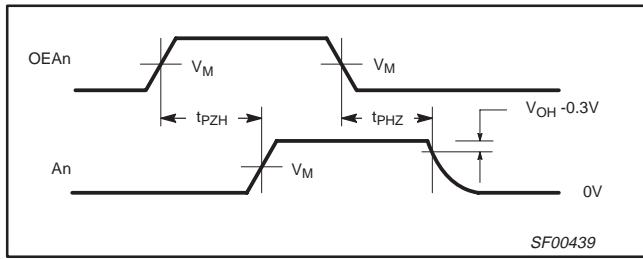
Waveform 1. Propagation delay, data to output and enable/disable time OEBn to Bn



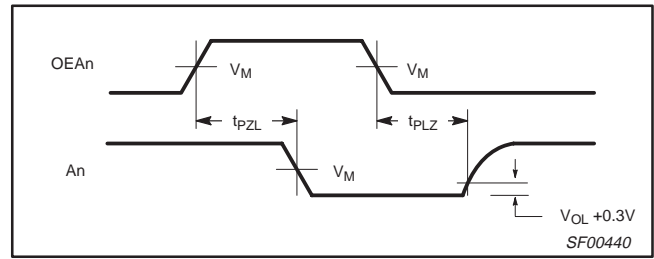
Waveform 2. Data set-up and hold times and LEn pulse width

Triple bidirectional latched bus transceiver (3-State + Open Collector)

74F777



Waveform 3. 3-State output enable time to High level and output disable time from High level



Waveform 4. 3-State output enable time to Low level and output disable time from Low level

Notes to AC waveforms

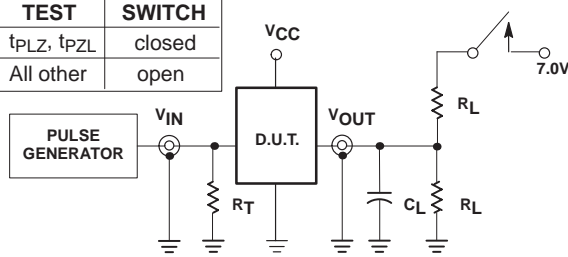
For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

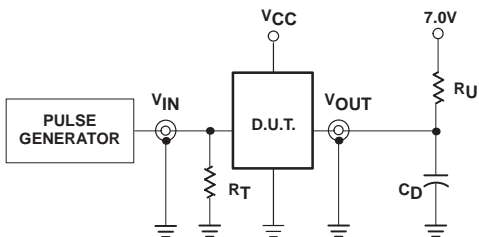
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

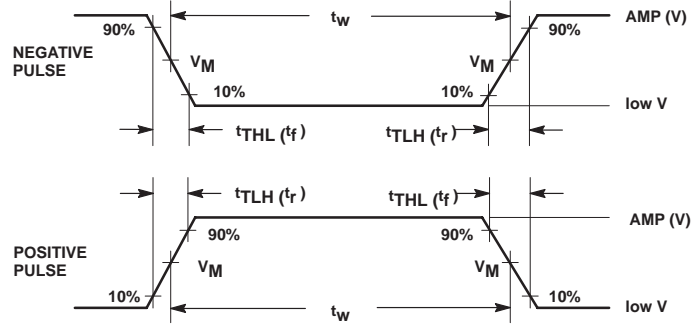
TEST	SWITCH
t_{PLZ} , t_{PZL}	closed
All other	open



Test circuit for 3-State outputs on A port



Test circuit for outputs on B port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	2.0V	1.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_U = Pull up resistor; see AC electrical characteristics for value.

C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

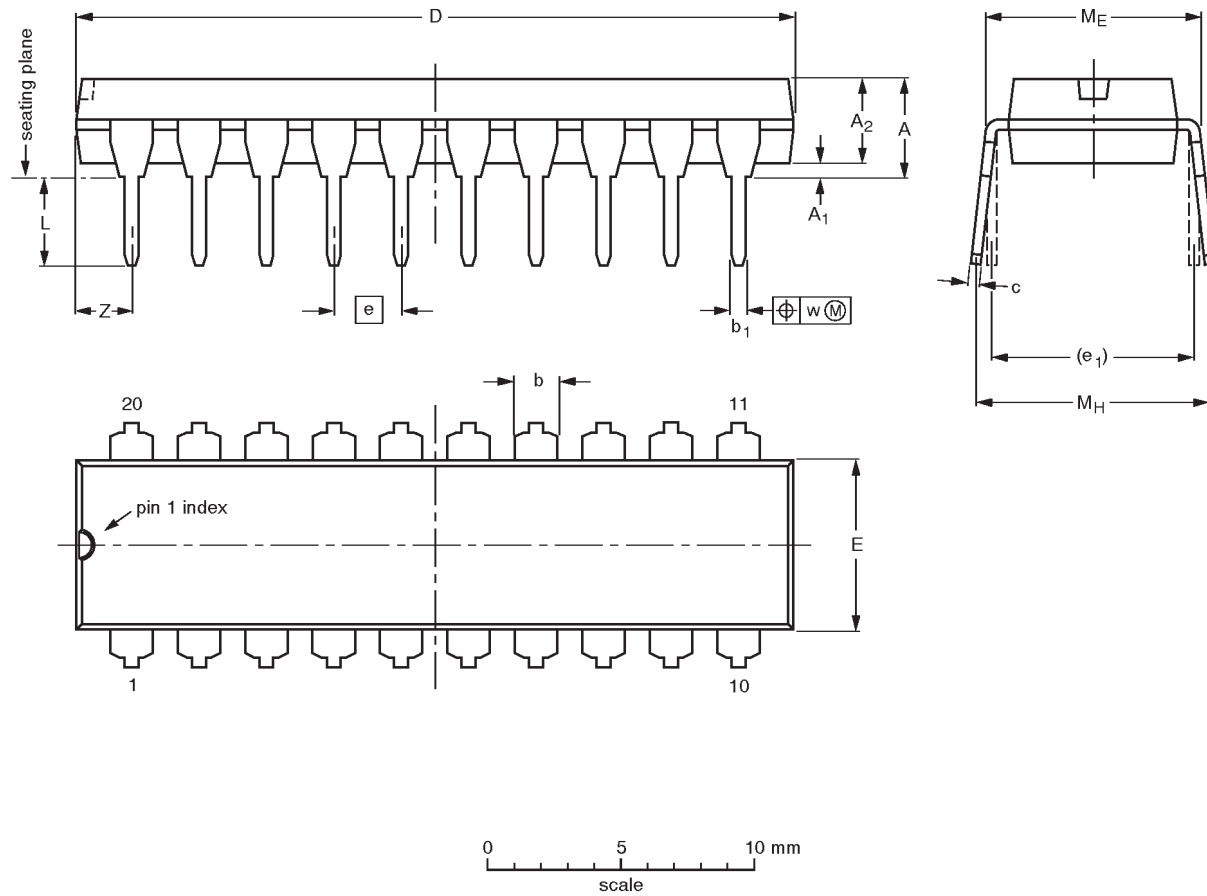
SF00431

Triple bidirectional latched bus transceiver (3-State + open collector)

74F777

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

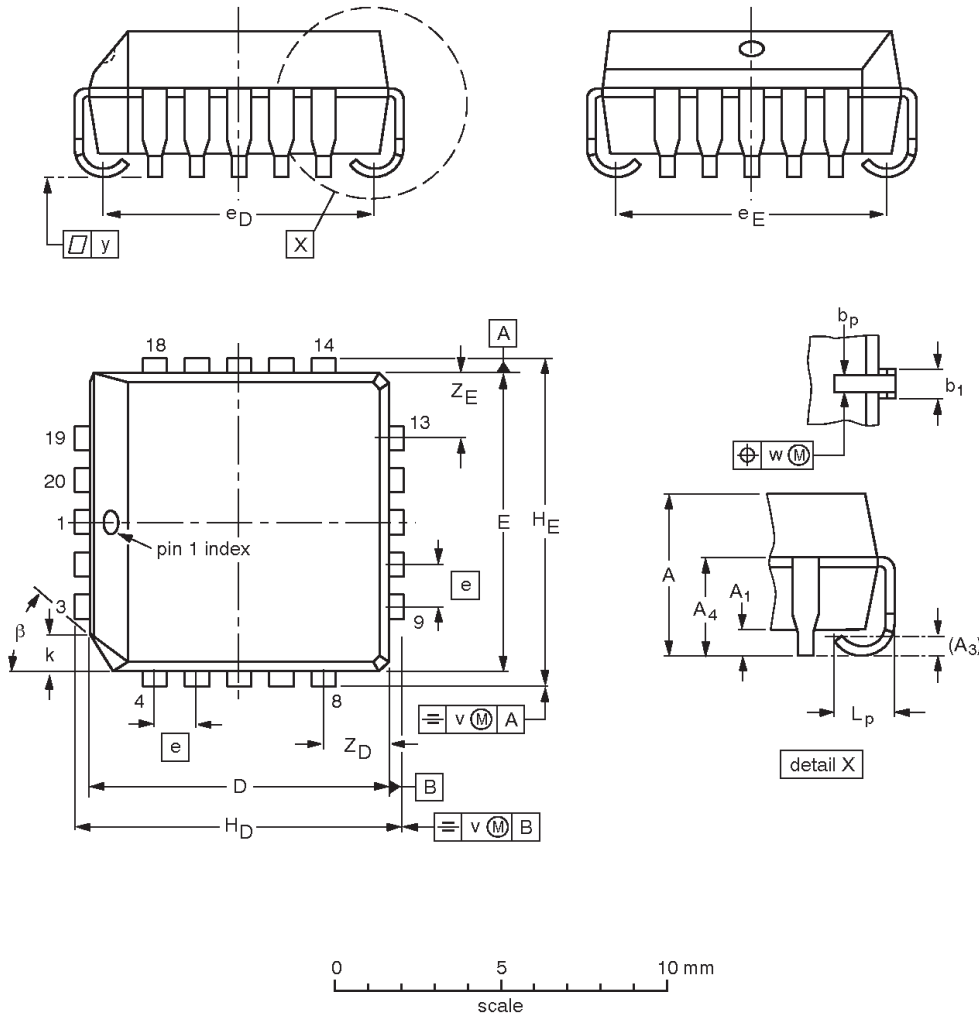
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Triple bidirectional latched bus transceiver (3-State + open collector)

74F777

PLCC20: plastic leaded chip carrier; 20 leads

SOT380-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT380-1		MO-047AA			95-02-25 97-12-16

Triple bidirectional latched bus transceiver
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74F777

NOTES

Triple bidirectional latched bus transceiver (3-State + open collector)

74F777

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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