

74F821

10-Bit D-Type Flip-Flop

General Description

The 74F821 is a 10-bit D-type flip-flop with 3-STATE true outputs arranged in a broadside pinout.

Features

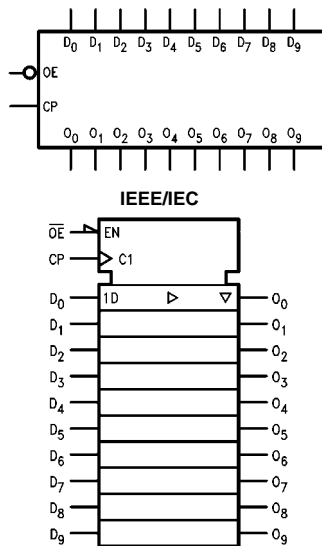
- 3-STATE Outputs

Ordering Code:

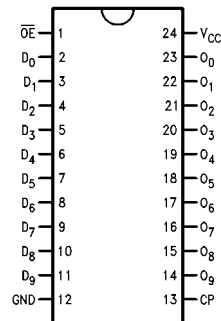
Order Number	Package Number	Package Description
74F821SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F821SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 – D_9	Data Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{OE}	Output Enable 3-STATE Input	1.0/1.0	20 μ A/–0.6 mA
CP	Clock Input	1.0/1.0	20 μ A/–0.6 mA
O_0 – O_9	3-STATE Outputs	150/40 (33.3)	–3.0 mA/24 mA (20 mA)

Functional Description

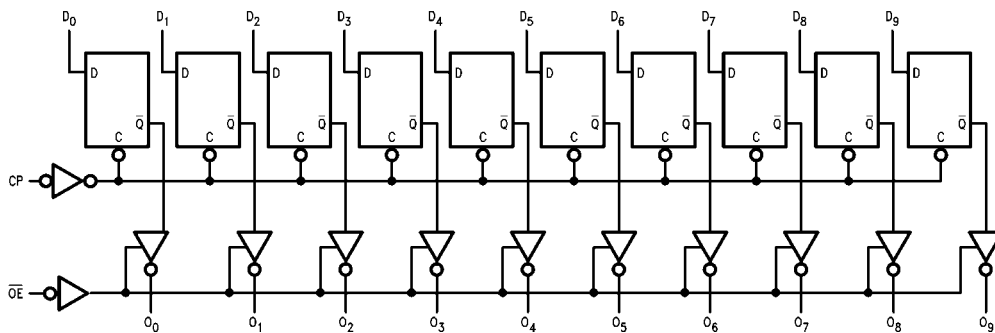
The 74F821 consists of ten D-type edge-triggered flip-flops. This device has 3-STATE true outputs for bus systems organized in a broside pinning. The buffered Clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the \overline{OE} LOW the content of the flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Output	Function
\overline{OE}	CP	D	\overline{Q}	O	
H	H	X	NC	Z	Hold
H	L	X	NC	Z	Hold
H	\nearrow	L	H	Z	Load
H	\nearrow	H	L	Z	Load
L	\nearrow	L	H	L	Data Available
L	\nearrow	H	L	H	Data Available
L	H	X	NC	NC	No Change in Data
L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
 \nearrow = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCZ}	Power Supply Current		78	100	mA	Max	V _O = HIGH Z

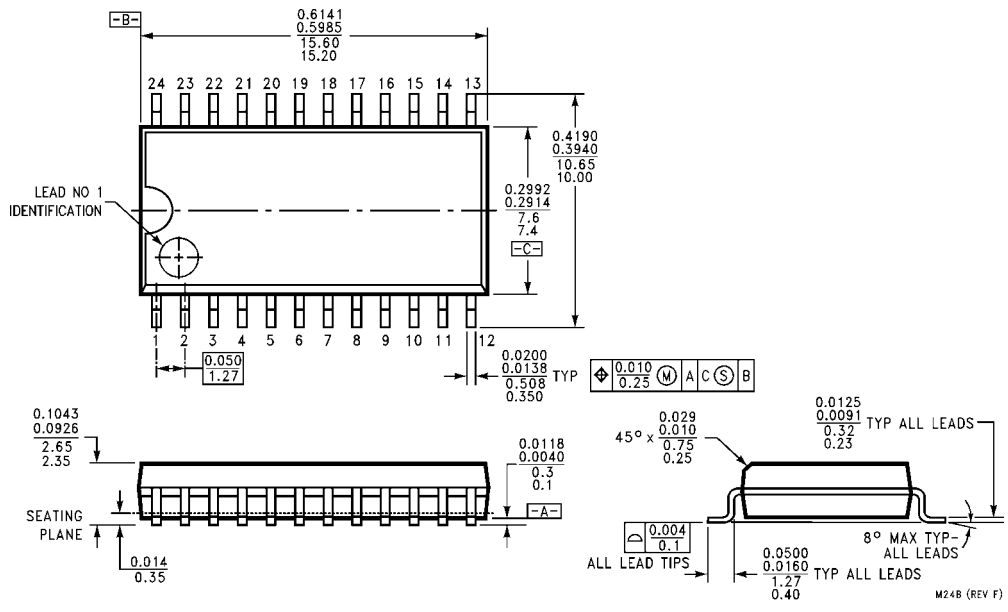
AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	150		60		70		MHz
t _{PLH}	Propagation Delay	2.0	6.4	9.5	2.0	10.5	2.0	10.5	ns
t _{PHL}	CP to O _n	2.0	6.2	9.5	2.0	10.5	2.0	10.5	
t _{PZH}	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns
t _{PZL}	$\overline{\text{OE}}$ to O _n	2.0	6.3	10.5	2.0	13.0	2.0	11.5	
t _{PHZ}	Output Disable Time	1.5	3.4	7.0	1.0	7.5	1.5	7.5	
t _{PLZ}	$\overline{\text{OE}}$ to O _n	1.5	3.5	7.0	1.0	7.5	1.5	7.5	

AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
t _S (L)	D _n to CP	2.5		4.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns
t _H (L)	D _n to CP	2.5		2.5		2.5		
t _W (H)	CP Pulse Width	5.0		6.0		6.0		ns
t _W (L)	HIGH or LOW	5.0		6.0		6.0		

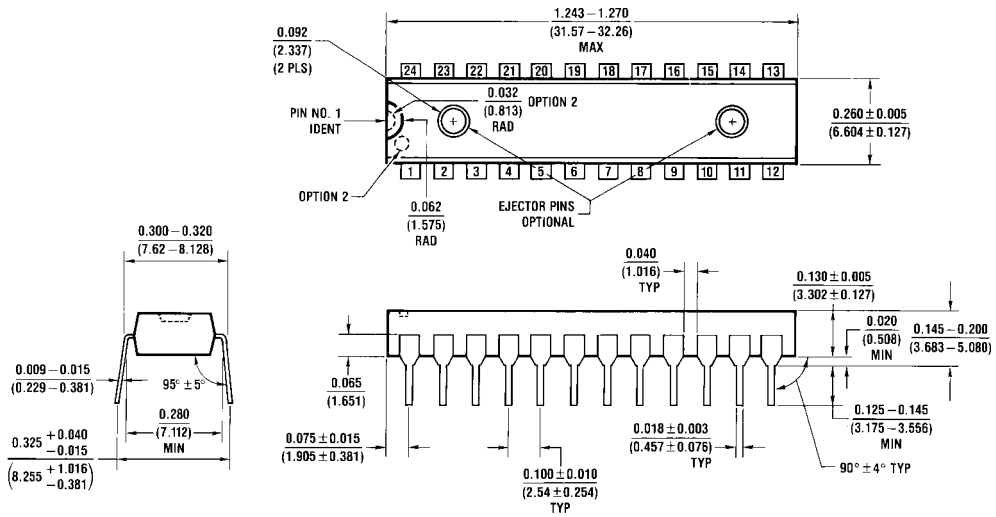
Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

M24B (REV F)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide Package Number N24C

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