

DATA SHEET

74F821/822/823/824/825/826 Bus interface registers

Product specification

1996 Jan 05

IC15 Data Handbook

Bus interface registers

74F821/822/823/824/825/826

- 74F821 10-bit bus interface register, non-inverting (3-State)
 74F822 10-bit bus interface register, inverting (3-State)
 74F823 9-bit bus interface register, non-inverting (3-State)
 74F824 9-bit bus interface register, inverting (3-State)
 74F825 8-bit bus interface register, non-inverting (3-State)
 74F826 8-bit bus interface register, inverting (3-State)

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- High performance bus interface buffering for wide data/address paths or busses carrying parity
- High impedance PNP base inputs for reduced loading (20 μ A in high and low states)
- I_{IL} is 20 μ A vs 1000 μ A for AM29821 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessor
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29821-29826 series
- Outputs sink 64mA and source 24mA
- Industrial temperature range available (-40°C to +85°C) for 74F823

DESCRIPTION

The 74F821 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 74F821/74F822 are buffered 10-bit wide versions of the popular 74F374/74F534 functions.

The 74F822 is the inverted output version of 74F821.

The 74F823 and 74F824 are 9-bit wide buffered registers with clock enable (\overline{CE}) and master reset (\overline{MR}) which are ideal for parity bus interfacing in high microprogrammed systems.

The 74F824 is the inverted version of 74F823.

The 74F825 and 74F826 are 8-bit buffered registers with all the 74F823/74F824 controls plus output enable ($\overline{OE0}$, $\overline{OE1}$, $\overline{OE2}$) to allow multiuser control of the interface, e.g., \overline{CS} , DMA, and RD/ \overline{WR} . They are ideal for uses as an output port requiring high I_{OL}/I_{OH} .

The 74F826 is the inverted version of 74F825.

| TYPE | TYPICAL f_{max} | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------------|----------------------|--------------------------------------|
| 74F821, 74F822 | 180MHz | 75mA |
| 74F823, 74F824 | 180MHz | 70mA |
| 74F825, 74F826 | 180MHz | 65mA |

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | | PKG. DWG. # |
|----------------------------------|--|--|-------------|
| | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C$ to $+70^\circ C$ | INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^\circ C$ to $+85^\circ C$ | |
| 24-pin plastic slim DIP (300mil) | N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N | I74F823N | SOT222-1 |
| 24-pin plastic SOL | N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D | I74F823D | SOT137-1 |

Bus interface registers

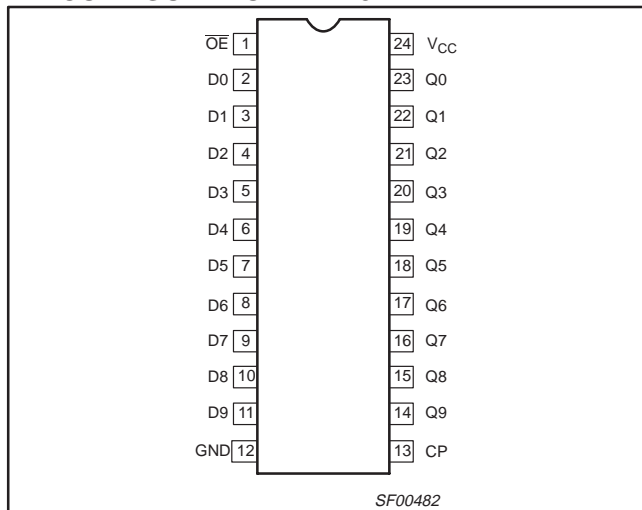
74F821/822/823/824/825/826

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

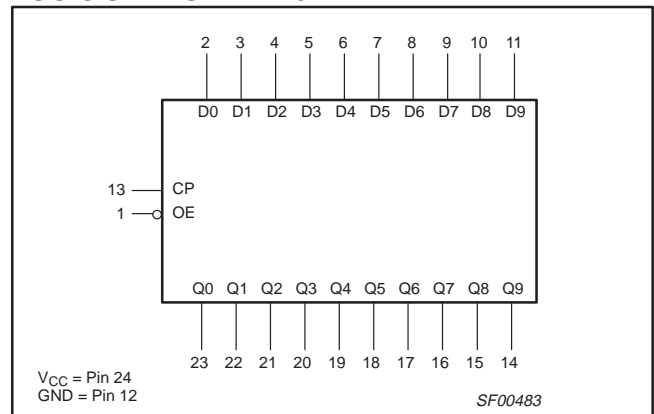
| PINS | | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|------------------|---------------------|----------------------------------|---------------------|---------------------|
| 74F821 74F822 | Dn | Data inputs | 1.0/1.0 | 20µA/0.6mA |
| | CP | Clock input | 1.0/1.0 | 20µA/0.6mA |
| | \overline{OE} | Output enable input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | Qn, \overline{Qn} | Data outputs | 1200/106.7 | 24mA/64mA |
| 74F823 74F824 | Dn | Data inputs | 1.0/1.0 | 20µA/0.6mA |
| | CP | Clock input | 1.0/1.0 | 20µA/0.6mA |
| | \overline{CE} | Clock enable input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | \overline{MR} | Master reset input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | \overline{OE} | Output enable input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | Qn, \overline{Qn} | Data outputs | 1200/106.7 | 24mA/64mA |
| 74F825 74F826 | Dn | Data inputs | 1.0/1.0 | 20µA/0.6mA |
| | CP | Clock input | 1.0/1.0 | 20µA/0.6mA |
| | \overline{CE} | Clock enable input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | \overline{MR} | Master reset input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | \overline{OE} | Output enable input (active low) | 1.0/3.0 | 20µA/1.8mA |
| | Qn, \overline{Qn} | Data outputs | 1200/106.7 | 24mA/64mA |

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION – 74F821



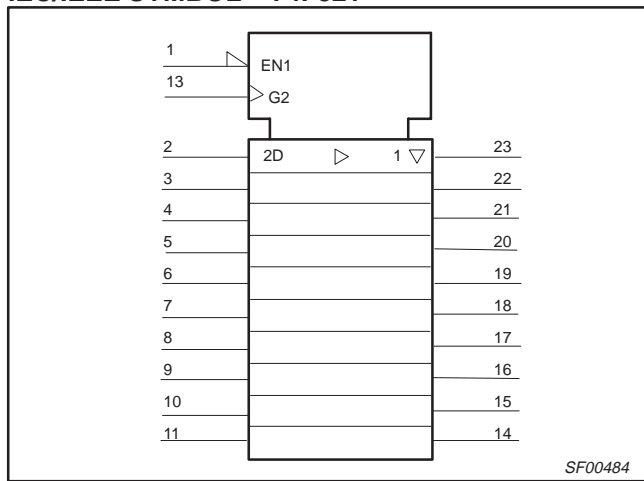
LOGIC SYMBOL – 74F821



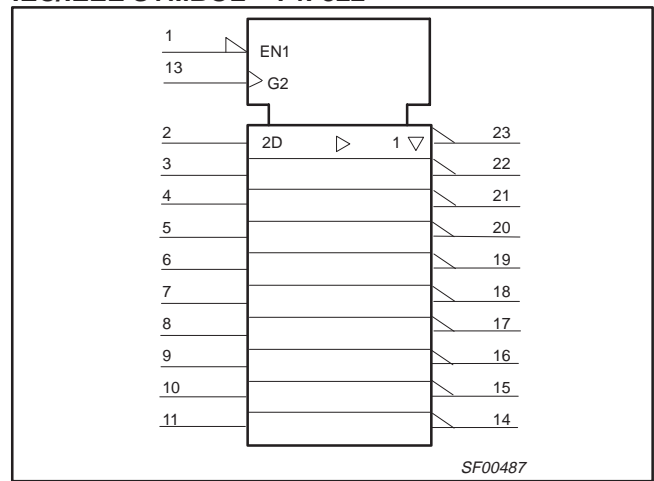
Bus interface registers

74F821/822/823/824/825/826

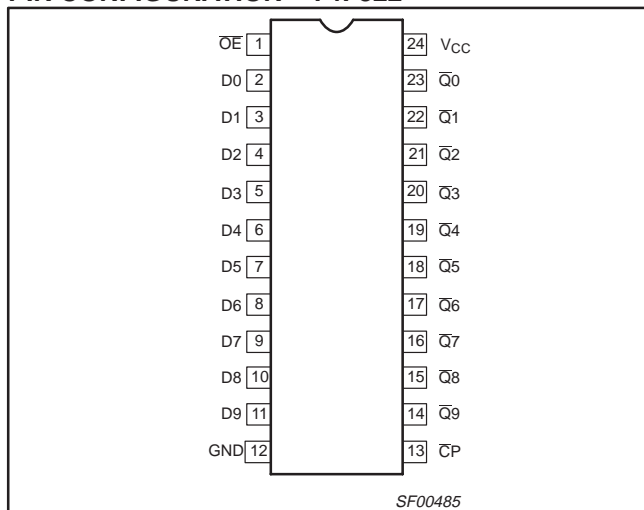
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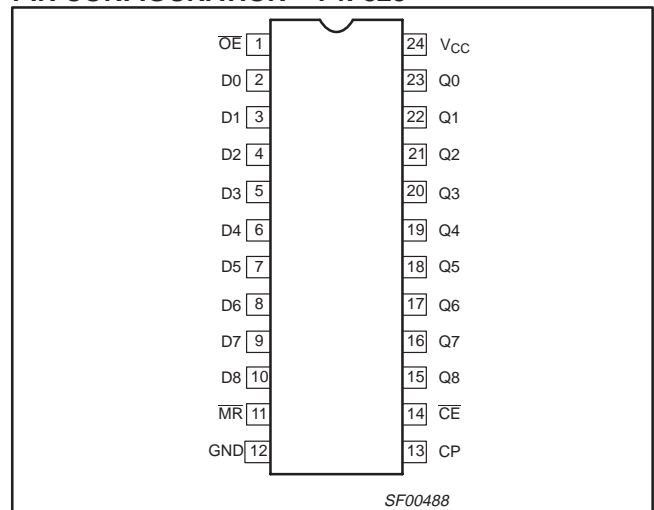
IEC/IEEE SYMBOL – 74F822



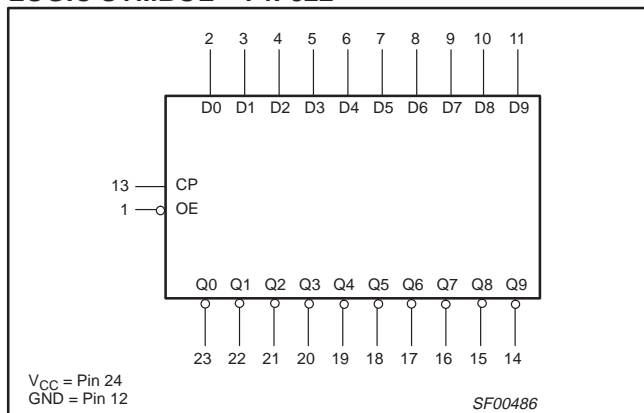
PIN CONFIGURATION – 74F822



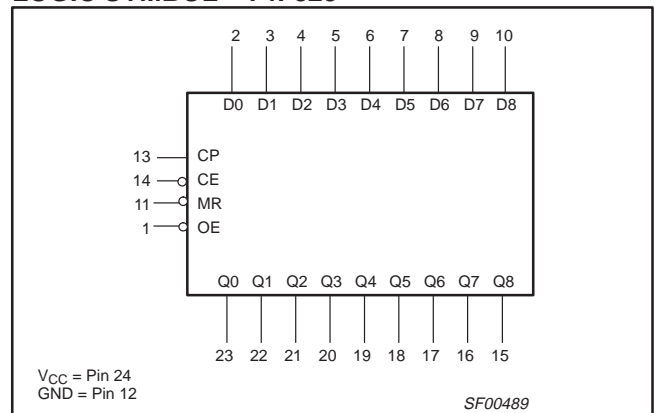
PIN CONFIGURATION – 74F823



LOGIC SYMBOL – 74F822



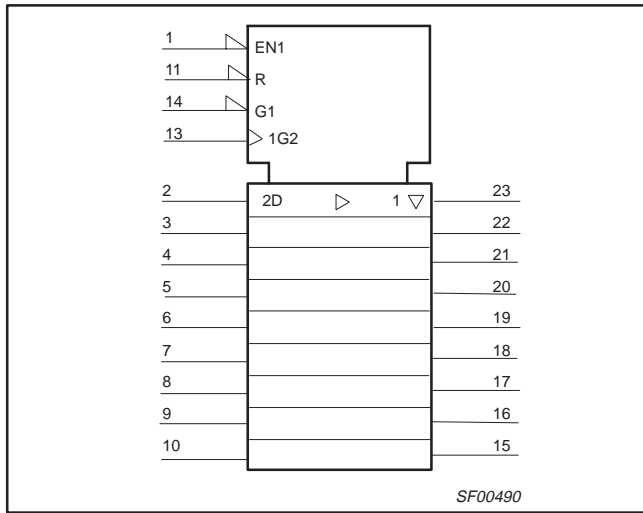
LOGIC SYMBOL – 74F823



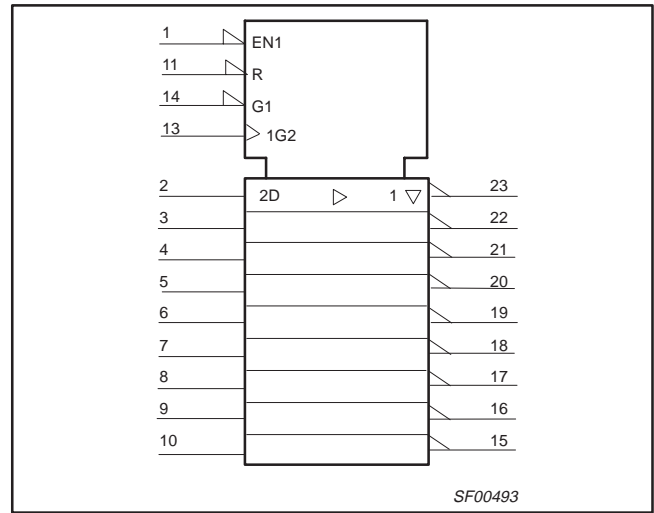
Bus interface registers

74F821/822/823/824/825/826

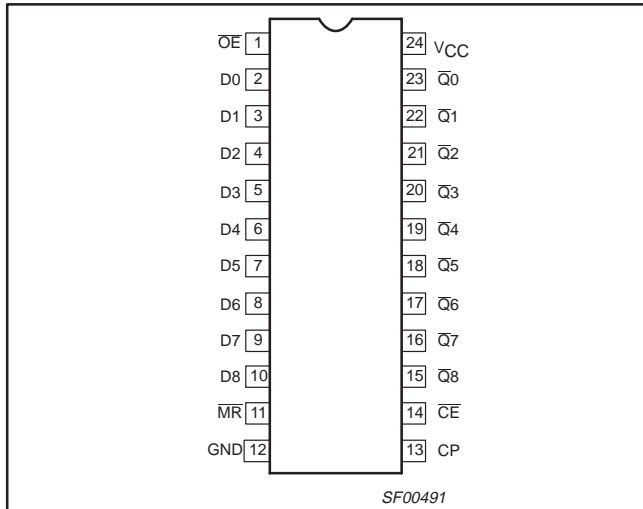
IEC/IEEE SYMBOL – 74F823



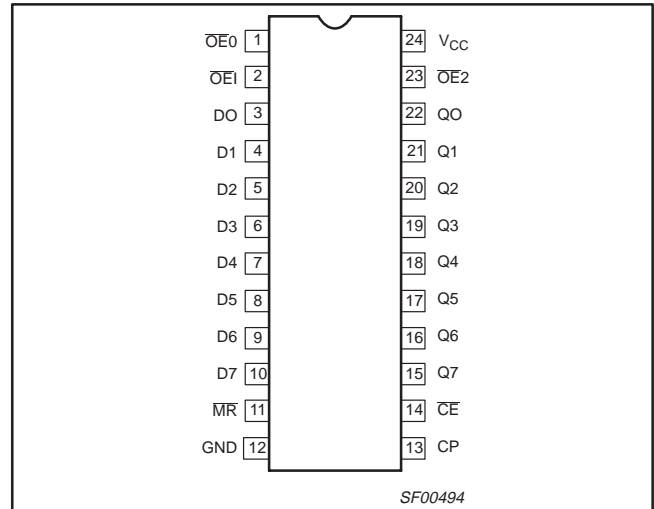
IEC/IEEE SYMBOL – 74F824



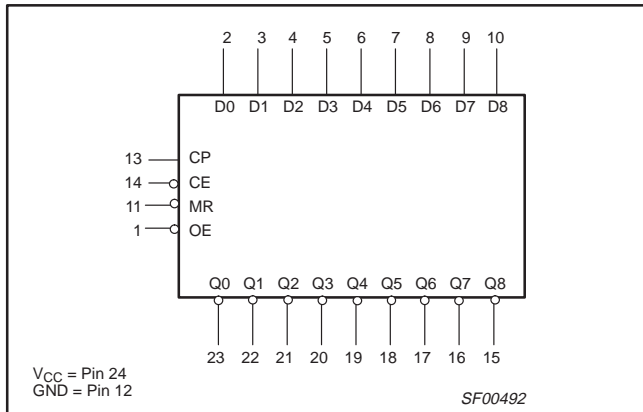
PIN CONFIGURATION – 74F824



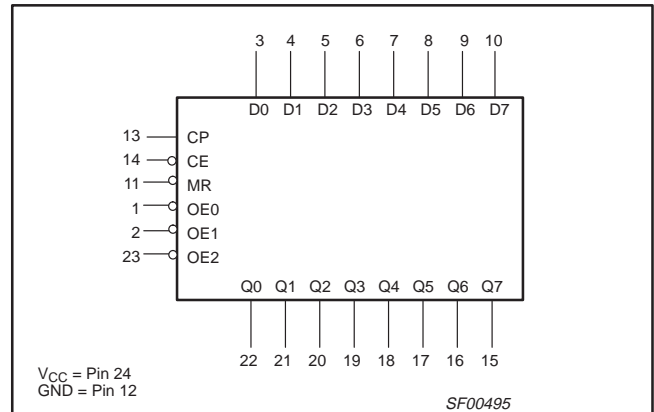
PIN CONFIGURATION – 74F825



LOGIC SYMBOL – 74F824



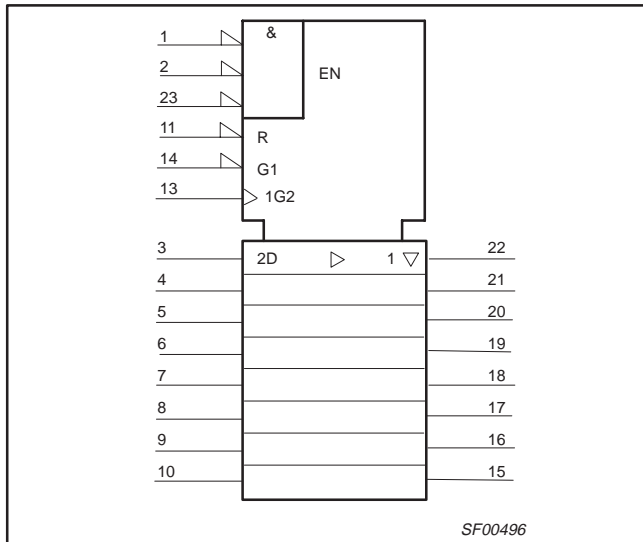
LOGIC SYMBOL – 74F825



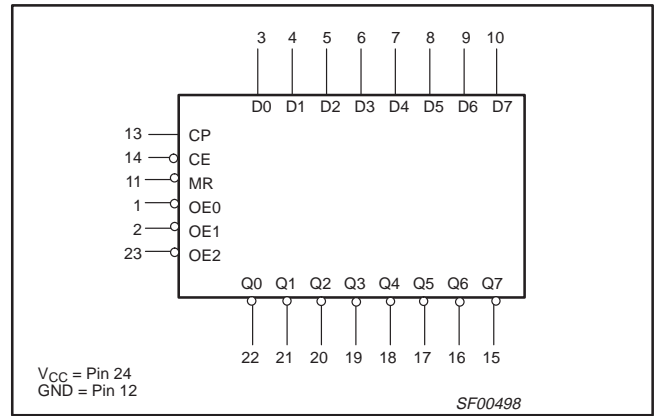
Bus interface registers

74F821/822/823/824/825/826

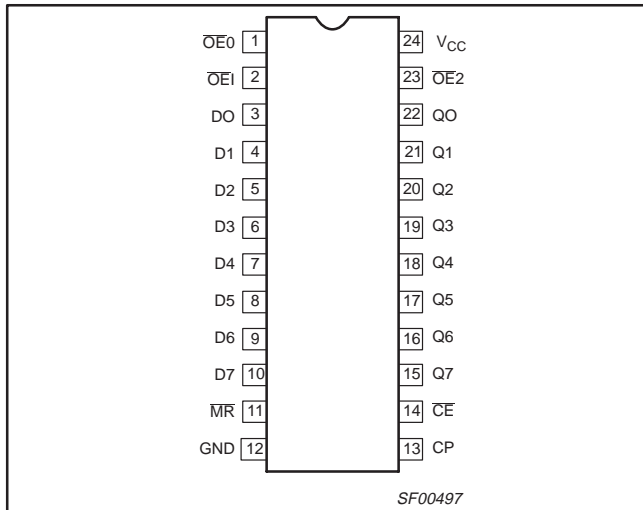
IEC/IEEE SYMBOL – 74F825



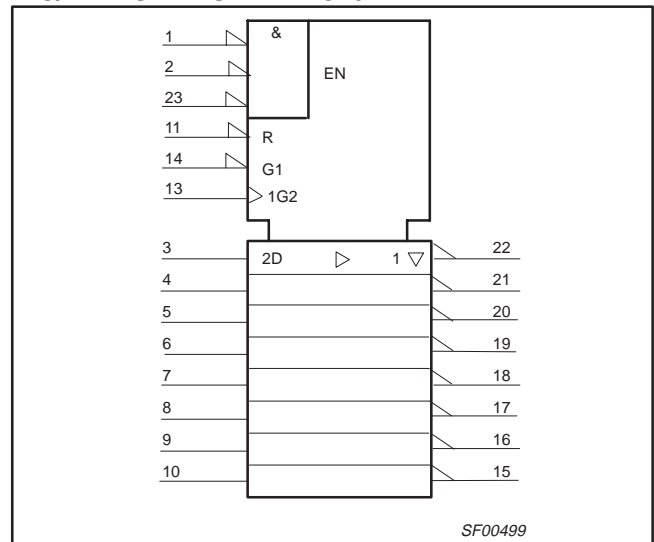
LOGIC SYMBOL – 74F826



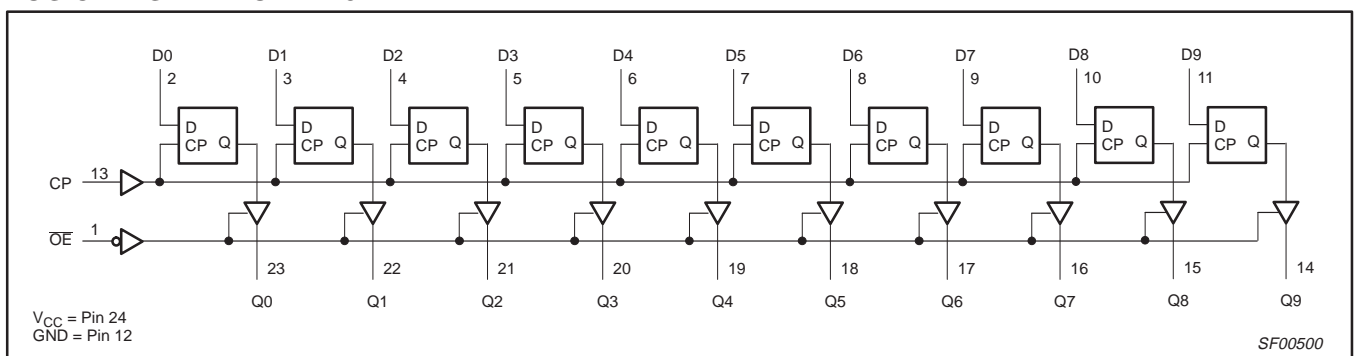
PIN CONFIGURATION – 74F826



IEC/IEEE SYMBOL – 74F826



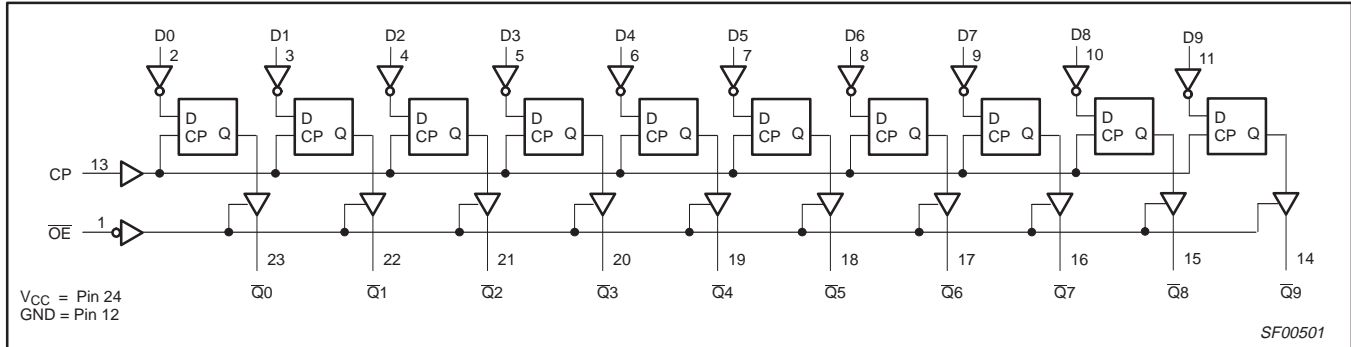
LOGIC DIAGRAM FOR 74F821



Bus interface registers

74F821/822/823/824/825/826

LOGIC DIAGRAM FOR 74F822

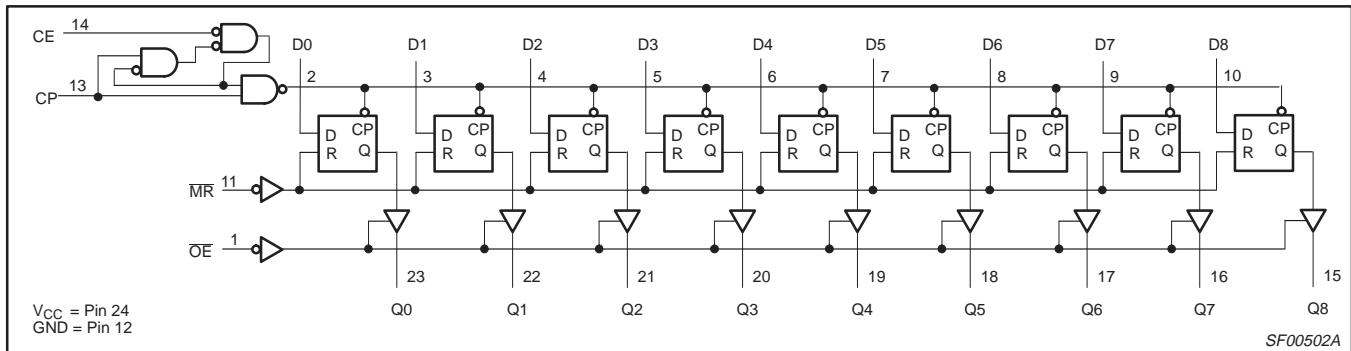


FUNCTION TABLE FOR 74F821 AND 74F822

| INPUTS | | | OUTPUTS | | OPERATING MODE |
|--------|----|----|---------|--------|--------------------|
| | | | 74F821 | 74F822 | |
| OE | CP | Dn | Q | Q̄ | |
| L | ↑ | l | L | H | Load and read data |
| L | ↑ | h | H | L | |
| L | ↕ | X | NC | NC | Hold |
| H | X | X | Z | Z | High impedance |

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↑ = Low-to-high clock transition
- ↕ = Not low-to-high clock transition

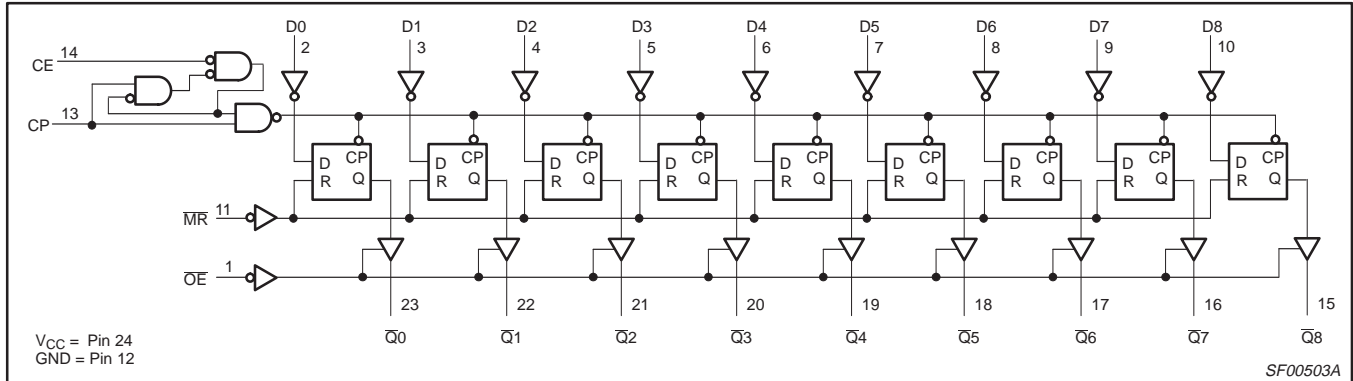
LOGIC DIAGRAM FOR 74F823



Bus interface registers

74F821/822/823/824/825/826

LOGIC DIAGRAM FOR 74F824

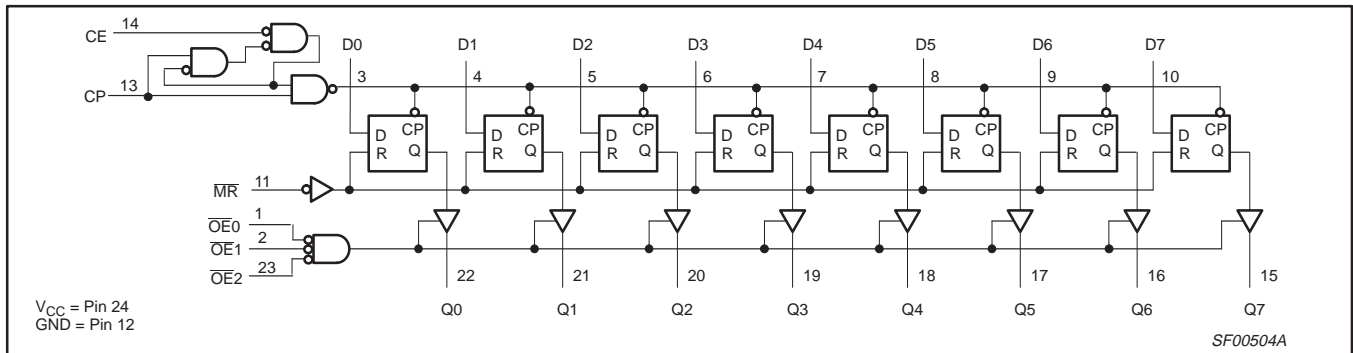


FUNCTION TABLE for 74F823 and 74F824

| INPUTS | | | | | OUTPUTS | | OPERATING MODE |
|--------|----|-----|----|----|---------|--------|--------------------|
| | | | | | 74F823 | 74F824 | |
| OE | MR | CE* | CP | Dn | Q | Q̄ | |
| L | L | X | X | X | L | L | Clear |
| L | H | L | ↑ | h | H | L | Load and read data |
| L | H | L | ↑ | l | L | H | |
| L | H | H | X | X | NC | NC | Hold |
| H | X | X | X | X | Z | Z | High impedance |

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- * = Since CE input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the CE input.
- ↑ = Low-to-high clock transition

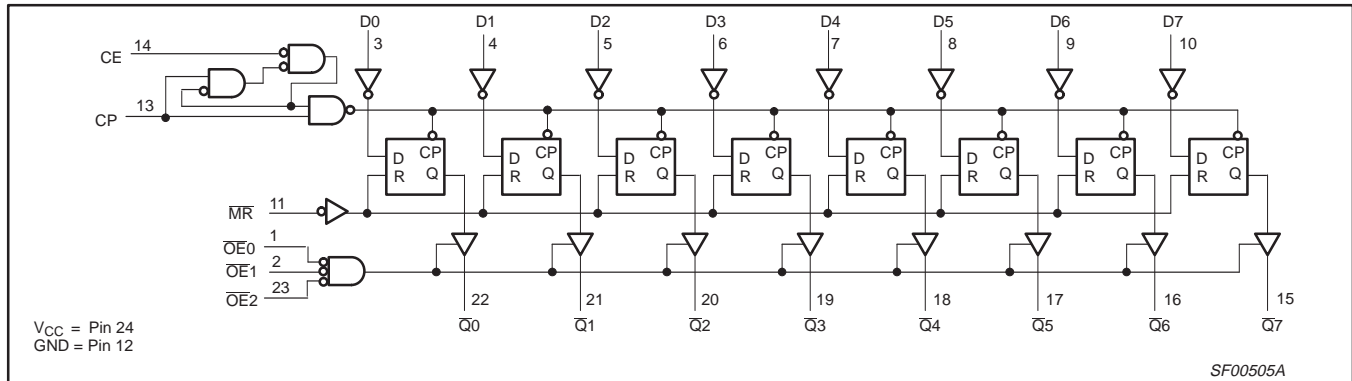
LOGIC DIAGRAM FOR 74F825



Bus interface registers

74F821/822/823/824/825/826

LOGIC DIAGRAM FOR 74F826



FUNCTION TABLE FOR 74F825 AND 74F826

| INPUTS | | | | | OUTPUTS | | OPERATING MODE |
|-----------------|----|-----|----|----------------|---------|--------|--------------------|
| | | | | | 74F825 | 74F826 | |
| OE _n | MR | CE* | CP | D _n | Q | Q̄ | |
| L | L | X | X | X | L | L | Clear |
| L | H | L | ↑ | h | H | L | Load and read data |
| L | H | L | ↑ | l | L | H | |
| L | H | H | X | X | NC | NC | Hold |
| H | X | X | X | X | Z | Z | High impedance |

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- * = Since CE input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the CE input.
- ↑ = Low-to-high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|-------------------------|------------|
| V _{CC} | Supply voltage | -0.5 to +7.0 | V |
| V _{IN} | Input voltage | -0.5 to +7.0 | V |
| I _{IN} | Input current | -30 to +5 | mA |
| V _{OUT} | Voltage applied to output in high output state | -0.5 to V _{CC} | V |
| I _{OUT} | Current applied to output in low output state | 128 | mA |
| T _{amb} | Operating free-air temperature range | Commercial range | 0 to +70 |
| | | Industrial range | -40 to +85 |
| T _{stg} | Storage temperature range | -65 to +150 | °C |

Bus interface registers

74F821/822/823/824/825/826

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|------------------|--------------------------------------|------------------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{Ik} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -24 | mA |
| I _{OL} | Low-level output current | | | 64 | mA |
| T _{amb} | Operating free-air temperature range | Commercial range | 0 | +70 | °C |
| | | Industrial range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|------------------|--|---|-------------------------|-----------------------|------|------|------|
| | | | MIN | TYP ² | MAX | | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OH} = -15mA | ±10%V _{CC} | 2.4 | | V |
| | | | | ±5%V _{CC} | 2.4 | | V |
| | | | I _{OH} = -24mA | ±10%V _{CC} | 2.0 | | V |
| | | | | ±5%V _{CC} | 2.0 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OL} = MAX | ±10%V _{CC} | | 0.55 | V |
| | | | | ±5%V _{CC} | | 0.42 | 0.55 |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | -0.73 | -1.2 | V | |
| I _I | Input current at maximum input voltage | V _{CC} = 0.0V, V _I = 7.0V | | | 100 | μA | |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7V | | | 20 | μA | |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.5V | | | -20 | μA | |
| I _{OZH} | Off-state output current, high-level voltage applied | V _{CC} = MAX, V _O = 2.7V | | | 50 | μA | |
| I _{OZL} | Off-state output current, low-level voltage applied | V _{CC} = MAX, V _O = 0.5V | | | -50 | μA | |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | -100 | | -225 | mA | |
| I _{CC} | Supply current (total) | 74F821, 74F822 | I _{CCH} | V _{CC} = MAX | 75 | 105 | mA |
| | | | I _{CCL} | | 75 | 105 | mA |
| | | | I _{CCZ} | | 75 | 115 | mA |
| | | 74F823, 74F824 | I _{CCH} | V _{CC} = MAX | 65 | 100 | mA |
| | | | I _{CCL} | | 70 | 105 | mA |
| | | | I _{CCZ} | | 75 | 110 | mA |
| | | 74F825, 74F826 | I _{CCH} | V _{CC} = MAX | 60 | 85 | mA |
| | | | I _{CCL} | | 60 | 90 | mA |
| | | | I _{CCZ} | | 65 | 95 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Bus interface registers

74F821/822/823/824/825/826

AC ELECTRICAL CHARACTERISTICS FOR 74F821/74F822/74F824/74F825/74F826

| SYMBOL | PARAMETER | | TEST CONDITION | LIMITS | | | | | UNIT |
|--------------------------------------|--|---------------------------|--------------------------|---|------------|------------|--|-------------|------|
| | | | | T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | | MIN | TYP | MAX | MIN | MAX | |
| f _{max} | Maximum clock frequency | | Waveform 1 | 150 | 180 | | 140 | | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to Qn or \bar{Q} n | 74F821, 74F825, 74F826 | Waveform 1 | 4.0 4.0 | 6.5 6.0 | 8.5 8.5 | 4.0 3.5 | 9.5 9.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to \bar{Q} n | 74F822, 74F824 | Waveform 1 | 4.5 4.5 | 6.5 6.5 | 9.0 9.0 | 4.5 4.5 | 10.0 9.0 | ns |
| t _{PHL} | Propagation delay $\bar{M}R$ to Qn or \bar{Q} n | 74F824 74F825, 74F826 | Waveform 2 | 3.0 | 5.0 | 8.0 | 3.0 | 8.0 | ns |
| t _{PZH} t _{PZL} | Output enable time $\bar{O}E$ n to Qn or \bar{Q} n | | Waveform 4 Waveform 5 | 2.0 3.0 | 4.5 5.0 | 8.0 8.0 | 2.0 2.5 | 9.0 9.0 | ns |
| t _{PHZ} t _{PLZ} | Output disable time $\bar{O}E$ n to Qn or \bar{Q} n | | Waveform 4 Waveform 5 | 1.5 1.5 | 3.5 3.5 | 6.5 6.5 | 1.5 1.5 | 7.5 7.5 | ns |

AC SETUP REQUIREMENTS FOR 74F821/74F822/74F824/74F825/74F826

| SYMBOL | PARAMETER | | TEST CONDITION | LIMITS | | | | | UNIT |
|--|--|---------------------------|----------------|---|-----|-----|--|-----|------|
| | | | | T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{SU} (H) t _{SU} (L) | Setup time, high or low Dn to CP | | Waveform 3 | 1.0 1.0 | | | 1.0 1.0 | | ns |
| t _H (H) t _H (L) | Hold time, high or low Dn to CP | | Waveform 3 | 2.0 2.0 | | | 2.0 2.0 | | ns |
| t _W (H) t _W (L) | CP Pulse width, high or low | | Waveform 1 | 3.5 3.5 | | | 4.0 4.0 | | ns |
| t _{SU} (H) t _{SU} (L) | Setup time, high or low, $\bar{C}E$ to CP | 74F824, 74F825, 74F826 | Waveform 3 | 0.0 2.0 | | | 0.0 2.0 | | ns |
| t _H (H) t _H (L) | Hold time, high or low $\bar{C}E$ to CP | | Waveform 3 | 0.0 3.0 | | | 0.0 3.5 | | ns |
| t _W (L) | $\bar{M}R$ Pulse width, low | | Waveform 2 | 4.5 | | | 4.5 | | ns |
| t _{rec} | Recovery time, $\bar{M}R$ to CP | | Waveform 2 | 2.5 | | | 2.5 | | ns |

Bus interface registers

74F821/822/823/824/825/826

AC ELECTRICAL CHARACTERISTICS FOR 74F823

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | |
|------------------------|---|--------------------------|--|------------|------------|---|------------|---|-------------|-----|
| | | | $T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| f_{max} | Maximum clock frequency | Waveform 1 | 150 | 180 | | 140 | | 130 | | ns |
| t_{PLH} t_{PHL} | Propagation delay CP to Q_n or \bar{Q}_n | Waveform 1 | 4.0 4.0 | 6.5 6.0 | 8.5 8.5 | 4.0 3.5 | 9.5 9.0 | 4.0 3.5 | 10.0 9.0 | ns |
| t_{PHL} | Propagation delay $\bar{M}R$ to Q_n or \bar{Q}_n | Waveform 2 | 3.0 | 5.0 | 8.0 | 3.0 | 8.0 | 3.0 | 8.5 | ns |
| t_{PZH} t_{PZL} | Output enable time OEn to Q_n or \bar{Q}_n | Waveform 4 Waveform 5 | 2.0 3.0 | 4.5 5.0 | 8.0 8.0 | 2.0 2.5 | 9.0 9.0 | 2.0 2.5 | 11.0 9.0 | ns |
| t_{PHZ} t_{PLZ} | Output disable time OEn to Q_n or \bar{Q}_n | Waveform 4 Waveform 5 | 1.5 1.5 | 3.5 3.5 | 6.5 6.5 | 1.5 1.5 | 7.5 7.5 | 1.5 1.5 | 8.5 8.5 | ns |

AC SETUP REQUIREMENTS FOR 74F823

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | |
|----------------------------|--|----------------|--|-----|-----|---|-----|---|------|-----|
| | | | $T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| $t_{su}(H)$ $t_{su}(L)$ | Setup time, high or low Dn to CP | Waveform 3 | 1.0 1.0 | | | 1.0 1.0 | | 2.0 1.5 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold time, high or low Dn to CP | Waveform 3 | 2.0 2.0 | | | 2.0 2.0 | | 2.5 2.0 | | ns |
| $t_w(H)$ $t_w(L)$ | CP Pulse width, high or low | Waveform 1 | 3.5 3.5 | | | 4.0 4.0 | | 4.0 4.0 | | ns |
| $t_{su}(H)$ $t_{su}(L)$ | Setup time, high or low, $\bar{C}E$ to CP | Waveform 3 | 0.0 2.0 | | | 0.0 2.0 | | 0.0 2.0 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold time, high or low $\bar{C}E$ to CP | Waveform 3 | 0.0 3.0 | | | 0.0 3.5 | | 1.5 4.0 | | ns |
| $t_w(L)$ | $\bar{M}R$ Pulse width, low | Waveform 2 | 4.5 | | | 4.5 | | 4.5 | | ns |
| t_{rec} | Recovery time, $\bar{M}R$ to CP | Waveform 2 | 2.5 | | | 2.5 | | 2.5 | | ns |

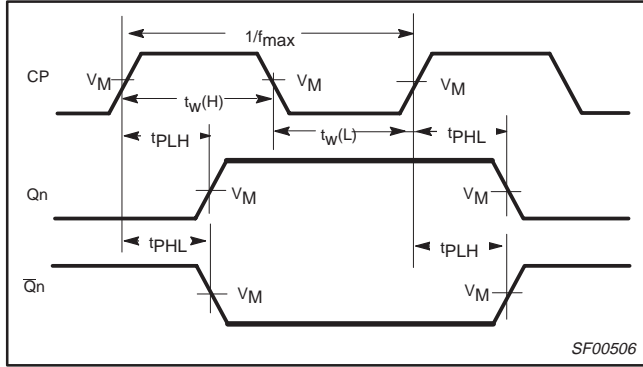
Bus interface registers

74F821/822/823/824/825/826

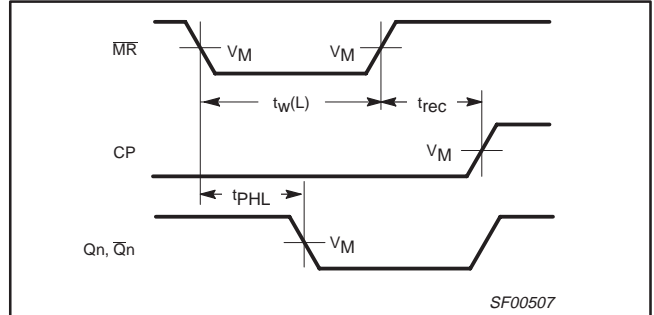
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

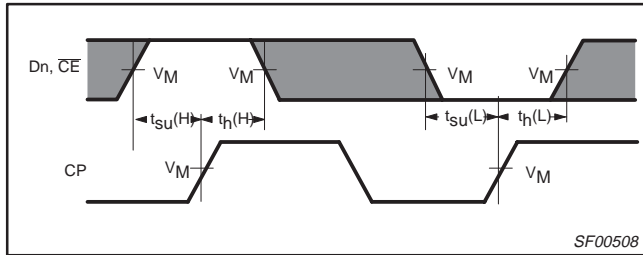
The shaded areas indicate when the input is permitted to change for predictable output performance.



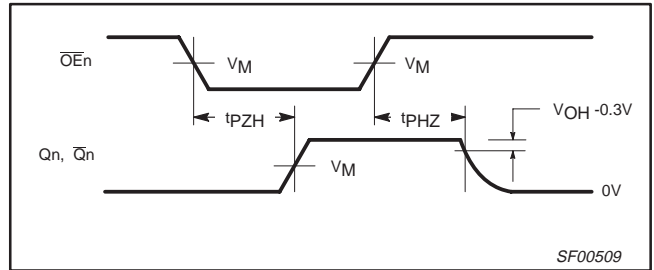
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



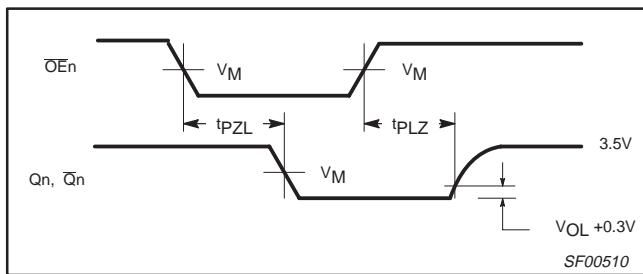
Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time



Waveform 3. Data setup time and hold times



Waveform 4. 3-State output enable time to high level and output disable time from high level

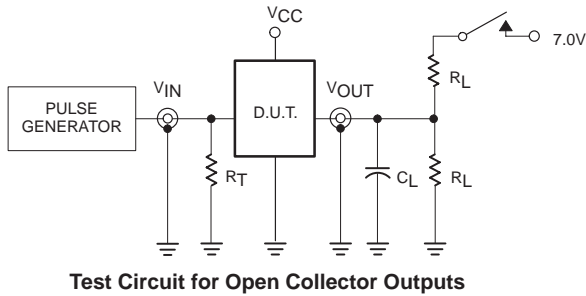


Waveform 5. 3-State output enable time to low level and output disable time from low level

Bus interface registers

74F821/822/823/824/825/826

TEST CIRCUIT AND WAVEFORMS

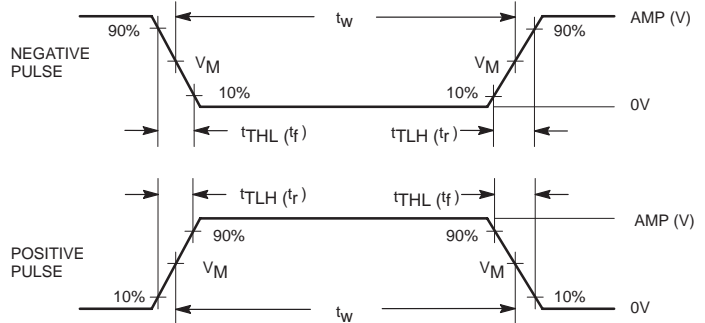


SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| t_{PLZ} | closed |
| t_{PZL} | closed |
| All other | open |

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

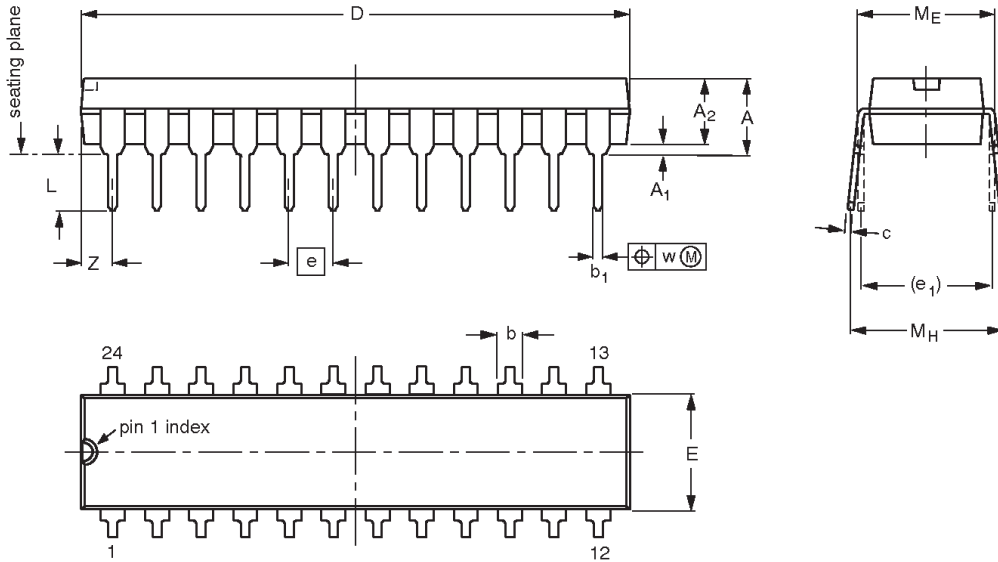
SF00128

Bus interface registers

74F821/822/823/824/825/826

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|----------------|----------------|----------------|------|-----------------------|
| mm | 4.70 | 0.38 | 3.94 | 1.63 1.14 | 0.56 0.43 | 0.36 0.25 | 31.9 31.5 | 6.73 6.48 | 2.54 | 7.62 | 3.51 3.05 | 8.13 7.62 | 10.03 7.62 | 0.25 | 2.05 |
| inches | 0.185 | 0.015 | 0.155 | 0.064 0.045 | 0.022 0.017 | 0.014 0.010 | 1.256 1.240 | 0.265 0.255 | 0.100 | 0.300 | 0.138 0.120 | 0.32 0.30 | 0.395 0.300 | 0.01 | 0.081 |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

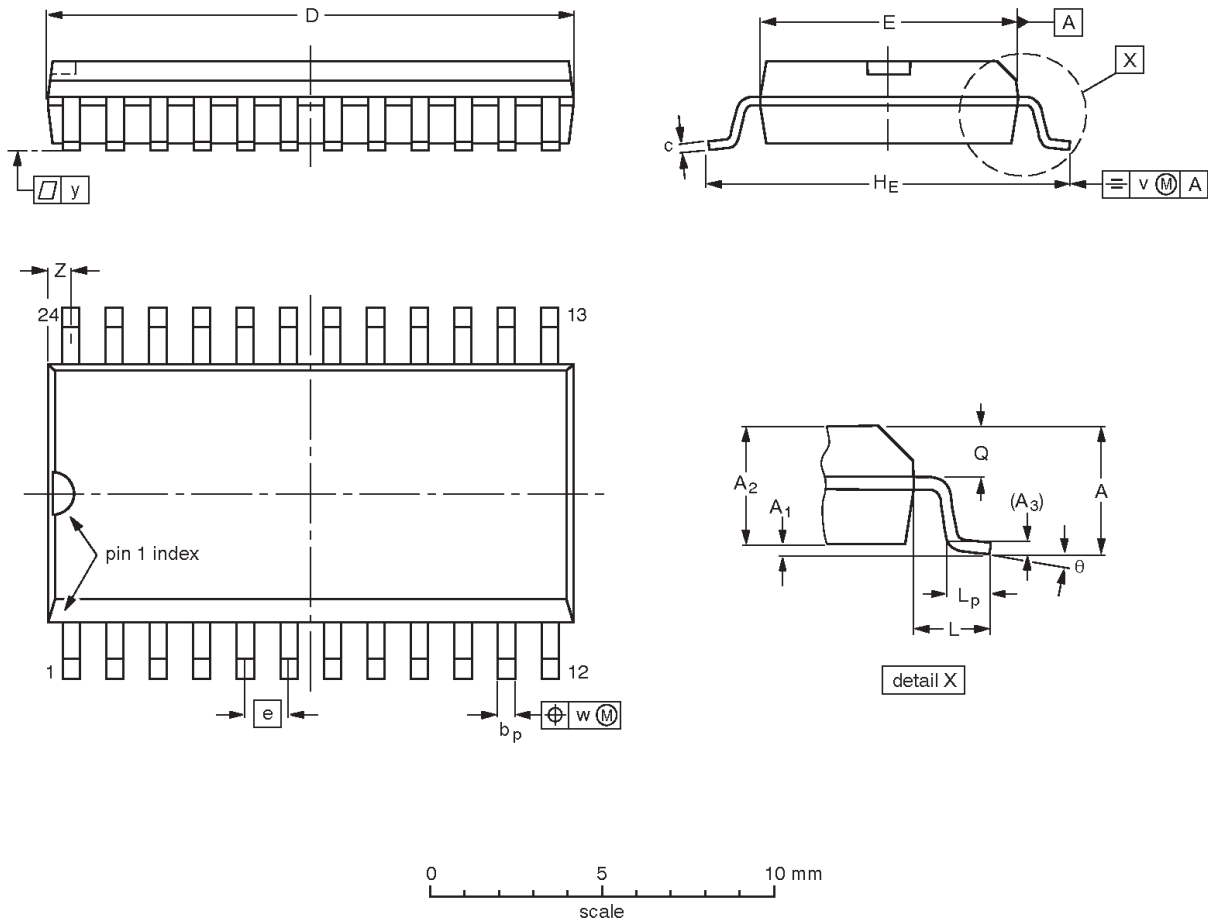
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT222-1 | | MS-001AF | | | | 95-03-11 |

Bus interface registers

74F821/822/823/824/825/826

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 15.6 15.2 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.61 0.60 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT137-1 | 075E05 | MS-013AD | | | | 95-01-24 97-05-22 |

Bus interface registers

74F821/822/823/824/825/826

NOTES

Bus interface registers

74F821/822/823/824/825/826

DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
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