PYRAMID SEMICONDUCTOR CORPORATION

P54FCT245/74FCT245

OCTAL TRANSCEIVER WITH 3-STATE OUTPUTS

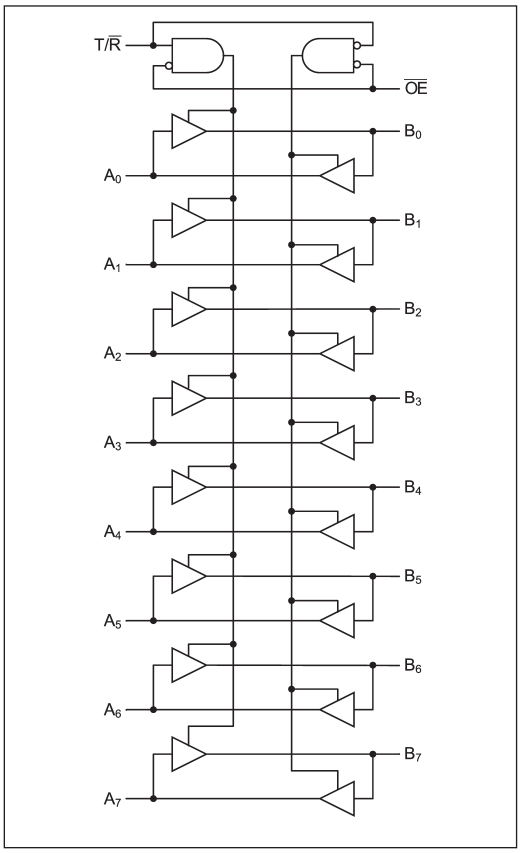
FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-A speed at 4.9ns max (MIL)**
- **Output levels compatible with TTL and CMOS**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **48 mA sink current, 12 mA source current (MIL)**

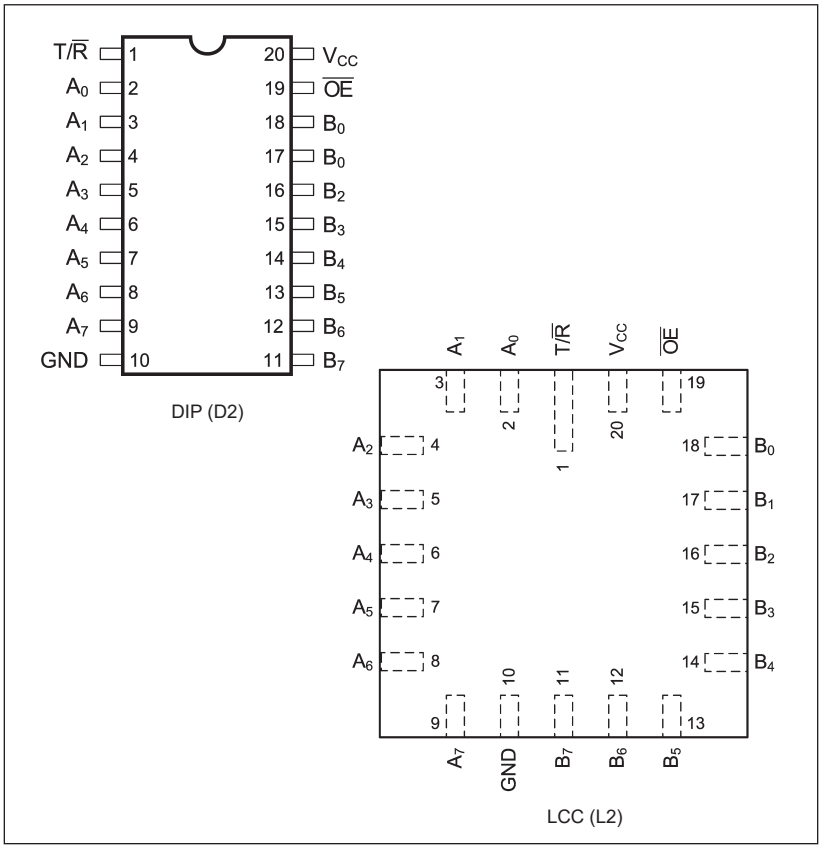
DESCRIPTION

The P54/74FCT245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus oriented applications. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in a High-Z condition.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1,2]

Sym	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Temperature Under Bias	-65 to +135	°C
V_{CC}	V_{CC} Potentional to Ground	-0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	-0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	-0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Grade	Ambient Temp	GND	V_{cc}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 5%

CAPACITANCES

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	Test Conditions		Min	Max	Unit
V_{OH}	High Level Output Voltage	V_{CC} = V_{CC} (Min) V_{IH} = 2.0 V, V_{IL} = 0.8 V	I_{OH} = -300 µA	4.3		V
			I_{OH} = -12 mA	2.4		
V_{OL}	Low Level Output Voltage (Port A and Port B)	V_{CC} = V_{CC} (Min) V_{IH} = 2.0 V, V_{IL} = 0.8 V	I_{OL} = 300 µA		0.2	V
			I_{OL} = 48 mA		0.55	
V_{IK}	Input Clamp Voltage	V_{CC} = V_{CC} (Min), I_{IN} = -18mA			-1.2	V
I_{IH1}	High Level Input Current	V_{CC} = V_{CC} (Max), V_{IN} = V_{CC}			5.0	µA
I_{IH2}	High Level Input Current for Common I/O Pins	V_{CC} = V_{CC} (Max), V_{IN} = V_{CC}			20	µA
I_{IL1}	Low Level Input Current	V_{CC} = V_{CC} (Max), V_{IN} = GND			-5.0	µA
I_{IL2}	Low Level Input Current for Common I/O Pins	V_{CC} = V_{CC} (Max), V_{IN} = GND			-20	µA
I_{OZH}	High Impedence Output Current	V_{CC} = V_{CC} (Max), V_{IN} = V_{CC}			5	µA
I_{OZL}		V_{CC} = V_{CC} (Max), V_{IN} = GND			-5	
I_{OS}	Short Circuit Output Current	V_{CC} = V_{CC} (Max)		-60		mA
I_{CCQ}	Quiescent Power Supply Current (CMOS inputs)	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} - 0.2 V V_{CC} = V_{CC} (Max) f_i = 0 MHz			1.5	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC} = V_{CC} (Max) V_{IN} = 3.4 V			2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = V_{CC} (Max) Outputs open One bit toggling 50% duty cycle V_{IN} ≥ V_{CC} - 0.2 V or V_{IN} ≤ 0.2 V $\overline{OE}$ = GND, T/$\overline{R}$ = V_{CC}			0.4	mA/ MHz

Notes:

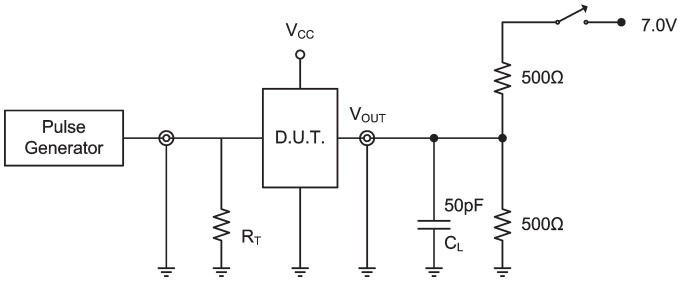
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

Sym	Parameter	Test Conditions			Min	Max	Unit
I_{CCT}	Total Power Supply Current	$V_{CC} = V_{CC}$ (Max) Outputs open, $\overline{OE} = T/\overline{R}$ = GND 50% duty cycle	f_i = 10 MHz One bit toggling	$V_{IN} \geq 5.3$ V or $V_{IN} \leq 0.2$ V		5.5	mA
				$V_{IN} = 3.4$ V or V_{IN} = GND		6.0	mA
			f_i = 2.5 MHz Eight bits toggling	$V_{IN} \geq 5.3$ V or $V_{IN} \leq 0.2$ V		6.5	mA
				$V_{IN} = 3.4$ V or V_{IN} = GND		14.5	mA
C_{IN}	Input Capacitance	T_C = +25°C, V_{CC} = GND, F = 1 MHz				10	pF
$C_{I/O}$	Output Capacitance	T_C = +25°C, V_{CC} = GND, F = 1 MHz				12	pF

AC CHARACTERISTICS

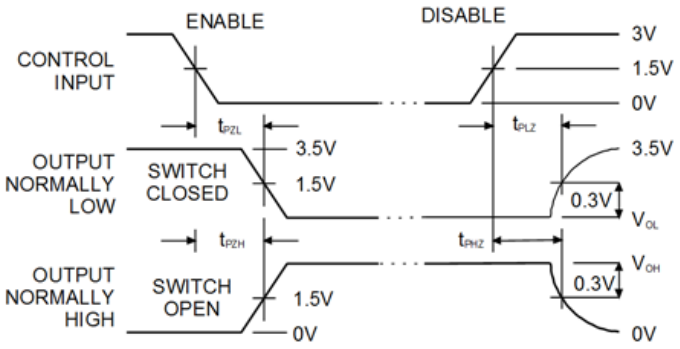
(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	Condition	54/74FCT245				54/74FCT245A				Unit
			Ind		Mil		Ind		Mil		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time $T/\overline{R}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $T/\overline{R}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns

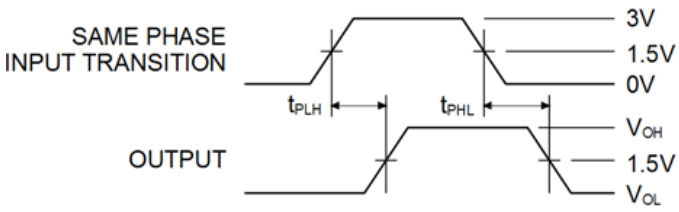


Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

ENABLE/DISABLE TIMES



PROPAGATION DELAY



PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = High Voltage Level
X = Don't Care
L = Low Voltage Level
Z = High Impedance

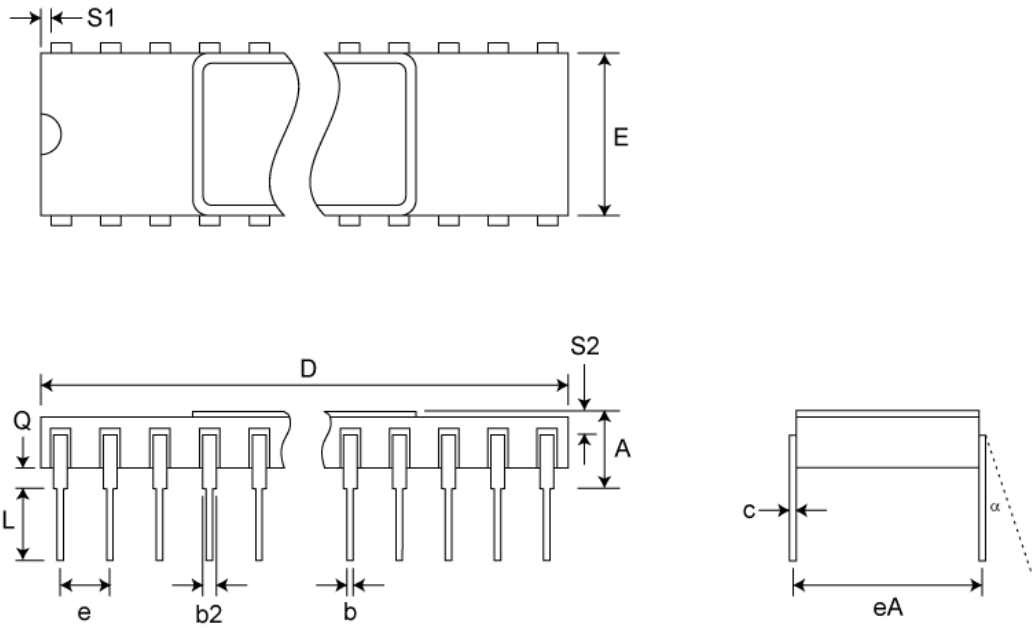
ORDERING INFORMATION

PxxFCT — xx — x — x

- PxxFCT — Temp. Class
  - 74 — Industrial
  - 54 — Military
- xx — Device Type
  - 245 — Octal Buffer/Line Driver
  - 245A — Fast Octal Buffer/Line Driver
- x — Package
  - C — Ceramic side brazed DIP, 300 mil
  - L — Square LCC (350x350 mil)
- x — Processing
  - I — -40°C to +85°C
  - M — -55°C to +125°C
  - MB — Mil Temp with MIL-STD-883 Class B Compliance

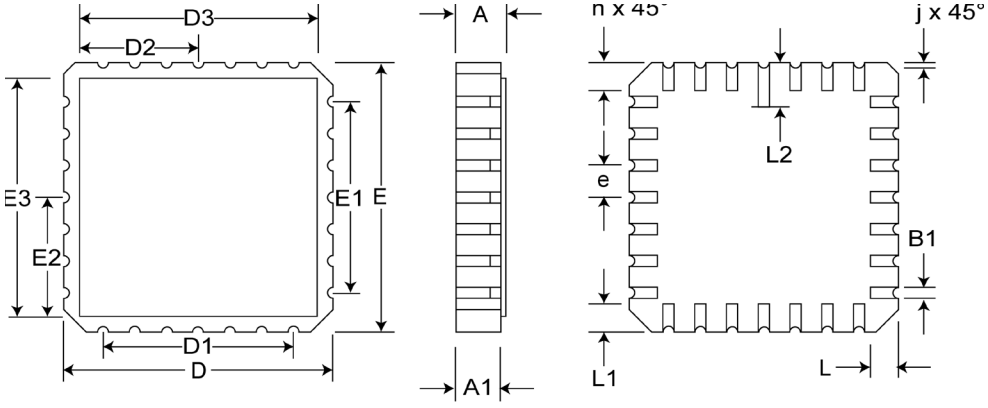
Pkg #	D2	
# Pins	20 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	-	1.060
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-
α	0°	15°

SIDEBRAZED DUAL INLINE PACKAGE



Pkg #	L2	
# Pins	20	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.342	0.358
D1/E1	0.200 BSC	
D2/E2	0.100 BSC	
D3/E3	-	0.358
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	5	

SQUARE LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	LOGIC109
DOCUMENT TITLE	P54FCT245 - FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS WITH 3-STATE OUTPUTS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Mar 2016	JDB	New Data Sheet
01	Mar 2016	JDB	Title Change