



FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT574/A/C

FEATURES:

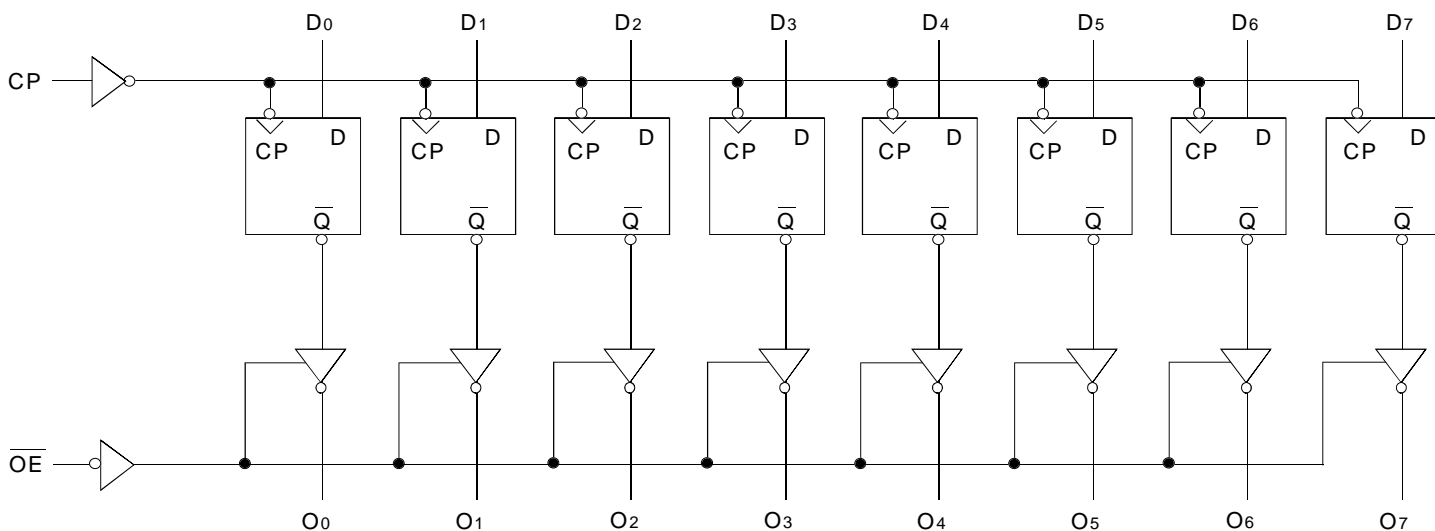
- IDT54/74FCT574 equivalent to FAST™ speed and drive
- IDT54/74FCT574A up to 30% faster than FAST
- IDT54/74FCT574C up to 50% faster than FAST
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Edge triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC, CERPACK

DESCRIPTION:

The FCT574 is an 8-bit register built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable (\overline{OE}) is low, the eight outputs are enabled. When the \overline{OE} input is high, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the low-to-high transition of the clock input. The FCT574 has non-inverting outputs with respect to the data at the D inputs.

FUNCTIONAL BLOCK DIAGRAM

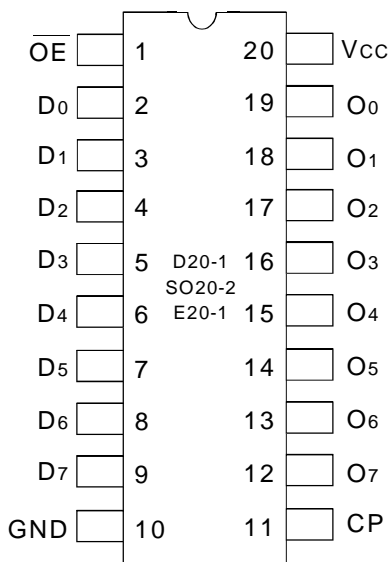


MILITARY AND COMMERCIAL TEMPERATURE RANGES

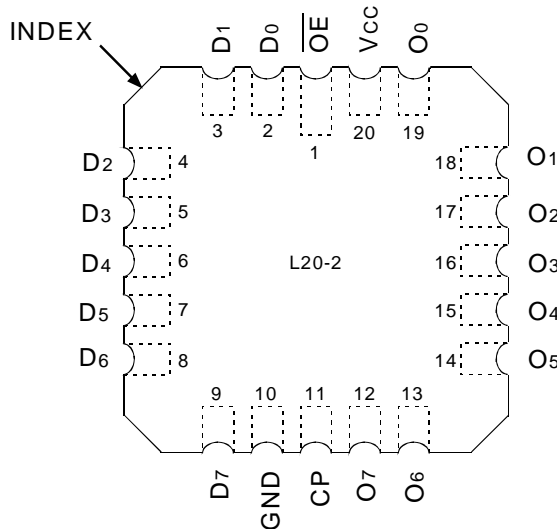
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PIN CONFIGURATION



CERDIP/ SOIC/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
DN	D Flip-Flop Data Inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
ON	3-State Outputs (true)
OE	Active LOW 3-state Output Enable Input

FUNCTION TABLE (1)

Function	Inputs			Outputs	Internal
	OE	CP	DN	ON	QN
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
NC = No Change
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	5	μA
I_{IL}	Input LOW Current		$V_i = 2.7V$	—	—	5 ⁽⁴⁾	
			$V_i = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_i = GND$	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_o = V_{CC}$	—	—	10	μA
I_{OZL}			$V_o = 2.7V$	—	—	10 ⁽⁴⁾	
			$V_o = 0.5V$	—	—	-10 ⁽⁴⁾	
			$V_o = GND$	—	—	-10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_o = GND$		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC}$ or $V_{HC}, I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
			$I_{OH} = -12mA$ MIL.	2.4	4.3	—	
			$I_{OH} = -15mA$ COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC}$ or $V_{HC}, I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$	
			$I_{OL} = 32mA$ MIL.	—	0.3	0.5	
			$I_{OL} = 48mA$ COM'L.	—	0.3	0.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE} = GND$ One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = GND$ fi = 5MHz 50% Duty Cycle One Bit Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = GND$ Eight Bits Toggling fi = 2.5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	4	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.2	16.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

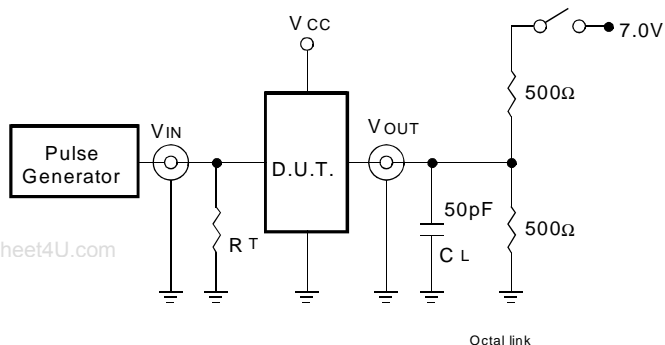
Symbol	Parameter	Conditions ⁽¹⁾	54/74FCT574				54/74FCT574A				54/74FCT574C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to ON	CL = 50pF RL = 500Ω	2	10	2	11	2	6.5	2	7.2	2	5.2	2	6.2	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	12.5	1.5	14	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.2	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	8	1.5	8	1.5	5.5	1.5	6.5	1.5	5	1.5	5.7	ns
t _{SU}	Set-up Time HIGH or LOW, D _N to CP		2	—	2	—	2	—	2	—	2	—	2	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _w	CP Pulse Width HIGH or LOW		7	—	7	—	5	—	6	—	5	—	6	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

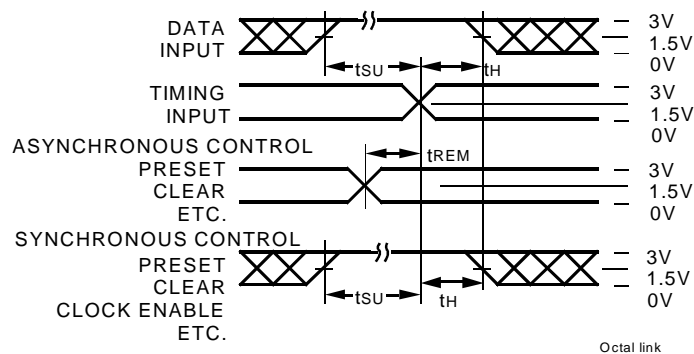
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

DEFINITIONS:

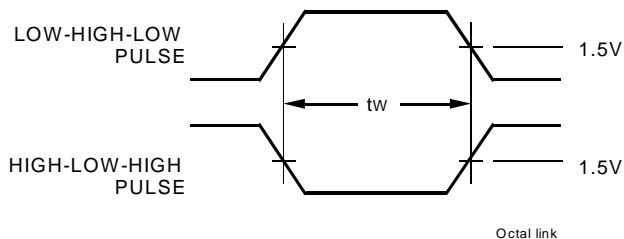
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

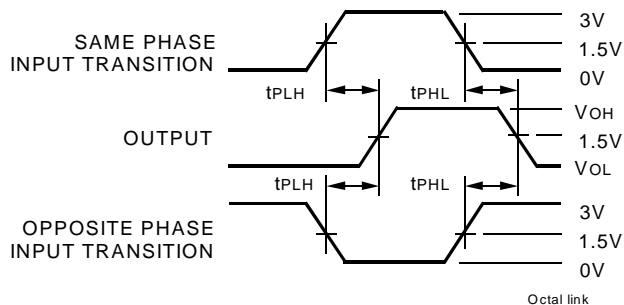
SET-UP, HOLD, AND RELEASE TIMES



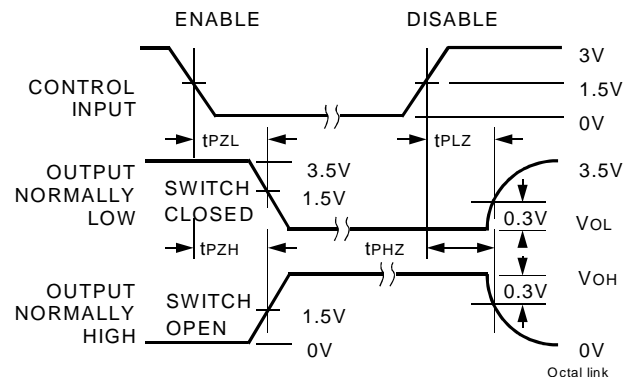
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT	XX	FCT	XXXX	XX	X	
Temp. Range	Device Type	Package	Process			
					Blank	Commercial
					B	MIL-STD-883, Class B
					SO	<u>Commercial Options</u> Small Outline IC (SO20-2)
					D	<u>Military Options</u> CERDIP (D20-1)
					E	CERPACK (E20-1)
					L	Leadless Chip Carrier (L20-2)
			574			Fast CMOS Octal D Register (3-State)
			574A			
			574C			
				54		- 55°C to +125°C
				74		- 40°C to +85°C



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