

74FR543

Octal Latched Transceiver with 3-STATE Outputs

General Description

The 74FR543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Both the A and B outputs will source 15 mA and sink 64 mA.

Features

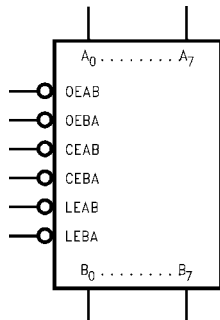
- Functionally equivalent to 74F543
- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 15 mA and current sinking capability of 64 mA
- Separate controls for data flow in each direction
- Guaranteed pin-to-pin skew
- Guaranteed 4000V minimum ESD protection

Ordering Code:

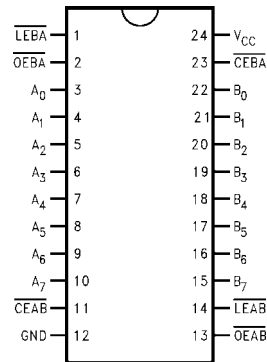
Order Number	Package Number	Package Description
74FR543SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74FR543SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OEAB} , \overline{OEBA}	Output Enable Inputs
\overline{LEAB} , \overline{LEBA}	Latch Enable Inputs
\overline{CEAB} , \overline{CEBA}	Chip Enable Inputs
A ₀ -A ₇	Side A Inputs or 3-STATE Outputs
B ₀ -B ₇	Side B Inputs or 3-STATE Outputs

Functional Description

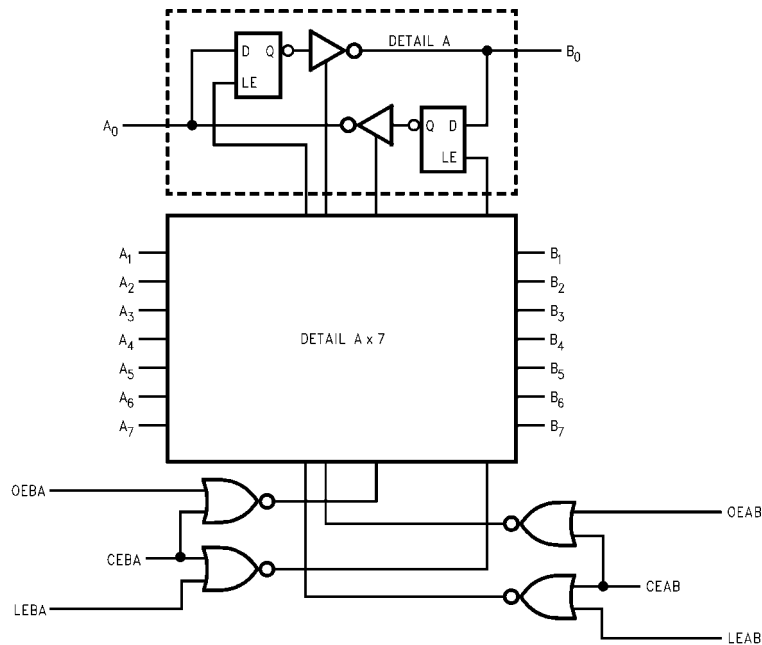
The 74FR543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A-to-B, for example, the A-to-B Enable (CEAB) input must be LOW in order to enter data from the A Port or take data from the B Port as indicated in the Data I/O Control Table. With \overline{CEAB} LOW, a LOW signal on (\overline{LEAB}) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LEAB} line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{CEAB} and \overline{OEAB} both LOW, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B-to-A is similar, but using the \overline{CEBA} , \overline{LEBA} and \overline{OEBA} .

Data I/O Control Table

Inputs			Latch Status	Output Buffers
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4			V	Min	I _{OH} = -3 mA (A _n , B _n)
		2.0			V	Min	I _{OH} = -15 mA (A _n , B _n)
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA (A _n , B _n)
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V (Control Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			-150	μA	Max	V _{IN} = 0.5 (CEAB, CEBA)
				-100	μA	Max	V _{IN} = 0.5 (LEAB, LEBA, OEAB, OEBA)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Circuit Leakage Test			3.75	μA	0.0	V _{IOD} = 150 mV, All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current			25	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			-150	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0.0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.25V (A _n , B _n)
I _{CCH}	Power Supply Current		59	72	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		87	102	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		69	85	mA	Max	Outputs 3-STATE
C _{IN}	Input Capacitance		8.0		pF	5.0	Control Pins
				17.0	pF	5.0	A _n , B _n

AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	1.3	3.0	4.7	1.3	4.7	ns
t _{PHL}	A _n to B _n or B _n to A _n	1.3	2.6	4.7	1.3	4.7	
t _{PLH}	Propagation Delay	2.3	5.7	8.5	2.3	8.5	ns
t _{PHL}	LEAB to B, LEBA to A	2.3	4.0	8.5	2.3	8.5	
t _{PZH}	Output Enable Time	2.3	4.3	7.4	2.3	7.4	ns
t _{PZL}		2.3	4.9	7.4	2.3	7.4	
t _{PHZ}	Output Disable Time	1.6	3.9	7.0	1.6	7.0	ns
t _{PLZ}		1.6	3.5	7.0	1.6	7.0	

AC Operating Requirements							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.5	0.5		2.5		ns
t _S (L)	D _n to LE	2.5	0.1		2.5		
t _H (H)	Hold Time, HIGH or LOW	2.0	0.0		2.0		ns
t _H (L)	D _n to LE	2.0	-0.6		2.0		
t _W (H)	LE Pulse Width HIGH	6.0	3.6		6.0		ns

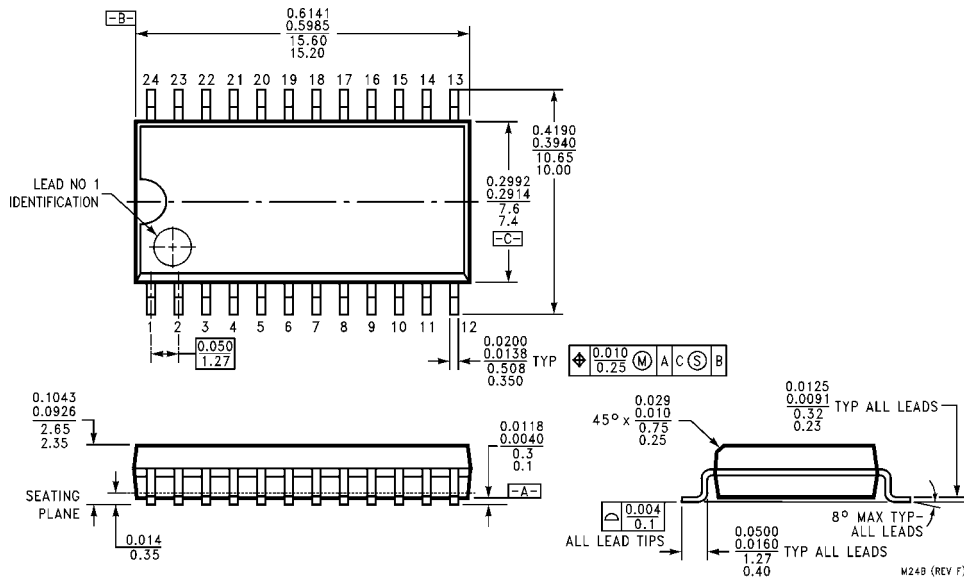
Extended AC Electrical Characteristics						
Symbol	Parameter	T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF Eight Outputs Switching (Note 3)		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 250 pF (Note 4)		Units
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.3	6.3	3.2	8.7	ns
t _{PHL}	A _n to B _n or B _n to A _n	1.3	6.3	3.2	8.7	
t _{PLH}	Propagation Delay	2.3	10.2	4.2	12.8	ns
t _{PHL}	LEAB to B, LEBA to A	2.3	10.2	4.2	12.8	
t _{PZH}	Output Enable Time	2.3	11.1			ns
t _{PZL}		2.3	11.1			
t _{PHZ}	Output Disable Time	1.6	7.2			ns
t _{PLZ}		1.6	7.2			
t _{OSHL} (Note 5)	Pin-to-Pin Skew for HL Transitions		1.2			ns
t _{OSLH} (Note 5)	Pin-to-Pin Skew for LH Transitions		1.0			ns
t _{OST} (Note 5)	Pin-to-Pin Skew for HL/LH Transitions		3.1			ns

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

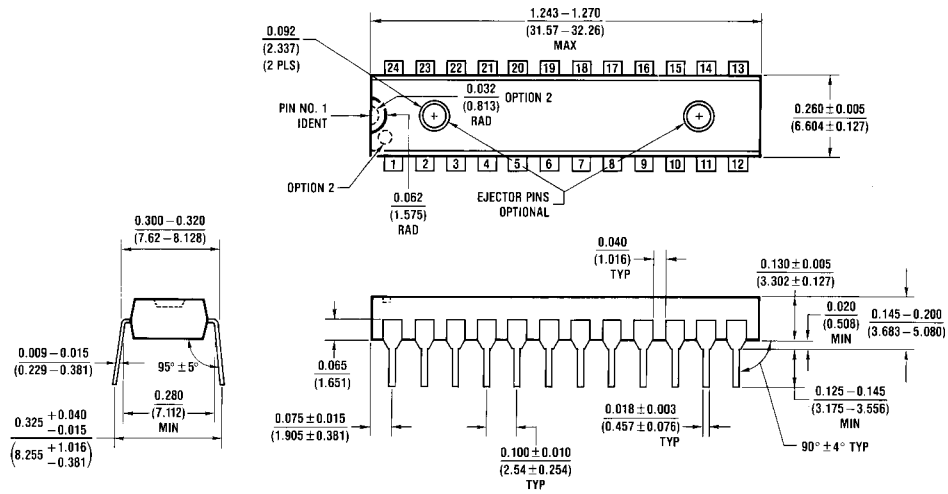
Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (t_{OSHL}), LOW-to-HIGH, (t_{OSLH}), or HIGH-to-LOW and/or LOW-to-HIGH, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C**

N24C (REV F)

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