

74HC3G07; 74HCT3G07

Triple buffer with open-drain outputs

Rev. 5 — 24 January 2019

Product data sheet

1. General description

The 74HC3G07; 74HCT3G07 is a triple buffer with open-drain outputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC3G07: CMOS level
 - For 74HCT3G07: TTL level
- Complies with JEDEC standard no. 7 A
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|--------|---|----------|
| | Temperature range | Name | Description | Version |
| 74HC3G07DP | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74HCT3G07DP | | | | |
| 74HC3G07DC | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74HCT3G07DC | | | | |

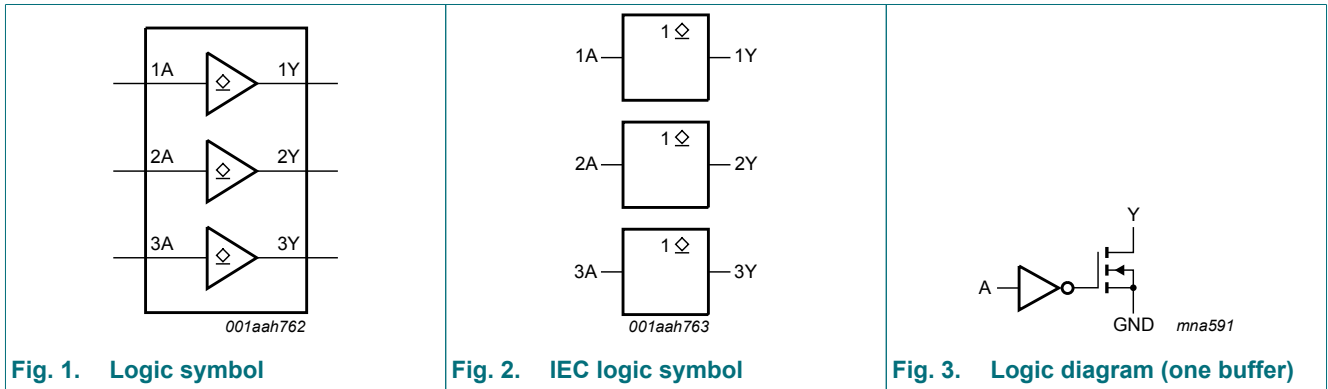
4. Marking

Table 2. Marking code

| Type number | Marking code [1] |
|-------------|------------------|
| 74HC3G07DP | H07 |
| 74HCT3G07DP | T07 |
| 74HC3G07DC | H07 |
| 74HCT3G07DC | T07 |

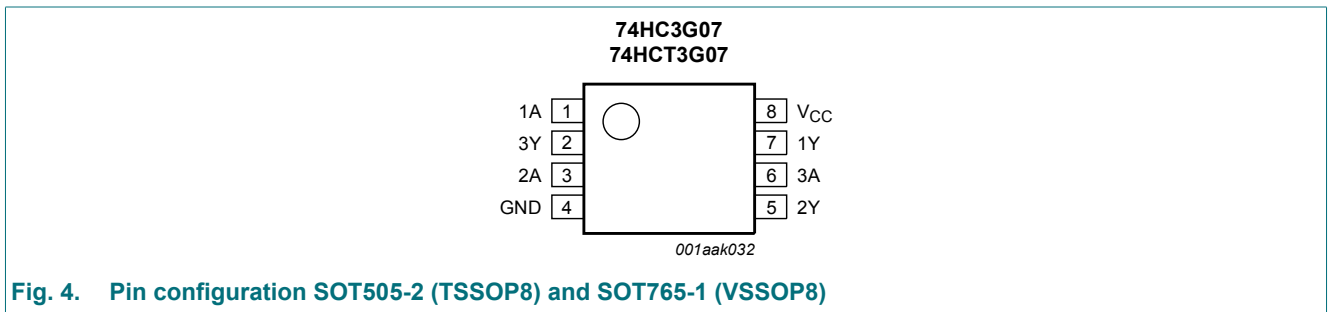
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|---------|----------------|
| 1A, 2A, 3A | 1, 3, 6 | data input |
| GND | 4 | ground (0 V) |
| 1Y, 2Y, 3Y | 7, 5, 2 | data output |
| V _{CC} | 8 | supply voltage |

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

| Input nA | Output nY |
|----------|-----------|
| L | L |
| H | Z |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------|--|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | 7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ [1] | -20 | - | mA |
| V_O | output voltage | active mode [1] | -0.5 | $V_{CC} + 0.5$ | V |
| | | high-impedance mode [1] | -0.5 | 7.0 | V |
| I_O | output current | $V_O = -0.5\text{ V}$ to 7.0 V [1] | -25 | - | mA |
| I_{CC} | supply current | [1] | - | 50 | mA |
| I_{GND} | ground current | [1] | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_D | dynamic power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2] | - | 300 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 74HC3G07 | | | 74HCT3G07 | | | Unit |
|---------------------|-------------------------------------|-------------------------|----------|------|----------|-----------|------|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 6.0 | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | - | - | - | ns/V |

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|------------------|---------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| 74HC3G07 | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.33 | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | μA |
| I _{LO} | output leakage current | V _I = V _{IH} ; V _O = V _{CC} or GND | - | - | ±5.0 | - | ±10 | μA |
| I _{CC} | supply current | per input pin; V _{CC} = 6.0 V; V _I = V _{CC} or GND; I _O = 0 A | - | - | 10 | - | 20 | μA |
| C _I | input capacitance | | - | 1.5 | - | - | - | pF |
| 74HCT3G07 | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1.0 | - | ±1.0 | μA |
| I _{LO} | output leakage current | V _I = V _{IH} ; V _O = V _{CC} or GND | - | - | ±5.0 | - | ±10 | μA |
| I _{CC} | supply current | per input pin; V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A | - | - | 10 | - | 20 | μA |
| ΔI _{CC} | additional supply current | per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A | - | - | 375 | - | 410 | μA |
| C _I | input capacitance | | - | 1.5 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|------------------------------------|---|------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| 74HC3G07 | | | | | | | | |
| t _{PZL} | OFF-state to LOW propagation delay | nA to nY; see Fig. 5 | | | | | | |
| | | V _{CC} = 2.0 V | - | 25 | 95 | - | 125 | ns |
| | | V _{CC} = 4.5 V | - | 9 | 19 | - | 25 | ns |
| | | V _{CC} = 6.0 V | - | 7 | 16 | - | 20 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | nA to nY; see Fig. 5 | | | | | | |
| | | V _{CC} = 2.0 V | - | 25 | 95 | - | 125 | ns |
| | | V _{CC} = 4.5 V | - | 11 | 23 | - | 30 | ns |
| | | V _{CC} = 6.0 V | - | 10 | 23 | - | 26 | ns |
| t _{THL} | HIGH to LOW output transition time | nY; see Fig. 5 | | | | | | |
| | | V _{CC} = 2.0 V | - | 18 | 95 | - | 125 | ns |
| | | V _{CC} = 4.5 V | - | 6 | 19 | - | 25 | ns |
| | | V _{CC} = 6.0 V | - | 5 | 16 | - | 20 | ns |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} [2] | - | 4 | - | - | - | pF |
| 74HCT3G07 | | | | | | | | |
| t _{PZL} | OFF-state to LOW propagation delay | nA to nY; V _{CC} = 4.5 V; see Fig. 5 | - | 11 | 27 | - | 32 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | nA to nY; V _{CC} = 4.5 V; see Fig. 5 | - | 10 | 26 | - | 31 | ns |
| t _{THL} | HIGH to LOW output transition time | nY; V _{CC} = 4.5 V; see Fig. 5 | - | 6 | 19 | - | 22 | ns |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} - 1.5 V [2] | - | 4 | | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveforms and test circuit

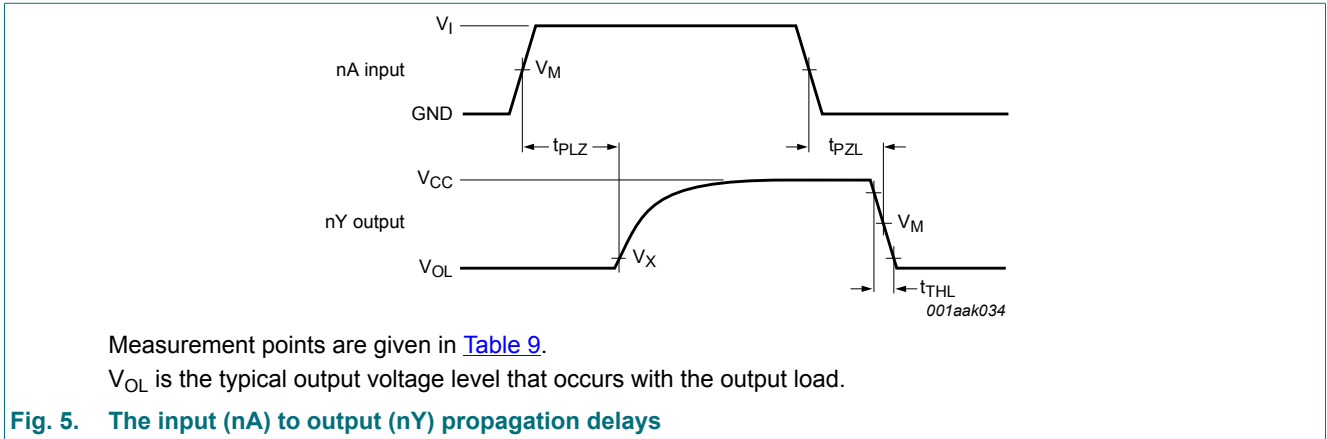


Table 9. Measurement points

| Type | Input | Output | |
|-----------|---------------------|---------------------|---------------------|
| | V_M | V_M | V_X |
| 74HC3G07 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $0.1 \times V_{CC}$ |
| 74HCT3G07 | 1.3 V | 1.3 V | $0.1 \times V_{CC}$ |

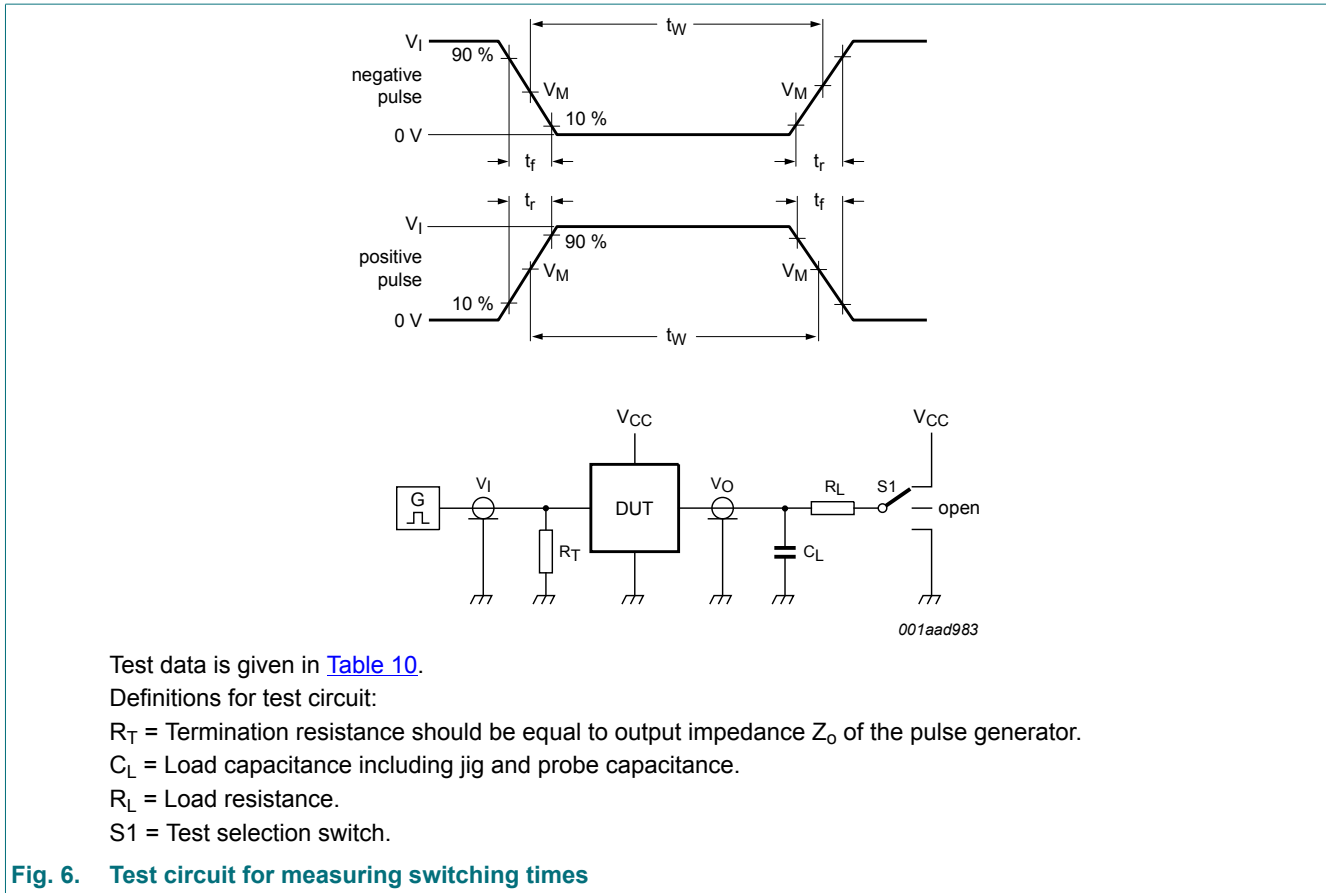


Fig. 6. Test circuit for measuring switching times

Table 10. Test data

| Type | Input | | Load | | S1 position |
|-----------|-----------------|-------------|-------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{pZL}, t_{pLZ} |
| 74HC3G07 | GND to V_{CC} | ≤ 6 ns | 50 pF | 1 k Ω | V_{CC} |
| 74HCT3G07 | GND to 3 V | ≤ 6 ns | 50 pF | 1 k Ω | V_{CC} |

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--|-----------------------|---------------|------------------|
| 74HC_HCT3G07 v.5 | 20190124 | Product data sheet | - | 74HC_HCT3G07 v.4 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC3G07GD and 74HCT3G07GD (SOT996-2) removed. Package outline drawing SOT765-1 (VSSOP8) updated. | | | |
| 74HC_HCT3G07 v.4 | 20131216 | Product data sheet | - | 74HC_HCT3G07 v.3 |
| Modifications: | <ul style="list-style-type: none"> Features and benefits updated (errata). | | | |
| 74HC_HCT3G07 v.3 | 20130814 | Product data sheet | - | 74HC_HCT3G07 v.2 |
| Modifications: | <ul style="list-style-type: none"> For type numbers 74HC3G07GD and 74HCT3G07GD XSON8U has changed to XSON8. | | | |
| 74HC_HCT3G07 v.2 | 20090512 | Product data sheet | - | 74HC_HCT3G07 v.1 |
| 74HC_HCT3G07 v.1 | 20031015 | Product specification | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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