

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4516** Binary up/down counter

Product specification  
File under Integrated Circuits, IC06

December 1990

## Binary up/down counter

## 74HC/HCT4516

## FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4516 are high-speed Si-gate CMOS devices and are pin compatible with the "4516" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4516 are edge-triggered synchronous up/down 4-bit binary counters with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input ( $\overline{CE}$ ), an asynchronous active HIGH

parallel load input (PL), four parallel inputs (D<sub>0</sub> to D<sub>3</sub>), four parallel outputs (Q<sub>0</sub> to Q<sub>3</sub>), an active LOW terminal count output ( $\overline{TC}$ ), and an overriding asynchronous master reset input (MR).

Information on D<sub>0</sub> to D<sub>3</sub> is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. When PL and  $\overline{CE}$  are LOW, the counter changes on the LOW-to-HIGH transition of CP. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up,  $\overline{TC}$  is LOW when Q<sub>0</sub> to Q<sub>3</sub> are HIGH and  $\overline{CE}$  is LOW. When counting down,  $\overline{TC}$  is LOW when Q<sub>0</sub> to Q<sub>3</sub> and  $\overline{CE}$  are LOW. A HIGH on MR resets the counter (Q<sub>0</sub> to Q<sub>3</sub> = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{(UP/DN) \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 + (UP/DN) \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3}\}$$

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	19	19	ns
f <sub>max</sub>	maximum clock frequency		45	57	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	59	61	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION

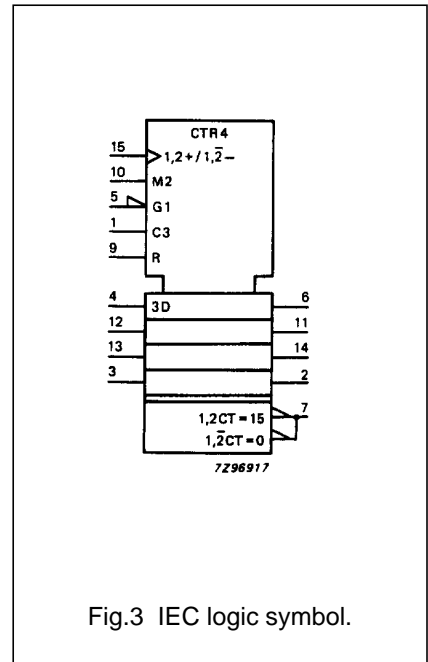
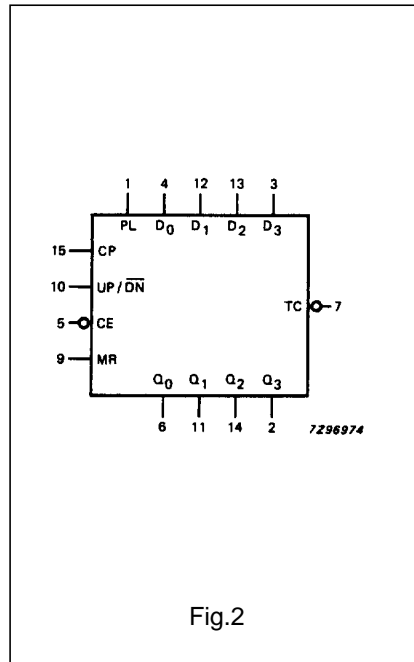
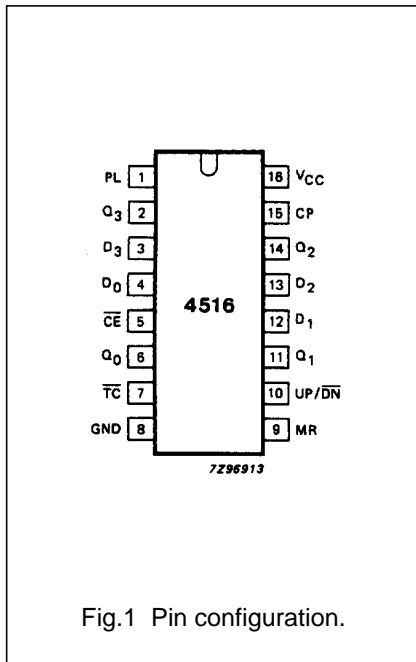
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Binary up/down counter

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D <sub>0</sub> to D <sub>3</sub>	parallel inputs
5	$\overline{CE}$	count enable input (active LOW)
6, 11, 14, 2	Q <sub>0</sub> to Q <sub>3</sub>	parallel outputs
7	$\overline{TC}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/ $\overline{DN}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V <sub>CC</sub>	positive supply voltage



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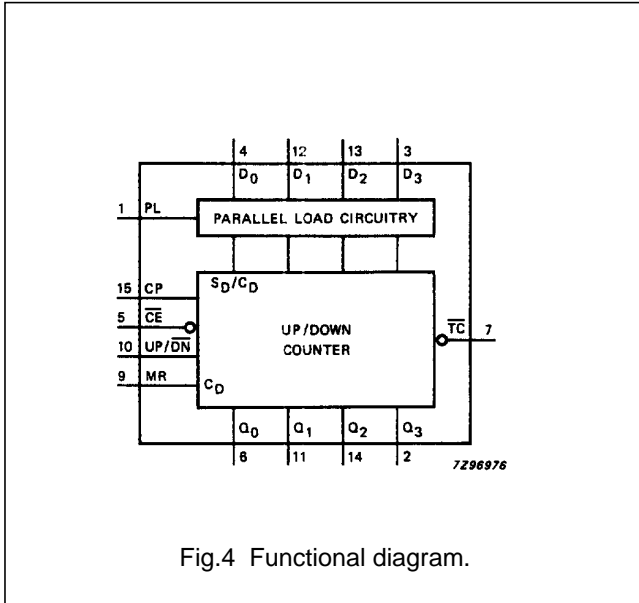


Fig.4 Functional diagram.

FUNCTION TABLE

MR	PL	UP/DN	CE	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH clock transition

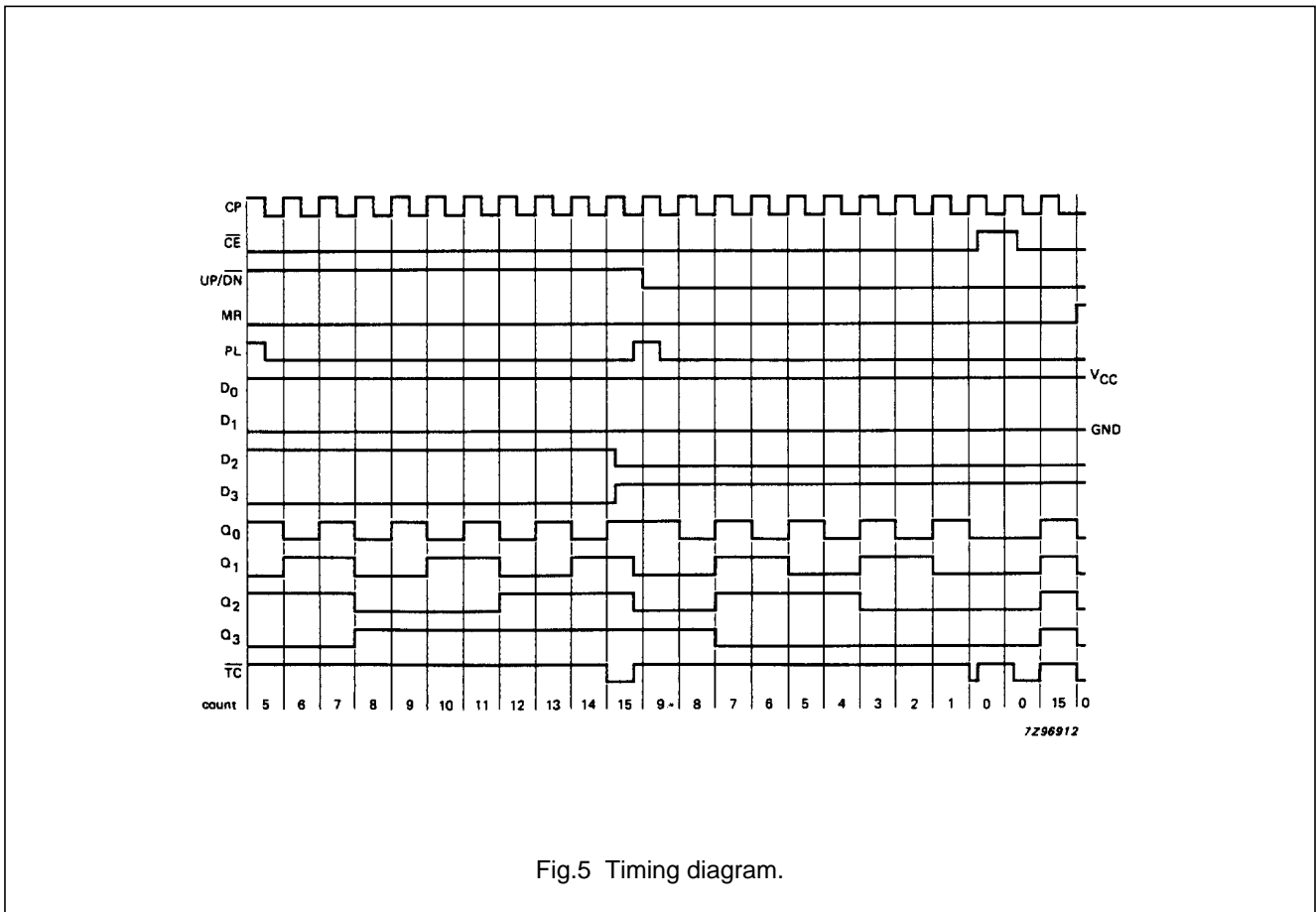
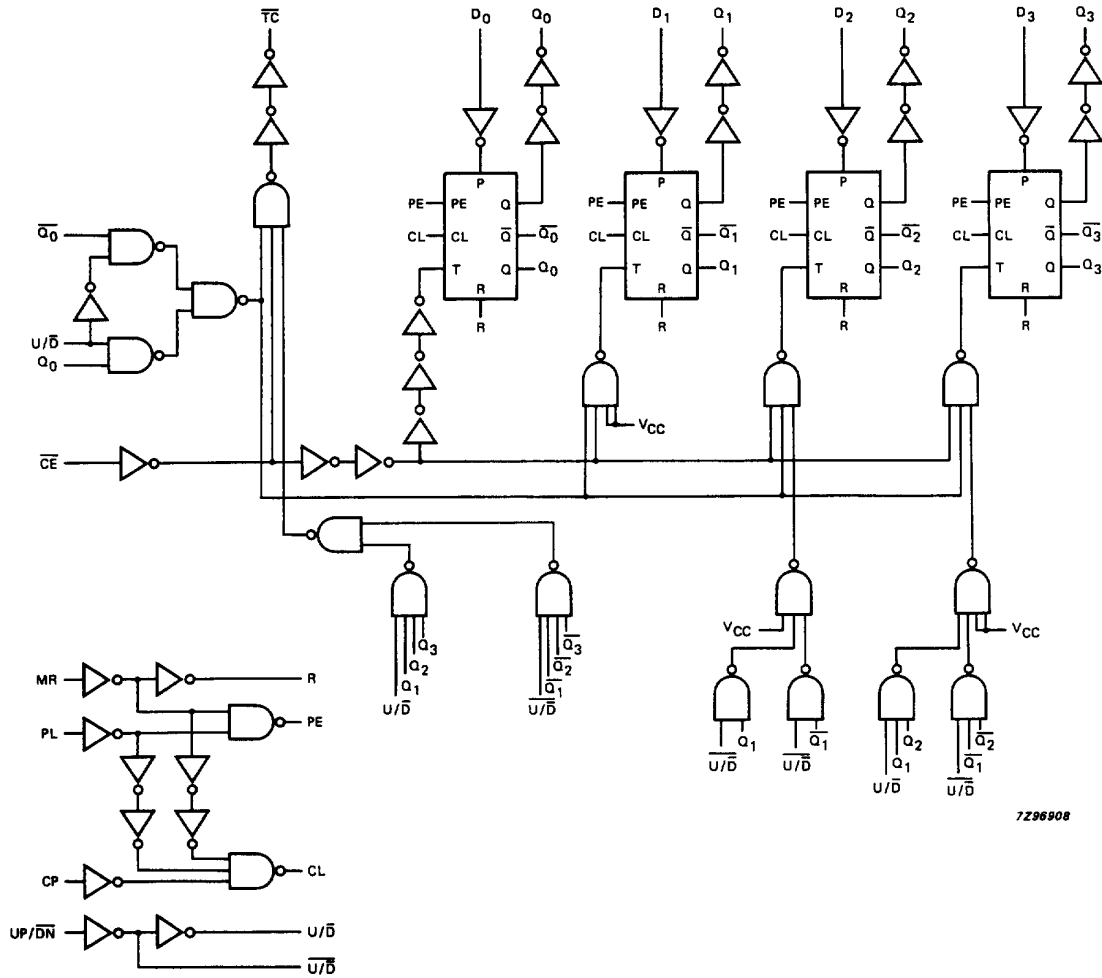


Fig.5 Timing diagram.

Binary up/down counter

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Fig.6 Logic diagram.

## Binary up/down counter

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to+85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.10
t <sub>PLH</sub> / t <sub>PHL</sub>	propagation delay PL to Q <sub>n</sub>		83 30 24	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{TC}$		74 27 22	260 52 44		325 65 55		395 78 66	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CE}$ to $\overline{TC}$		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t <sub>PLH</sub>	propagation delay MR to $\overline{TC}$		69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig.10
t <sub>PLH</sub> / t <sub>PHL</sub>	propagation delay PL to $\overline{TC}$		91 33 26	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.9
t <sub>TLH</sub> / t <sub>THL</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t <sub>w</sub>	clock pulse width CP, $\overline{CE}$ HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	parallel load pulse width HIGH	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.10
t <sub>w</sub>	master reset pulse width HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.10

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to+85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>rem</sub>	removal time MR to CP	80 16 14	28 10 8		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.10	
t <sub>rem</sub>	removal time PL to CP	80 16 14	25 9 7		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.10	
t <sub>su</sub>	set-up time UP/DN to CP	100 20 17	30 11 9		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.8	
t <sub>su</sub>	set-up time $\overline{CE}$ to CP	100 20 17	19 7 6		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.8	
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	100 20 17	17 6 5		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.11	
t <sub>h</sub>	hold time $\overline{CE}$ to CP	5 5 5	0 0 0		5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig.8	
t <sub>h</sub>	hold time D <sub>n</sub> to PL	3 3 3	-6 -2 -2		3 3 3		3 3 3	ns	2.0 4.5 6.0	Fig.11	
t <sub>h</sub>	hold time UP/DN to CP	0 0 0	-19 -7 -6		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig.8	
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	16 49 58		4.8 24 28		4.0 20 24	MHz	2.0 4.5 6.0	Fig.7	

## Binary up/down counter

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$D_n$	0.75
PL, $\overline{CE}$	1.00
UP/DN	1.00
CP	1.25
MR	1.50



## Binary up/down counter

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## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS	
		74HCT								$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$		28	50		63		75	ns	4.5	Fig.7
$t_{PHL}$	propagation delay MR to $Q_n$		24	42		53		63	ns	4.5	Fig.10
$t_{PLH}/t_{PHL}$	propagation delay PL to $Q_n$		32	53		66		80	ns	4.5	Fig.9
$t_{PHL}/t_{PLH}$	propagation delay CP to TC		29	58		73		87	ns	4.5	Fig.7
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CE}$ to $\overline{TC}$		18	31		39		47	ns	4.5	Fig.8
$t_{PLH}$	propagation delay MR to $\overline{TC}$		31	50		63		75	ns	4.5	Fig.10
$t_{PLH}/t_{PHL}$	propagation delay PL to $\overline{TC}$		34	68		85		102	ns	4.5	Fig.9
$t_{TLH}/t_{THL}$	output transition time		7	15		19		22	ns	4.5	Fig.9
$t_W$	clock pulse width CP, $\overline{CE}$ HIGH or LOW	16	9		20		24		ns	4.5	Fig.7
$t_W$	parallel load pulse width HIGH	16	8		20		24		ns	4.5	Fig.10
$t_W$	master rest pulse width HIGH	20	5		25		30		ns	4.5	Fig.10
$t_{rem}$	removal time MR to CP	23	14		29		35		ns	4.5	Fig.10
$t_{rem}$	removal time PL to CP	17	10		21		26		ns	4.5	Fig.10
$t_{su}$	set-up time UP/DN to CP	20	11		25		30		ns	4.5	Fig.8
$t_{su}$	set-up time $\overline{CE}$ to CP	20	9		25		30		ns	4.5	Fig.8
$t_{su}$	set-up time $D_n$ to PL	20	9		25		30		ns	4.5	Fig.11
$t_h$	hold time $\overline{CE}$ to CP	10	9		13		15		ns	4.5	Fig.8

## Binary up/down counter

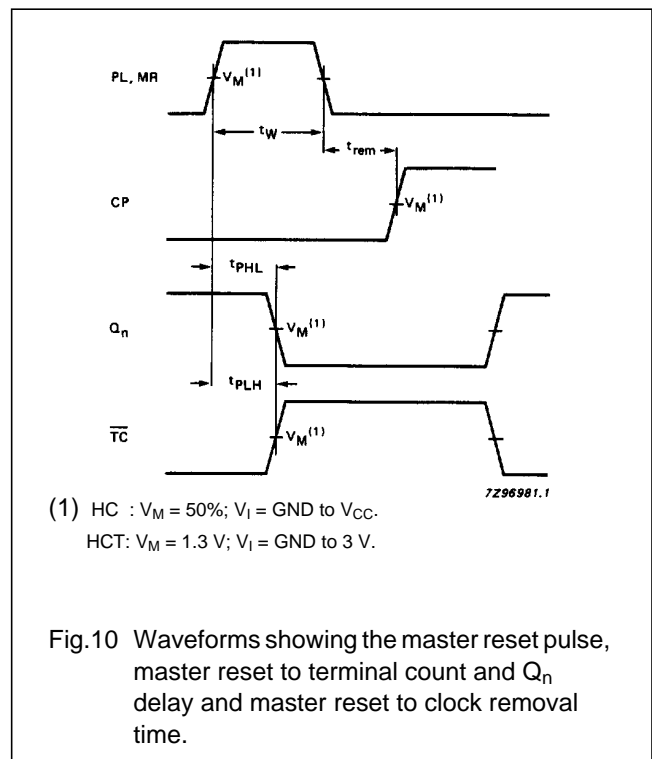
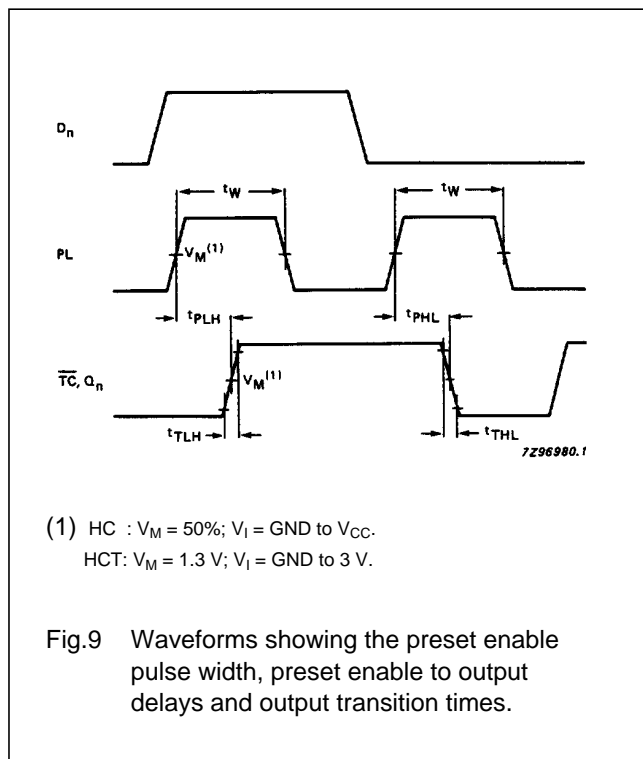
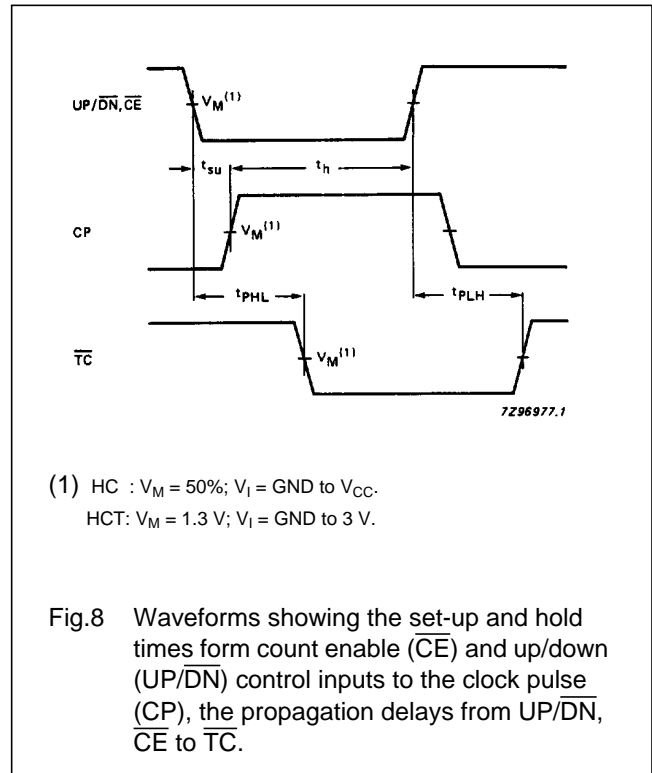
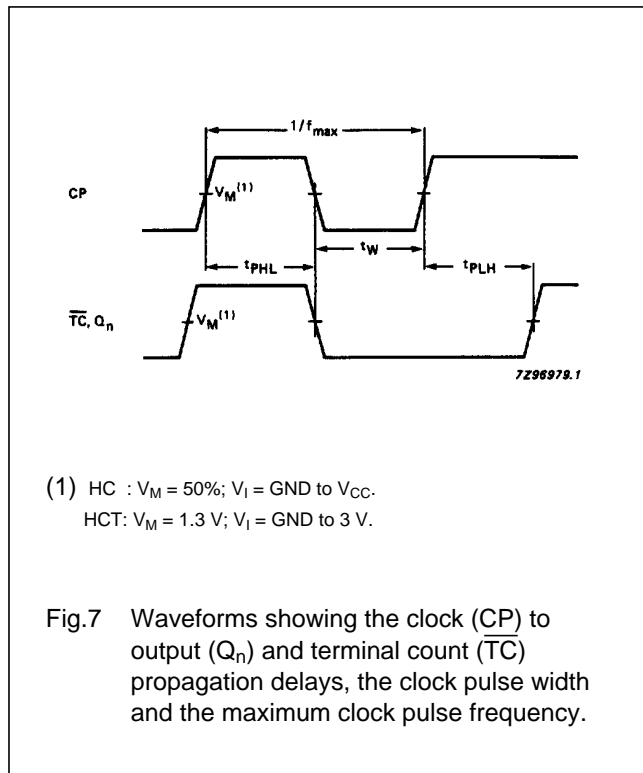
## 74HC/HCT4516

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>h</sub>	hold time D <sub>n</sub> to PL	5	-6		5		5		ns	4.5	Fig.11	
t <sub>h</sub>	hold time UP/ $\overline{\text{DN}}$ to CP	0	-5		0		0		ns	4.5	Fig.8	
f <sub>max</sub>	maximum clock pulse frequency	30	52		24		20		MHz	4.5	Fig.7	

Binary up/down counter

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AC WAVEFORMS



Binary up/down counter

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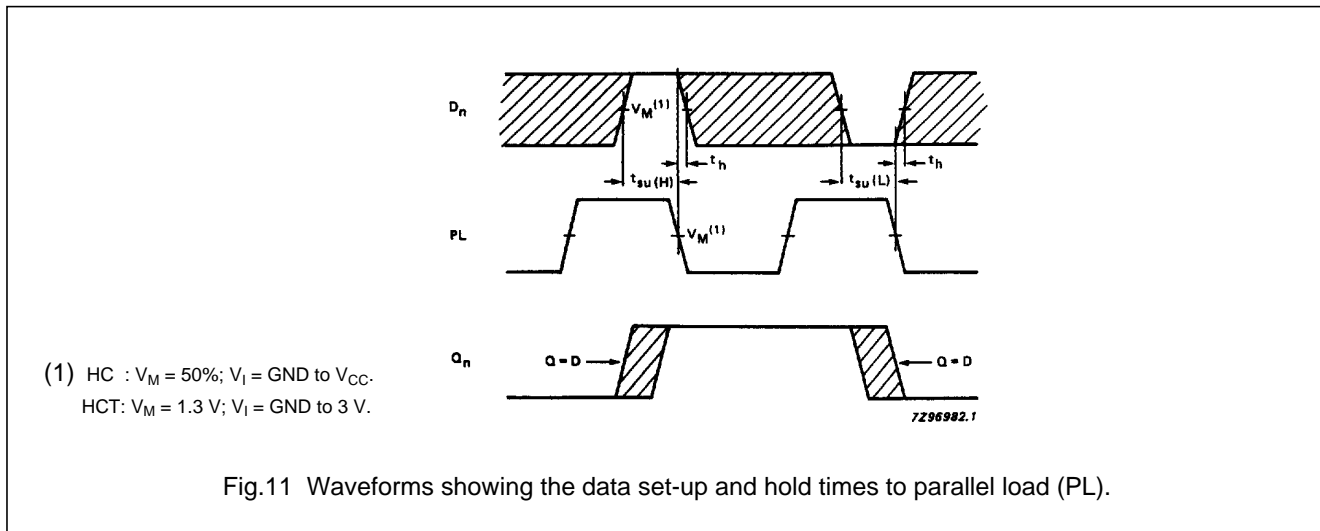
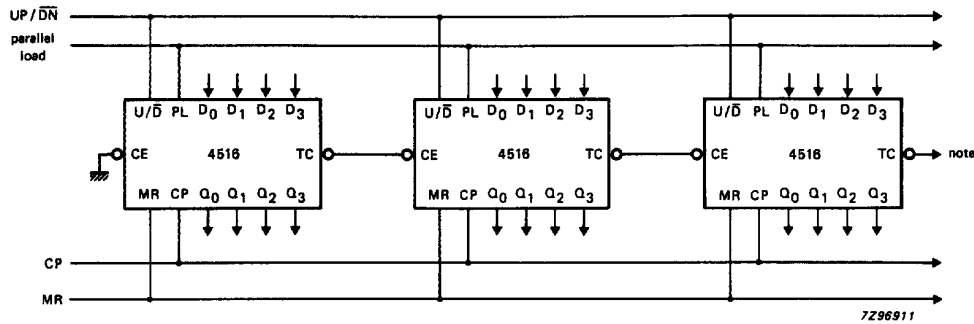


Fig.11 Waveforms showing the data set-up and hold times to parallel load (PL).

Binary up/down counter

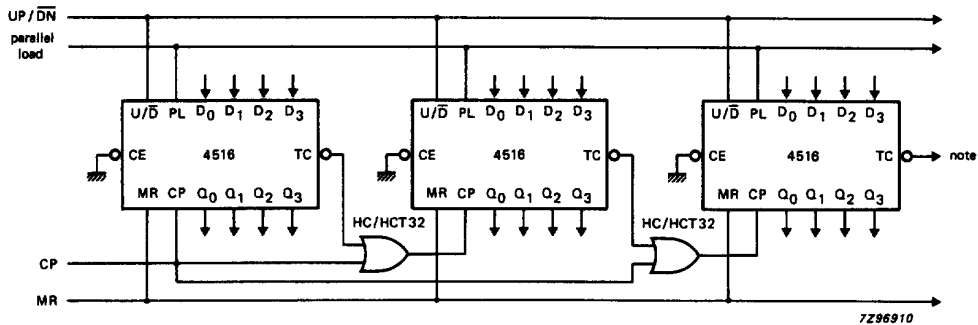
74HC/HCT4516

APPLICATION INFORMATION



Terminal count ( $\overline{TC}$ ) lines at the 2nd, 3rd, etc. Stages may have a negative-going glitch pulse resulting from differential delays of different 4516s. These negative-going glitches do not affect proper 4516 operation. However, if the terminal count signals are used to trigger other edge-sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.

Fig.12 Cascading counter packages (parallel clocking).



Ripple clocking mode: the  $\overline{UP/DN}$  control can be changed at any count. The only restriction on changing the  $\overline{UP/DN}$  control is that the clock input to the first counting stage must be "HIGH". For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and TC is connected directly to the CP input of the next stage with  $\overline{CE}$  grounded.

Fig.13 Cascading counter packages (ripple clocking).

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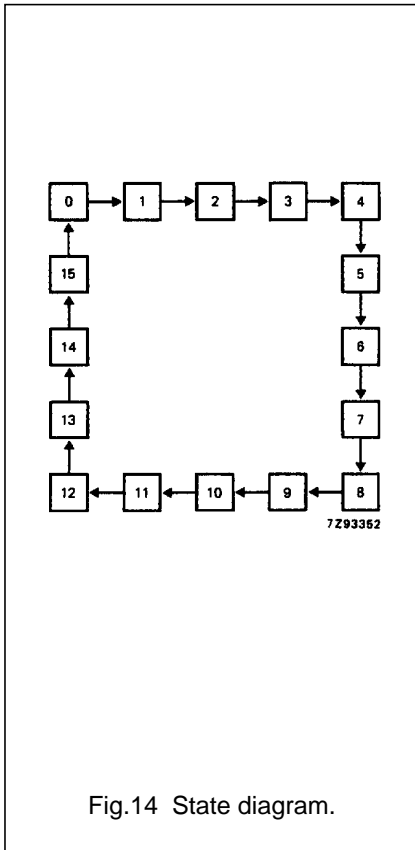
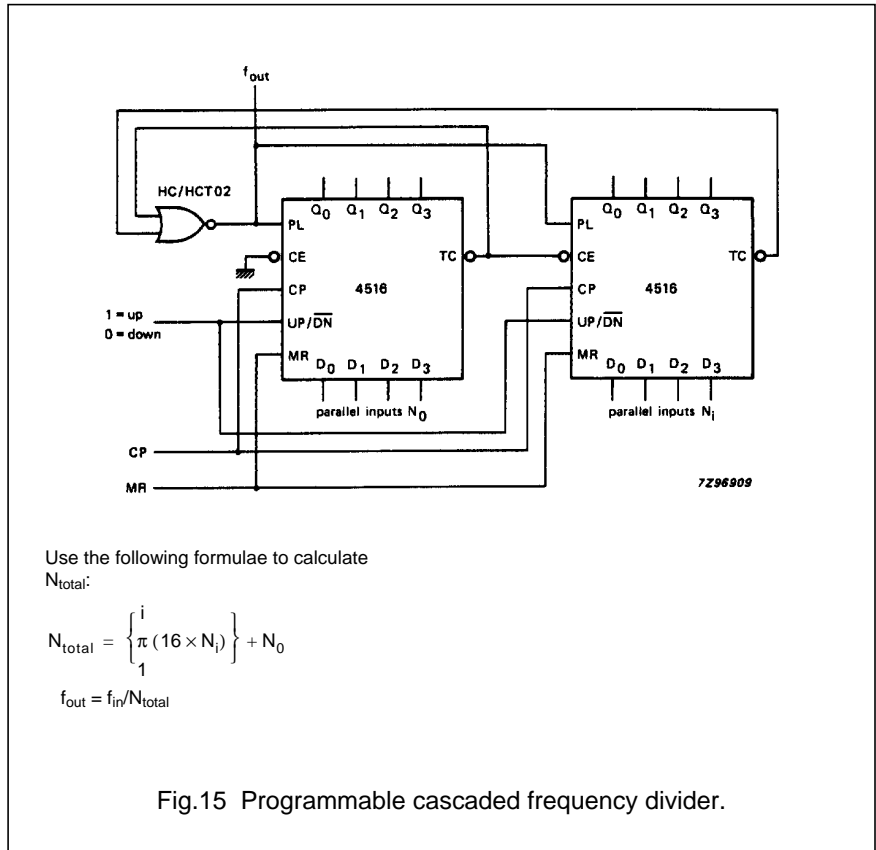


Fig.14 State diagram.



Use the following formulae to calculate  $N_{total}$ :

$$N_{total} = \left\{ \pi (16 \times N_i) \right\} + N_0$$

$$f_{out} = f_{in} / N_{total}$$

Fig.15 Programmable cascaded frequency divider.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

parallel inputs				count-up	count-down
D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	n	n
0	0	0	0	15	(1)
0	0	0	1	14	1
0	0	1	0	13	2
0	0	1	1	12	3
0	1	0	0	11	4
0	1	0	1	10	5
0	1	1	0	9	6
0	1	1	1	8	7
1	0	0	0	7	8
1	0	0	1	6	9
1	0	1	0	5	10
1	0	1	1	4	11
1	1	0	0	3	12
1	1	0	1	2	13
1	1	1	0	1	14
1	1	1	1	(1)	15

Note

- no count;  $f_{out}$  is HIGH.