Features

- 8-bit serial input
- 8-bit serial or parallel output
- Tri-state output register
- Shift register with direct clear
- Shift output frequency of 100MHz (typical)
- ESD protection function

Applications

- Serial-to-parallel conversion
- Remote control memory retention device

Description

- The 74HC595D is a high-speed Silicon Gate CMOS device, with pin compatibility with Low-Power Schottky TTL circuits(LSTTL). It complies with JEDEC standard no.7A. The 74HC595D consists of an 8-stage serial shift register with a storage register and tri-state outputs. Theshift register and the storage register each have separate clocks.

- Data is shifted on the rising edge of the shift clock (SH_CP), while transfer from the shift register to the storage register occurs on the rising edge of the storage clock (ST_CP). If both clocks are connected together, the dataon the shift register always leads the data on the storage register by one clock pulse.

- The shift register has a serial input (DS) and a serial output for cascading (Q7'), along with an asynchronous reset input (active low). The storage register features an 8-bit parallel bus driver output with tri-state outputs. When the output enable input (OE) is low, the outputs are in normal operation; conversely, when OE is high,the outputs are in a high-impedance state.

Function Table

Input					Output		Function
SH_CP	ST_CP	$\overline{OE}$	$\overline{MR}$	DS	Q7′	Qn	
×	×	L	L	×	L	n.c	When $\overline{MR}$ is low, it resets only the shift register.
×	↑	L	L	×	L	L	The shift register transfers empty values to the storage register
×	×	H	L	×	L	Z	The shift register is cleared, and the parallel outputs are in a high-impedance state.
↑	×	L	H	H	Q6′	n.c	A logic high level is transferred to the 0^{th} stage of the shift register from the input; all shift register data is sequentially shifted down under the control of the shift clock.
×	↑	L	H	×	n.c,	Qn′	All data in the shift registers is transferred to the corresponding storage registers under the control of the storage clock.
↑	↑	L	H	×	Q6′	Qn′	The shift register sequentially shifts data backward; simultaneously, it transfers the previous state to the corresponding storage register and output.

Note：

H=High level　　L=Low level　　↓ Falling edge　　↑ Rising edge

Z=High-Z (high-impedance) state　　n.c.=No change　　X=unrelated quantity

Pin Description

Pin	Symbol	Description
1	Q1	parallel output terminals
2	Q2	parallel output terminals
3	Q3	parallel output terminals
4	Q4	parallel output terminals
5	Q5	parallel output terminals
6	Q6	parallel output terminals
7	Q7	parallel output terminals
8	GND	ground（0V）
9	Q7′	serial output terminals
10	$\overline{MR}$	master reset (active low)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	output enable (active low)
14	DS	serial input terminal
15	Q0	parallel output terminal
16	V_{CC}	power supply

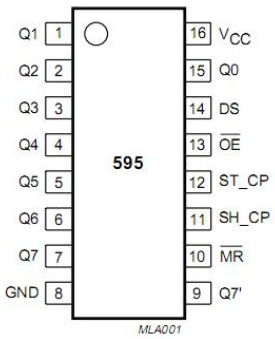


Fig.1 Pinout For DIP16, S016 and (T)SSOP16 Packages

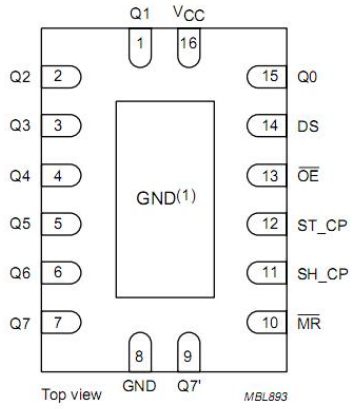


Fig.2 DHVQFN16 Pinout Diagram

Functional Diagram

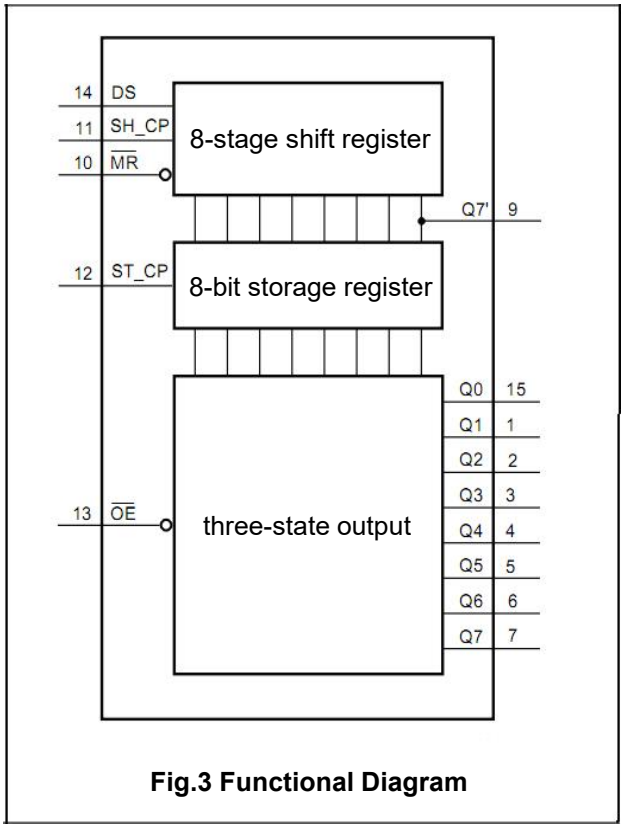


Fig.3 Functional Diagram

Logic Diagram

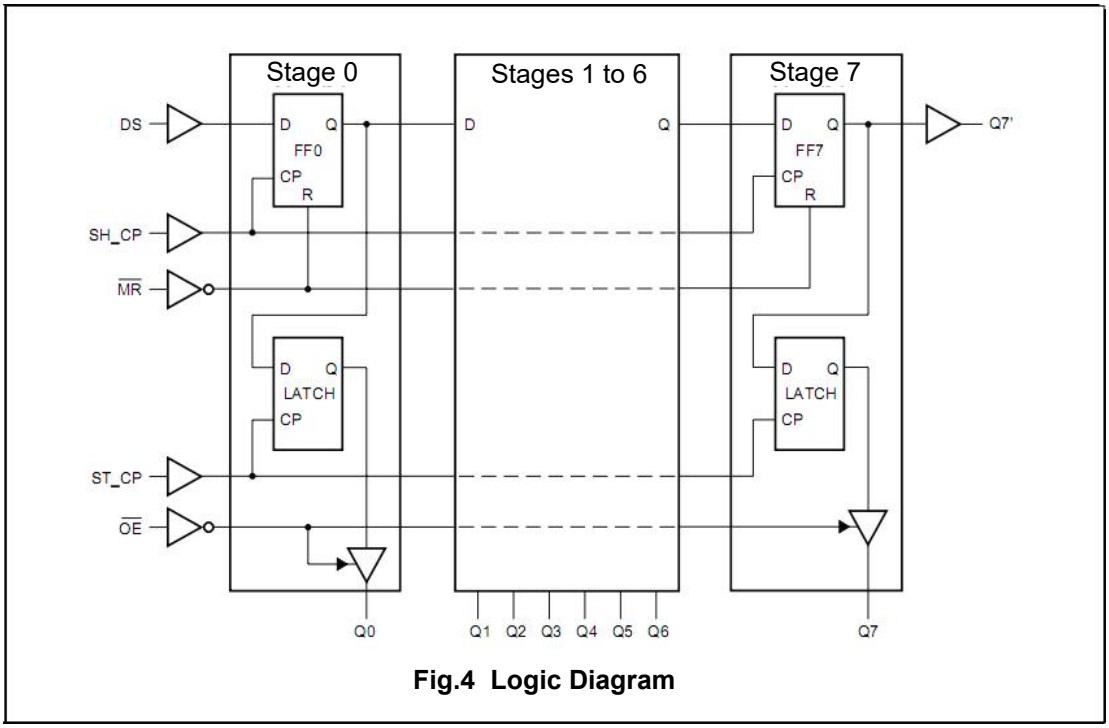


Fig.4 Logic Diagram

Timing Diagram

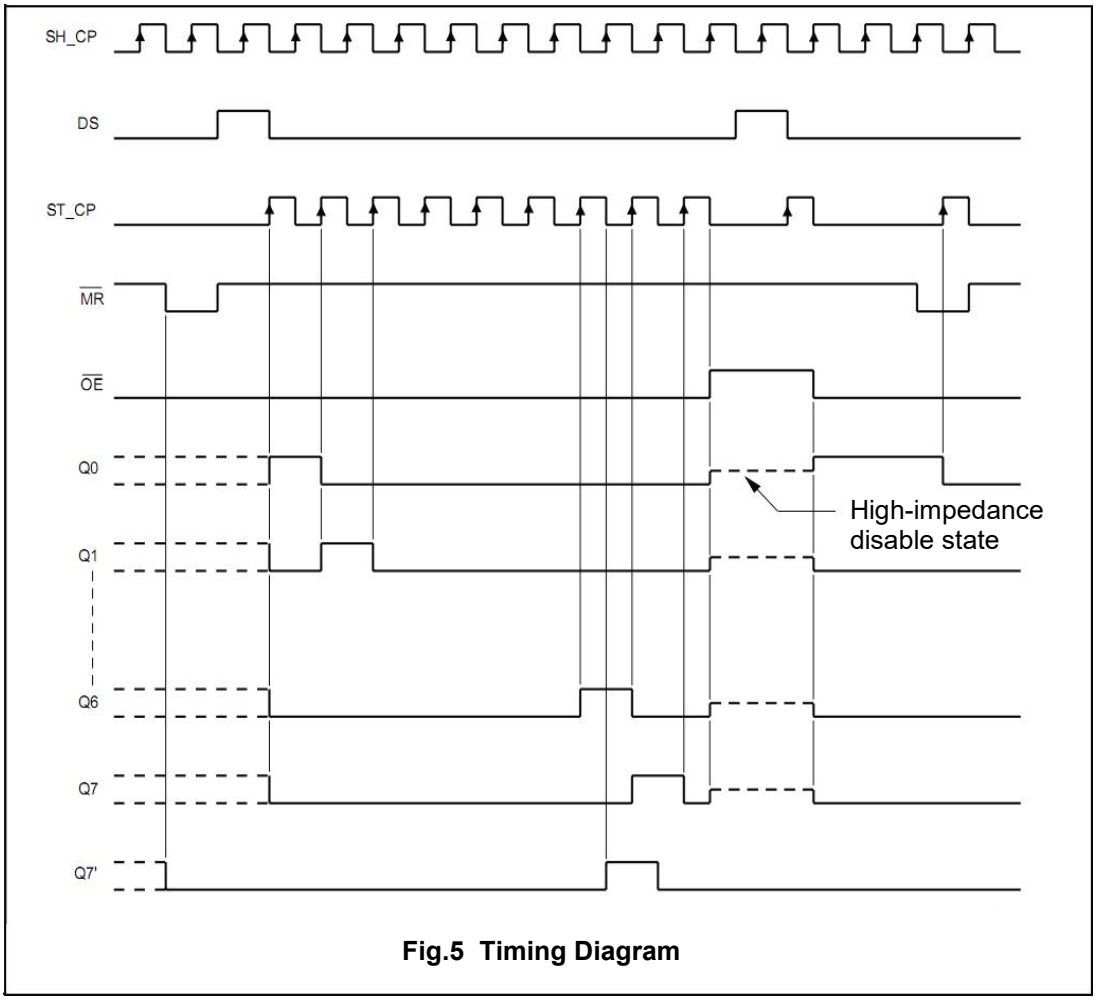


Fig.5 Timing Diagram

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	power supply	—	-0.5	7.0	V
I_{IK}	input diode current	V_I<-0.5V or V_I>V_{CC}+0.5V	—	±20	mA
I_{OK}	output diode current	V_O<-0.5V or V_O>V_{CC}+0.5V	—	±20	mA
I_O	output sourcing curren or sinking current	-0.5V<V_O<V_{CC}+0.5V	—		
		Q' standard output	—	±25	mA
		Q0~Q7 bus driver output	—	±35	mA
I_{CC},I_{GND}	V_{CC},GND current	—	—	±70	mA
T_{STG}	storage temperature	—	-65	+150	℃
P_{TOT}	power dissipation	T_{amb}= -40 to 125℃	—	500	mW

DC Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
		Other	V_{CC}（V）				
Ambient temperature: -40 to +125°C; all typical values are measured at 25°C.							
V_{IH}	high-level input voltage		2.0	1.5	1.2	—	V
			4.5	3.15	2.4	—	V
			6.0	4.2	3.2	—	V
V_{IL}	low-level input voltage		2.0	—	0.8	0.5	V
			4.5	—	2.1	1.35	V
			6.0	—	2.8	1.8	V
V_{OH}	high-level output voltage	V_I=V_{IH} or V_{IL}					
		all output terminals Io=-20uA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	V V V
		Q7′ standard output Io=-4.0mA Io=-5.2mA	4.5 6.0	3.84 5.34	4.32 5.81	— —	V V
		Qn bus driver output Io=-6.0mA Io=-7.8mA	4.5 6.0	3.84 5.34	4.32 5.81	— —	V V
V_{OL}	low-level output voltage	V_I=V_{IH} or V_{IL}					
		all output terminals Io=20uA	2.0 4.5 6.0	— — —	0 0 0	0.1 0.1 0.1	V V V
		Q7′ standard output Io=-4.0mA Io=-5.2mA	4.5 6.0	— —	0.15 0.16	0.33 0.33	V V
		Qn bus driver output Io=-6.0mA Io=-7.8mA	4.5 6.0	— —	0.16 0.16	0.33 0.33	V V
I_{LI}	peak input current	V_I=V_C or GND	6.0	—	—	±1.0	uA
I_{OZ}	output tri-state high-impedance current	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND	6.0	—	—	±5.0	uA
I_{CC}	static power supply current	V_I=V_{CC} or GND I_O=0	6.0	—	—	80	uA

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
		Other	V_{CC}（V）				
Ambient temperature : -40℃ to +125℃							
V_{IH}	high-level input voltage		2.0	1.5	—	—	V
			4.5	3.15	—	—	V
			6.0	4.2	—	—	V
V_{IL}	low-level input voltage		2.0	—	—	0.5	V
			4.5	—	—	1.35	V
			6.0	—	—	1.8	V
V_{OH}	high-level output voltage	V_I=V_{IH} or V_{IL}					
		all output terminals I_O=-20uA	2.0 4.5 6.0	1.9 4.4 5.9	— — —	— — —	V V V
		Q7′ standard output I_O=-4.0mA I_O=-5.2mA	4.5 6.0	3.7 5.2	— —	— —	VV
		Qn bus driver output I_O=-6.0mA I_O=-7.8mA	4.5 6.0	3.7 5.2	— —	— —	VV
V_{OL}	low-level output voltage	V_I=V_{IH} or V_{IL}					
		all output terminals I_O=20uA	4.5	—	—	0.1	V
		Q7′ standard output I_O=-4.0mA	4.5	—	—	0.4	V
		Qn bus driver output I_O=-6.0mA	4.5	—	—	0.4	V
I_{LI}	peak input current	V_I=V_{CC} or GND	5.5	—	—	±1.0	uA
I_{OZ}	output tri-state high-impedance current	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND	5.5	—	—	±10.0	uA
I_{CC}	static power supply current	V_I=V_{CC} or GND I_O=0	5.5	—	—	160	uA

AC Electrical Characteristics

GND=0V；t_r=t_f=6ns；C_L=50pF

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
		Waveform	V_{CC}（V）				
Ambient temperature : 25℃							
t_{PHL} /t_{PLH}	transmission delay time from SH_CP to Q7'	see fig.6	2.0	—	52	160	ns
			4.5	—	19	32	ns
			6.0	—	15	27	ns
	transmission delay time from ST_CP to Qn	see fig.7	2.0	—	55	175	ns
			4.5	—	20	35	ns
			6.0	—	16	30	ns
t_{PHL}	transmission delay time from $\overline{MR}$ to Q7'	see fig.9	2.0	—	47	175	ns
			4.5	—	17	35	ns
			6.0	—	14	30	ns
t_{PZH}/t_{PZL}	transition time from high-impedance state to enabled output at Qn due to $\overline{OE}$	see fig.10	2.0	—	47	150	ns
			4.5	—	17	30	ns
			6.0	—	14	26	ns
t_{PHZ}/t_{PLZ}	transition time from enabled output to high-impedance state at Qn due to $\overline{OE}$	see fig.10	2.0	—	41	150	ns
			4.5	—	15	30	ns
			6.0	—	12	26	ns
t_W	shift clock pulse width(high level or low level)	see fig.6	2.0	75	17	—	ns
			4.5	15	6	—	ns
			6.0	13	5	—	ns
	storage clock pulse width (high level or low level)	see fig.7	2.0	75	11	—	ns
			4.5	15	4	—	ns
			6.0	13	3	—	ns
	master reset pulse width (low level)	see fig.9	2.0	75	17	—	ns
			4.5	15	6.0	—	ns
			6.0	13	5.0	—	ns
t_{su}	setup time from DS to SH_CP	see fig.8	2.0	50	11	—	ns
			4.5	10	4.0	—	ns
			6.0	9.0	3.0	—	ns
	setup time from SH_CP to ST_CP	see fig.7	2.0	75	22	—	ns
			4.5	15	8	—	ns
			6.0	13	7	—	ns
t_h	hold time from DS to SH_CP	see fig.8	2.0	+3	-6	—	ns
			4.5	+3	-2	—	ns
			6.0	+3	-2	—	ns

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
		Waveform	V_{CC}（V）				
t_{rem}	time for $\overline{MR}$ to reset SH_CP	see fig.9	2.0	+50	-19	—	ns
			4.5	+10	-7	—	ns
			6.0	+9	-6	—	ns
f_{max}	minimum clock pulse width for SH_CP or ST_CP	see fig.6 and fig.7	2.0	9	30	—	MHz
			4.5	30	91	—	MHz
			6.0	35	108	—	MHz
Ambient temperature: -40 to +85°C							
t_{PHL} /t_{PLH}	transmission delay time from SH_CP to Q7'	see fig.6	2.0	—	—	200	ns
			4.5	—	—	40	ns
			6.0	—	—	34	ns
	transmission delay time from ST_CP to Qn	see fig.7	2.0	—	—	220	ns
			4.5	—	—	44	ns
			6.0	—	—	37	ns
t_{PHL}	transmission delay time from $\overline{MR}$ to Q7'	see fig.9	2.0	—	—	220	ns
			4.5	—	—	44	ns
			6.0	—	—	37	ns
t_{PZH}/t_{PZL}	transition time from high-impedance state to enabled output at Qn due to $\overline{OE}$	see fig.10	2.0	—	—	190	ns
			4.5	—	—	38	ns
			6.0	—	—	33	ns
t_{PHZ}/t_{PLZ}	transition time from enabled output to high-impedance state at Qn due to $\overline{OE}$	see fig.10	2.0	—	—	190	ns
			4.5	—	—	38	ns
			6.0	—	—	33	ns
t_W	shift clock pulse width (high level or low level)	see fig.6	2.0	95	—	—	ns
			4.5	19	—	—	ns
			6.0	16	—	—	ns
	storage clock pulse width (high level or low level)	see fig.7	2.0	95	—	—	ns
			4.5	19	—	—	ns
			6.0	16	—	—	ns
	master reset pulse width (low level)	see fig.9	2.0	95	—	—	ns
			4.5	19	—	—	ns
			6.0	16	—	—	ns
t_{su}	setup time from DS to SH_CP	see fig.8	2.0	65	—	—	ns
			4.5	13	—	—	ns
			6.0	11	—	—	ns
	setup time from SH_CP to ST_CP	see fig.7	2.0	95	—	—	ns
			4.5	19	—	—	ns
			6.0	16	—	—	ns

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
		Waveform	V_{CC}（V）				
t_h	hold time from DS to SH_CP	see fig.8	2.0	3	—	—	ns
			4.5	3	—	—	ns
			6.0	3	—	—	ns
t_{rem}	time for $\overline{MR}$ to reset SH_CP	see fig.9	2.0	65	—	—	ns
			4.5	13	—	—	ns
			6.0	11	—	—	ns
f_{max}	minimum clock pulse width for SH_CP or ST_CP	see fig.6 and fig.7	2.0	4.8	—	—	MHz
			4.5	24	—	—	MHz
			6.0	28	—	—	MHz
Ambient temperature: -40℃ to +125℃							
t_{PHL}/t_{PLH}	transmission delay time from SH_CP to Q7'	see fig.6	2.0	—	—	240	ns
			4.5	—	—	48	ns
			6.0	—	—	41	ns
	transmission delay time from ST_CP to Qn	see fig.7	2.0	—	—	265	ns
			4.5	—	—	53	ns
			6.0	—	—	45	ns
t_{PHL}	transmission delay time from MR to Q7'	see fig.9	2.0	—	—	265	ns
			4.5	—	—	53	ns
			6.0	—	—	45	ns
t_{PZH}/t_{PZL}	Transition time from high-impedance state to enabled output at Qn due to $\overline{OE}$	see fig.10	2.0	—	—	225	ns
			4.5	—	—	45	ns
			6.0	—	—	35	ns
t_{PHZ}/t_{PLZ}	transition time from enabled out to high-impedance state at Qn due to $\overline{OE}$	see fig.10	2.0	—	—	225	ns
			4.5	—	—	45	ns
			6.0	—	—	35	ns
t_W	Shift clock pulse width (high level or low level)	see fig.6	2.0	110	—	—	ns
			4.5	22	—	—	ns
			6.0	19	—	—	ns
	storage clock pulse width (high level or low level)	see fig.7	2.0	110	—	—	ns
			4.5	22	—	—	ns
			6.0	19	—	—	ns
	master reset pulse width (low level)	see fig.9	2.0	110	—	—	ns
			4.5	22	—	—	ns
			6.0	19	—	—	ns
t_{su}	setup time from DS to SH_CP	see fig.8	2.0	75	—	—	ns
			4.5	15	—	—	ns
			6.0	13	—	—	ns

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
		Waveform	V_{CC}（V）				
tsu	setup time from SH_CP to ST_CP	see fig.7	2.0	110	—	—	ns
			4.5	22	—	—	ns
			6.0	19	—	—	ns
th	hold time from DS to SH_CP	see fig.8	2.0	3	—	—	ns
			4.5	3	—	—	ns
			6.0	3	—	—	ns
trem	time for $\overline{MR}$ to reset SH_CP	see fig.9	2.0	75	—	—	ns
			4.5	15	—	—	ns
			6.0	13	—	—	ns
fmax	minimum clock pulse width for SH_CP or ST_CP	see fig.6 and fig.7	2.0	4	—	—	MHz
			4.5	20	—	—	MHz
			6.0	24	—	—	MHz

AC Waveform

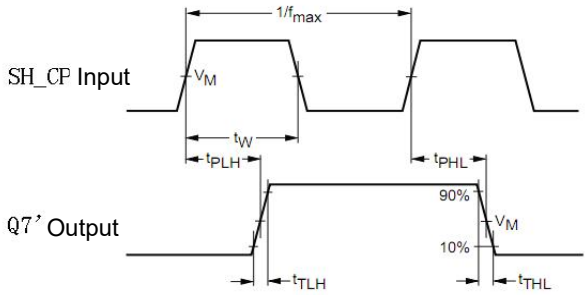


Fig.6 The diagram illustrates the propagation delay time from the shift clock (SH_CP) to theoutput (Q7'), shift clock pulse width, and maximum shift clock frequency.

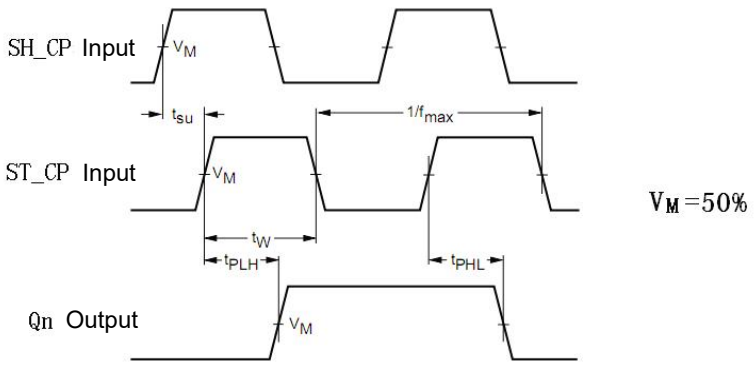
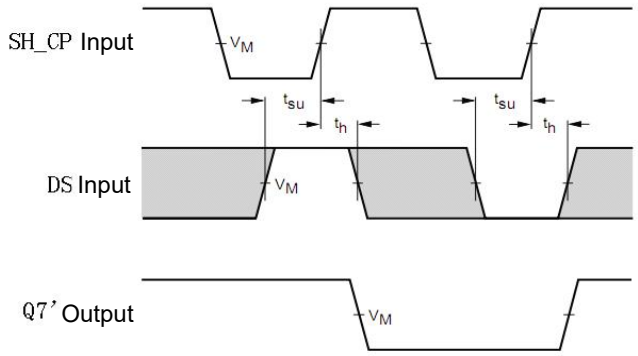


Fig.7 The diagram shows the propagation delay time from the storage clock (st_cp) to theoutput (qn), the storage clock pulse width, and the setup time from the shift clock to the storage clock.



The shaded area indicates that the input signal has no effect on the output during this period.

Fig.8 The Diagram Shows The Setup And Hold Times For DS Input.

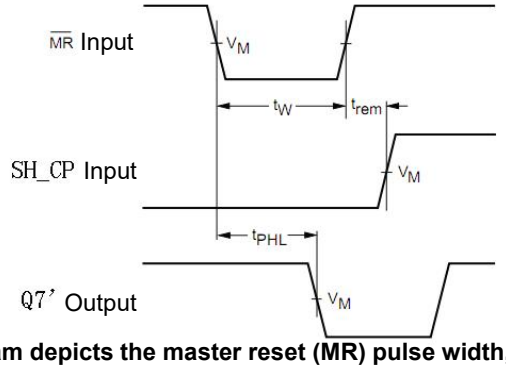


Fig.9 The diagram depicts the master reset (MR) pulse width, the propagation delay time from MR to the output (Q7'), and the reset time from MR to the shift clock (SH_CP).

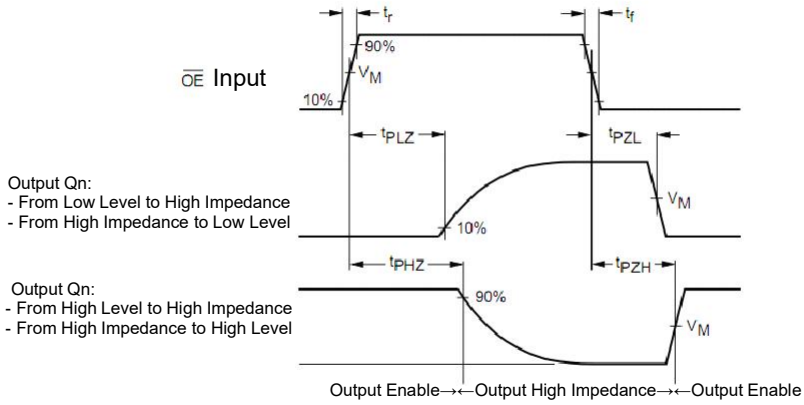
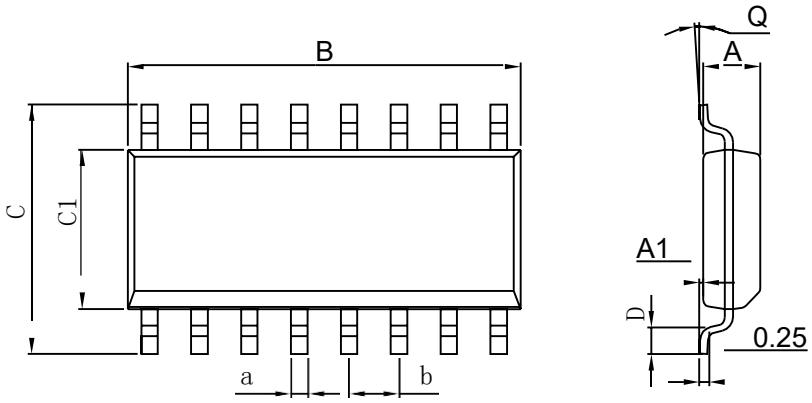


Fig.10 The diagram illustrates the transition time of the tri-state output in response to changes in the output enable terminal.

Package Outline

SOP16



Dimensions In Millimeters					
Symbol	**Min**	**Max**	**Symbol**	**Min**	**Max**
A	4.520	4.620	**D**	0.400	0.950
A1	0.100	0.250	**Q**	0°	8°
B	8.500	9.000	**a**	0.420TYP	
C	5.800	6.250	**b**	1.270TYP	
C1	3.800	4.000			