# **74HC688**

# 8-bit magnitude comparator

Rev. 5 — 5 August 2024

**Product data sheet** 

## 1. General description

The 74HC688 is an 8-bit magnitude comparator. It performs comparisons of two 8-bit binary or BCD words. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{\rm CC}$ .

### 2. Features and benefits

- · Compare two 8-bit words
- Wide supply voltage range from 2.0 V to 6.0 V
- · CMOS input levels
- · CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

# 3. Ordering information

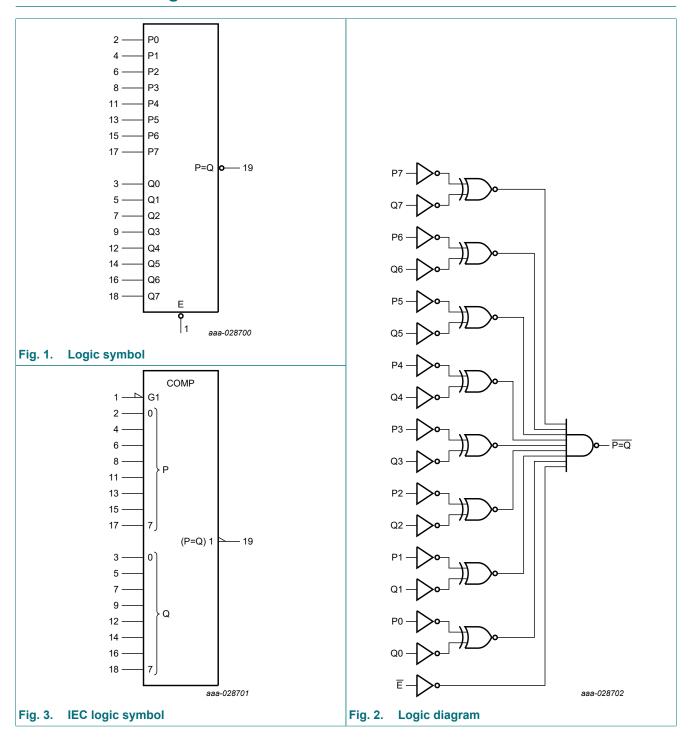
#### **Table 1. Ordering information**

Type number	Package								
	Temperature range	Name	Description	Version					
74HC688D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	<u>SOT163-1</u>					
74HC688PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1					



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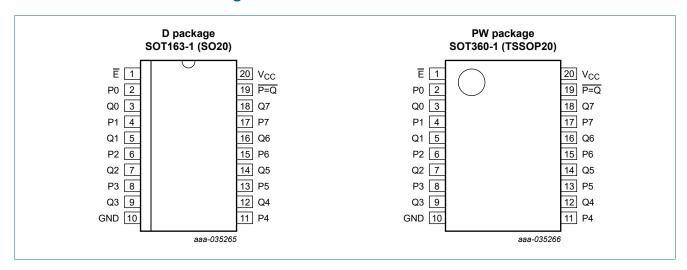
# 4. Functional diagram



8-bit magnitude comparator

# 5. Pinning information

### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
E	1	enable input (active LOW)
P0, P1, P2, P3, P4, P5, P6, P7	2, 4, 6, 8, 11, 13, 15, 17	word P inputs
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 5, 7, 9, 12, 14, 16, 18	word Q inputs
GND	10	ground (0 V)
P=Q	19	equal to output
V <sub>CC</sub>	20	supply voltage

# 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

inputs		output
data Pn, Qn	E	P=Q
P=Q	L	L
P>Q	L	Н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
X	Н	Н

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# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
lo	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±25	mA
I <sub>CC</sub>	supply current			-	50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V

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<sup>[2]</sup> For SOT163-1 (SO20) package: P<sub>tot</sub> derates linearly with 12.3 mW/K above 109 °C. For SOT360-1 (TSSOP20) package: P<sub>tot</sub> derates linearly with 10.0 mW/K above 100 °C.

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# 9. Static characteristics

**Table 6. Static characteristics** 

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

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# 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $C_L$  = 50 pF unless otherwise specified; for test circuit, see Fig. 6

Symbol	Parameter	Conditions	25 °C			_	°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation	Pn, Qn to P=Q; see Fig. 4 [1]								
	delay	V <sub>CC</sub> = 2.0 V	-	55	170	-	215	-	255	ns
		V <sub>CC</sub> = 4.5 V	-	20	34	-	43	-	51	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	16	29	-	37	-	43	ns
		E to P=Q; see Fig. 5								
	V <sub>CC</sub> = 2.0 V	-	28	120	-	150	-	180	ns	
		V <sub>CC</sub> = 4.5 V	-	10	24	-	30	-	36	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	8	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	8	20	-	26	-	31	ns
t <sub>t</sub>	transition time	see <u>Fig. 5</u> [2]								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC}$ [3]	-	30	-	-	-	-	-	pF

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

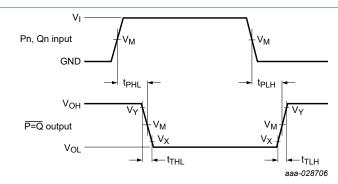
 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs};$ 

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

#### 8-bit magnitude comparator

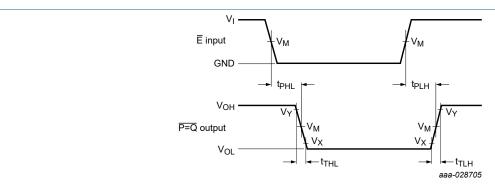
### 10.1. Waveforms and test circuit



Measurement points are given in Table 8.

 $\ensuremath{V_{OL}}$  and  $\ensuremath{V_{OH}}$  are typical voltage output levels that occur with the output load.

Fig. 4. Waveforms showing the word inputs (Pn, Qn) to the equal to output (P=Q) propagation delays and the output transition times.



Measurement points are given in <u>Table 8</u>.

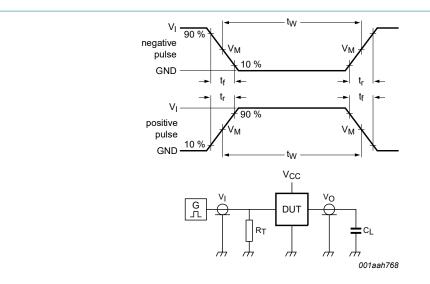
 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

Fig. 5. Waveforms showing the enable input (E) to the equal to output (P=Q) propagation delays and the output transition times.

**Table 8. Measurement points** 

Input		Output					
V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>			
GND to V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.1 × V <sub>CC</sub>	0.9 × V <sub>CC</sub>			

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Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

 $C_L$  = Load capacitance including jig and probe capacitance.

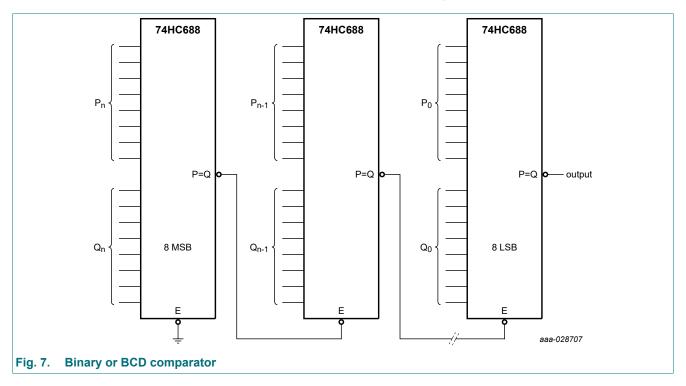
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input		Load	Test	
V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL		
GND to V <sub>CC</sub>	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>	

# 11. Application information

Two or more 74HC688 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits. An example is shown in <u>Fig. 7</u>.

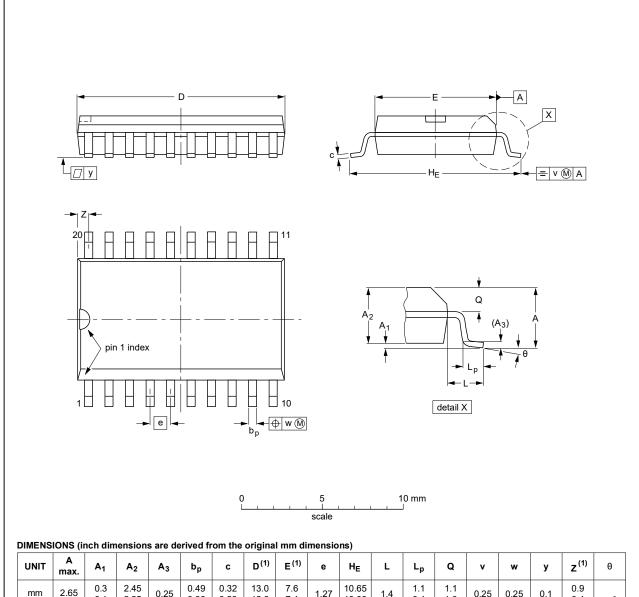


### 8-bit magnitude comparator

# 12. Package outline

### SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

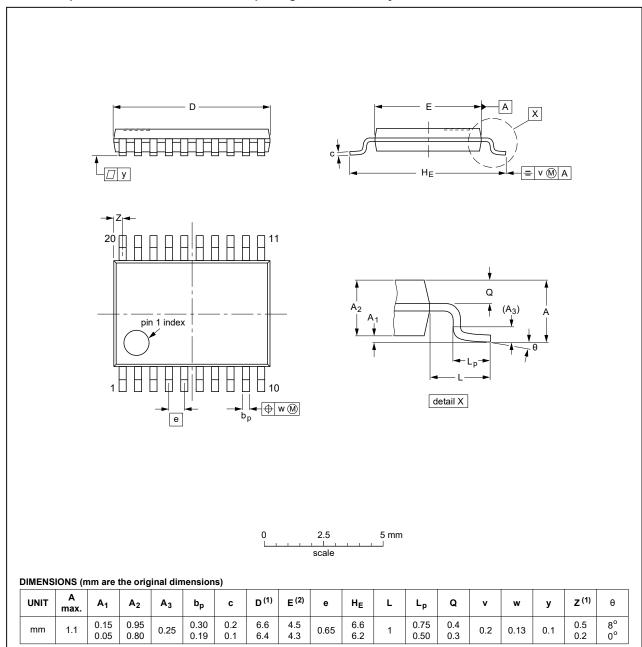
OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013				<del>99-12-27</del> 03-02-19

Package outline SOT163-1 (SO20)

### 8-bit magnitude comparator

#### TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT360-1		MO-153				<del>99-12-27</del> 03-02-19	

Fig. 9. Package outline SOT360-1 (TSSOP20)

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# 13. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description			
ANSI	American National Standards Institute			
CDM	Charged Device Model			
CMOS	Complementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
ESDA	ElectroStatic Discharge Association			
НВМ	Human Body Model			
JEDEC	Joint Electron Device Engineering Council			

# 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC688 v.5	20240805	Product data sheet	-	74HC688 v.4		
Modifications:	Section 2: E	<u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.				
74HC688 v.4	20210716	Product data sheet	-	74HC688 v.3		
Modifications:	Section 2 up	<ul> <li>Type number 74HC688DB (SOT339-1/SSOP20) removed.</li> <li>Section 2 updated.</li> <li>Section 7: Derating values for P<sub>tot</sub> total power dissipation updated.</li> </ul>				
74HC688 v.3	20180704	Product data sheet	-	74HC_HCT688 v.2		
Modifications:	guidelines o Legal texts Type number	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC688N (SOT146-1), 74HCT688N (SOT146-1) and 74HCT688PW (SOT360-1) removed.</li> </ul>				
74HC_HCT688 v.2	19901201	Product specification	-	74HC_HCT688 v.1		

### 8-bit magnitude comparator

# 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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