74HCS02

Quad 2-input NOR gate with Schmitt-trigger inputs

Rev. 1 — 18 September 2025

Product data sheet

1. General description

The 74HCS02 is a quad 2-input NOR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

All inputs are Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- · Schmitt-trigger inputs
- · Low power consumption
 - Typical supply current (I_{CC}) of 100 nA
 - Typical input leakage current (I_I) of ±10 nA
- ±7.8 mA output drive at 6 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- · Complies with JEDEC standards:
 - JESD7A (2.0 V to 6.0 V)
- · ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
 - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- · Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

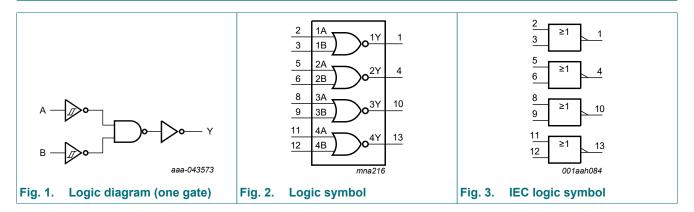
Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74HCS02D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1				
74HCS02PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1				
74HCS02BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1				



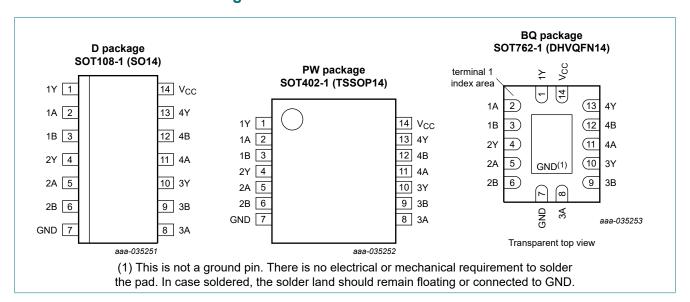
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4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 10, 13	data output
1A, 2A, 3A, 4A	2, 5, 8, 11	data input
1B, 2B, 3B, 4B	3, 6, 9,12	data input
GND	7	ground (0 V)
V _{CC}	14	supply voltage

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6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$

Input	Output	
nA	nB	nY
L	L	Н
X	Н	L
Н	X	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I _{OK}	output clamping current	V_{O} < -0.5 V or V_{O} > V_{CC} + 0.5 V	[1]	-	±20	mA
Io	output current	V _O = 0 V to V _{CC}		-	±35	mA
I _{CC}	supply current			-	70	mA
I _{GND}	ground current			-70	-	mA
Tj	junction temperature		[2]	-	+150	°C
T _{stg}	storage temperature			-65	+150	°C
V _{ESD}	electrostatic discharge	HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V		-	±4000	V
		CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V		-	±1500	V
P _{tot}	total power dissipation		[3]	-	500	mW

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

^[2] Guaranteed by design.

^[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C. For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

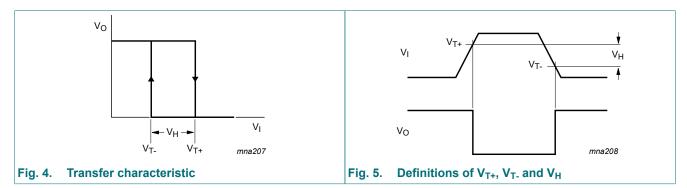
Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{T+}	positive-going	see Fig. 4 and Fig. 5								
	threshold voltage	V _{CC} = 2.0 V	0.7	-	1.5	0.7	1.5	0.7	1.5	٧
voitage	V _{CC} = 4.5 V	1.7	-	3.15	1.7	3.15	1.7	3.15	٧	
		V _{CC} = 6 V	2.1	-	4.2	2.1	4.2	2.1	4.2	٧
		V _{CC} = 3.0 V to 3.6 V	0.4V _{CC}	-	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	٧
		V _{CC} = 4.5 V to 5.5 V	0.38V _{CC}	-	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	٧
V _{T-}	negative-	see Fig. 4 and Fig. 5								
	going threshold	V _{CC} = 2.0 V	0.3	-	1.0	0.3	1.0	0.3	1.0	٧
	voltage	V _{CC} = 4.5 V	0.9	-	2.2	0.9	2.2	0.9	2.2	٧
	_	V _{CC} = 6 V	1.2	-	3.0	1.2	3.0	1.2	3.0	V
		V _{CC} = 3.0 V to 3.6 V	0.2V _{CC}	-	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.2V _{CC}	-	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	٧
V _H	hysteresis	see Fig. 4 and Fig. 5								
	voltage[1]	V _{CC} = 2.0 V	0.2	0.52	1.0	0.2	1.0	0.2	1.0	٧
		V _{CC} = 4.5 V	0.4	0.85	1.4	0.4	1.4	0.4	1.4	٧
		V _{CC} = 6 V	0.6	1.1	1.6	0.6	1.6	0.6	1.6	٧
		V _{CC} = 3.0 V to 3.6 V	0.1V _{CC}	0.72	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	٧
		V _{CC} = 4.5 V to 5.5 V	0.09V _{CC}	0.94	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	٧
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _{OH} = -20 μA; V _{CC} = 2.0 V to 6 V	V _{CC} -0.1	V _{CC} -0.002	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		I _{OH} = -4 mA; V _{CC} = 3.0 V	2.7	2.85	-	2.7	-	2.7	-	V
		I _{OH} = -6 mA; V _{CC} = 4.5 V	4.0	4.3	-	4.0	-	4.0	-	V
		I _{OH} = -7.8 mA; V _{CC} = 6.0 V	5.48	5.75	-	5.4	-	5.4	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{OL} = 20 \mu A;$ $V_{CC} = 2.0 \text{ V to 6 V}$	-	0.002	0.1	-	0.1	-	0.1	V
		I _{OL} = 4 mA; V _{CC} = 3.0 V	-	0.14	0.25	-	0.25	-	0.25	V
		I _{OL} = 6 mA; V _{CC} = 4.5 V	-	0.18	0.26	-	0.30	-	0.30	V
		I _{OL} = 7.8 mA; V _{CC} = 6.0 V	-	0.22	0.26	-	0.33	-	0.33	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	±0.01	±0.1	-	±0.25	-	±1.0	μΑ
I _{cc}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	0.1	-	-	0.5	-	2.0	μΑ

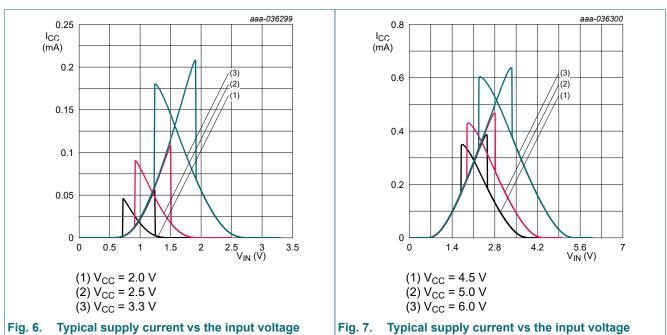
[1] Guaranteed by design.

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9.1. Transfer characteristic waveforms and graphs

9.1.1. For inputs

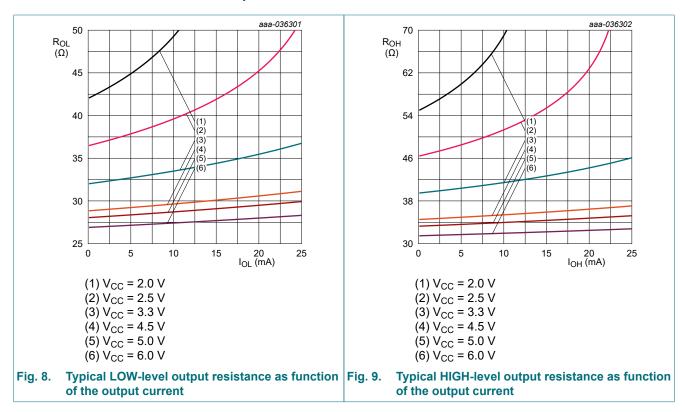




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Quad 2-input NOR gate with Schmitt-trigger inputs

9.1.2. For outputs



10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Section 10.1.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{pd}	propagation	nA, nB to nY; see Fig. 10 [2]								
	delay	V _{CC} = 2 V	-	16	29	-	33	-	36	ns
		V _{CC} = 4.5 V	-	7	11	-	12	-	13	ns
		V _{CC} = 6 V	-	6	10	-	11	-	12	ns
		V _{CC} = 3.0 V to 3.6 V	-	8	14	-	17	-	18	ns
		V _{CC} = 4.5 V to 5.5 V	-	6	11	-	12	-	13	ns
t _t	transition	nY; see <u>Fig. 10</u> [3]								
	time	V _{CC} = 2 V	-	9	13	-	15	-	16	ns
		V _{CC} = 4.5 V	-	5	7	-	8	-	8	ns
		V _{CC} = 6 V	-	4	6	-	7	-	7	ns
		V _{CC} = 3.0 V to 3.6 V	-	5	8	-	9	-	10	ns
		V _{CC} = 4.5 V to 5.5 V	-	4	7	-	8	-	8	ns
Cı	input capacitance		-	1.5	-	-	5	-	5	pF

Quad 2-input NOR gate with Schmitt-trigger inputs

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ[1]	Max	Min	Max	Min	Max	
C _{PD}	dissipation	$f_i = 1 \text{ MHz}; C_L = 0 \text{ pF};$ [4] $V_I = \text{GND to } V_{CC};$ $V_{CC} = 2.0 \text{ V to } 6.0 \text{ V}$	-	10	-	-	-	-	-	pF

- Typical values are measured at nominal supply voltage.
- [2] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [3] t_t is the same as t_{THL} and t_{TLH}.
 [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where: $f_i = \text{input frequency in MHz}$;

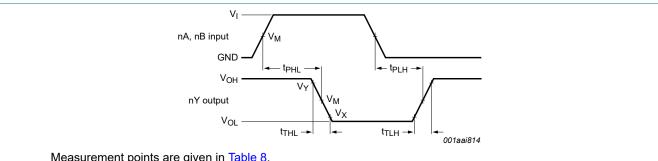
f_o = output frequency in MHz;

 $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs};$

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.

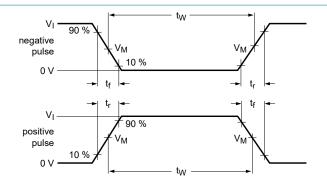
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

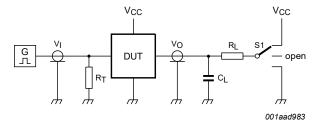
Fig. 10. Propagation delay input (nA) to output (nY)

Table 8. Measurement points

Input	Output	Dutput				
V_{M}	V _M	V_{M} V_{X} V_{Y}				
0.5V _{CC}	0.5V _{CC}	10 %	90 %			

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Test data is given in Table 9.

Definitions for test circuit:

 $\ensuremath{C_L}$ = load capacitance including jig and probe capacitance.

R_L = load resistance.

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1 = test selection switch.

Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Input Lo		Load		S1 position			
V _I	t _r , t _f	C _L R _L		t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t_{PZL}, t_{PLZ}	
V _{CC}	2.5 ns	50 pF	1 kΩ	open	GND	V _{CC}	

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11. Package outline

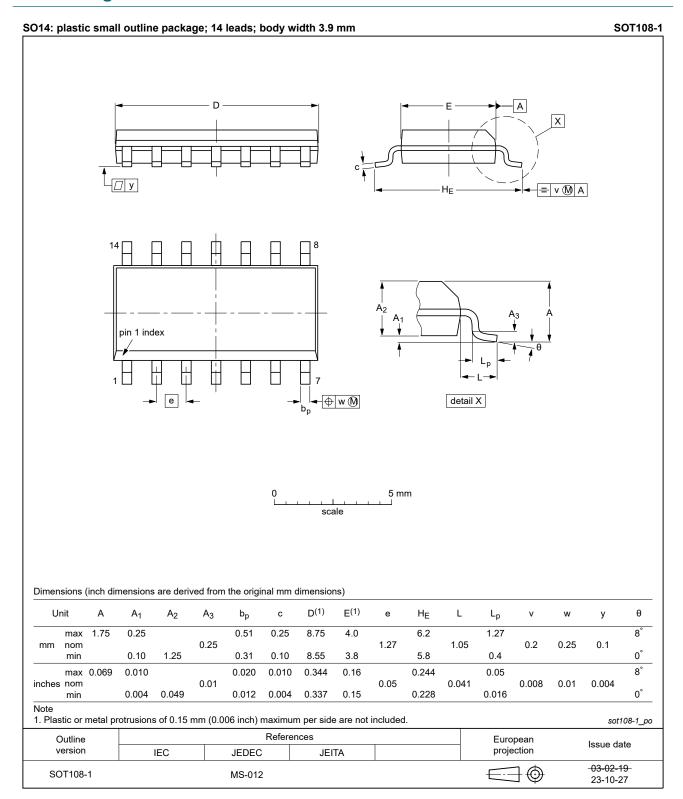


Fig. 12. Package outline SOT108-1 (SO14)

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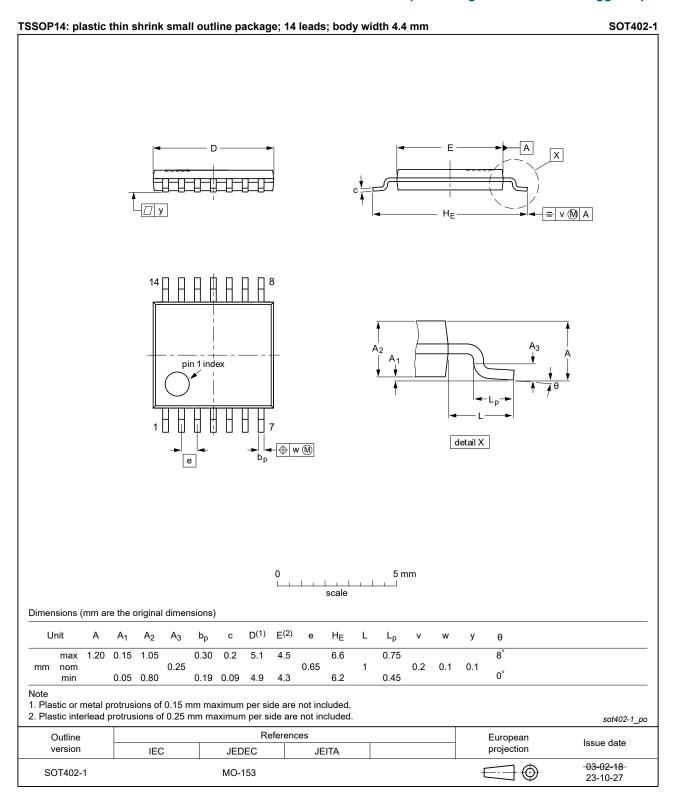


Fig. 13. Package outline SOT402-1 (TSSOP14)

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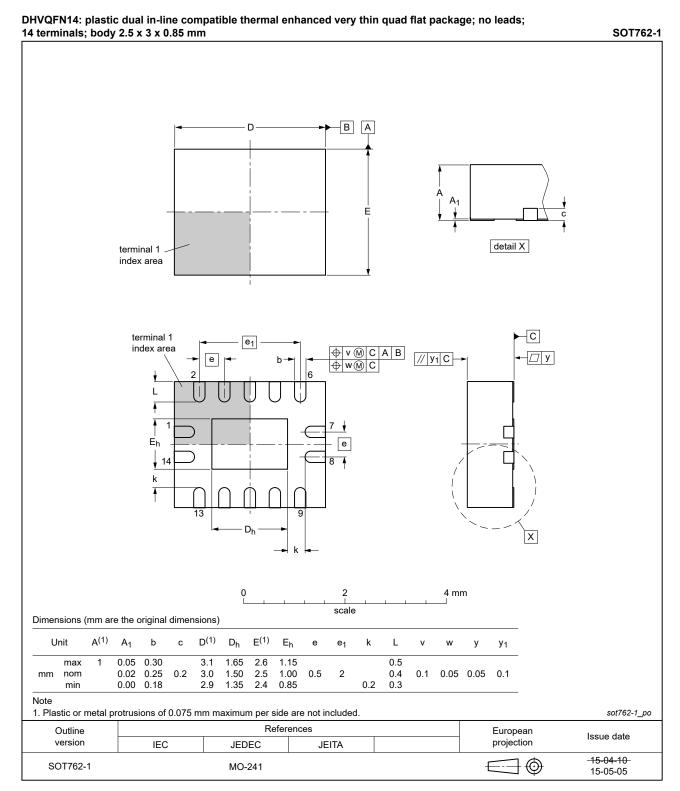


Fig. 14. Package outline SOT762-1 (DHVQFN14)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS02 v.1	20250918	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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