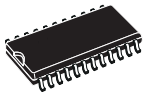
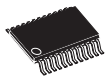
# 74LCX646

## LOW VOLT. CMOS OCTAL BUS TRANSCEIVER/REGISTER WITH 5 VOLT TOLERANT INPUTS AND OUTPUTS(3-STATE)

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
  $t_{PD}$ = 7.0 ns (MAX.) at $V_{CC}$ = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at $V_{CC}$ = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  $V_{CC}$(OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 646
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V



**SOP**



**TSSOP**

### ORDER CODES

| PACKAGE | TUBE | T & R |
|---|---|---|
| SOP | 74LCX646M1R | 74LCX646RM13TR |
| TSSOP | | 74LCX646TTR |

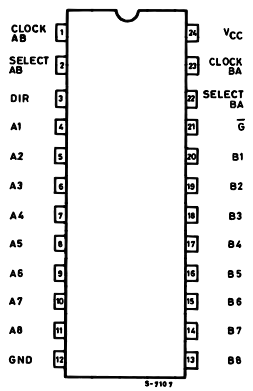
### DESCRIPTION

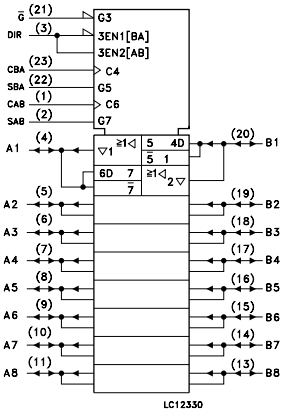
The 74LCX646 is a low voltage CMOS OCTAL BUS TRANSCEIVER AND REGISTER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring $C^2MOS$ technology.

It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

This device consists of bus transceiver circuits with 3 state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into register on the low to high transition of the appropriate clock pin (Clock AB or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (Select AB select BA) can multiplex stored and real time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode

### PIN CONNECTION AND IEC LOGIC SYMBOLS

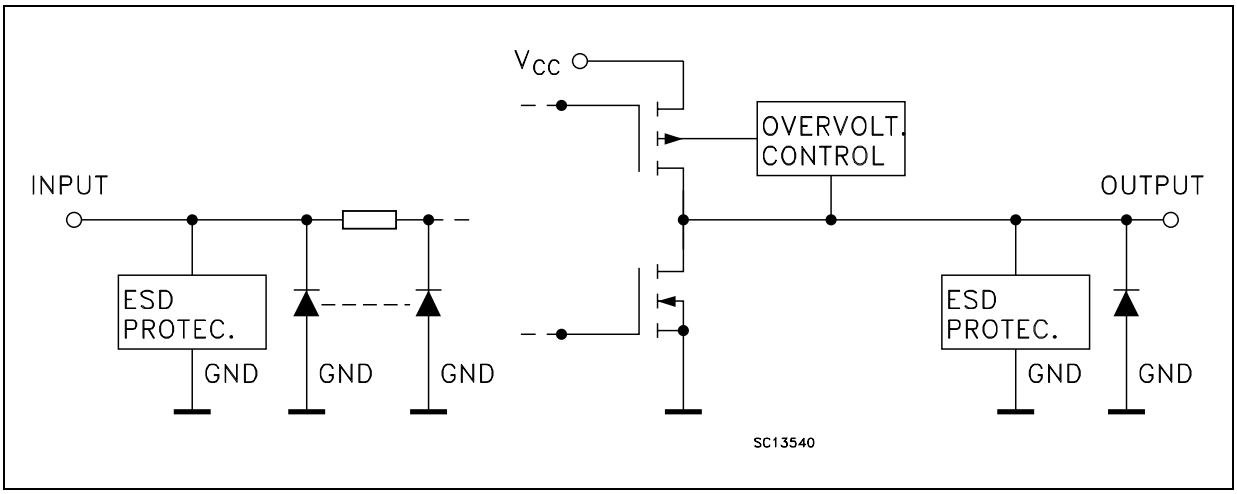


(enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

## INPUT AND OUTPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

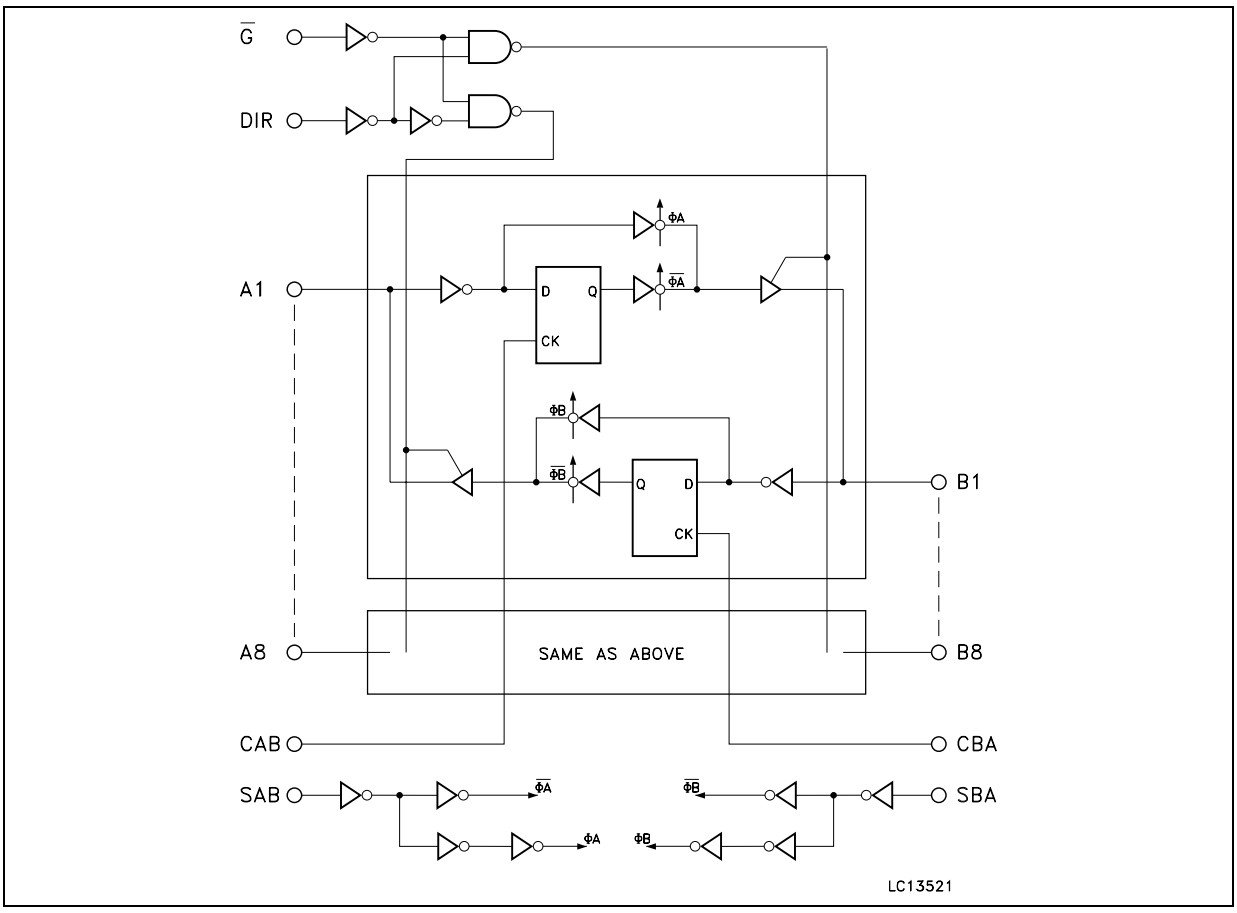
| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | CLOCK AB (CAB) | A to B Clock Input (LOW to HIGH, Edge-Triggered) |
| 2 | SELECT AB (SAB) | Select A to B Source Input |
| 3 | DIR | Direction Control Input |
| 4, 5, 6, 7, 8, 9, 10, 11 | A1 to A8 | A Data Inputs/Outputs |
| 20, 19, 18, 17, 16, 15, 14, 13 | B1 to B8 | B Data Inputs/Outputs |
| 21 | $\overline{G}$ | Output Enable Input (Active LOW) |
| 22 | SELECT BA (SBA) | Select B to A Source Input |
| 23 | CLOCK BA (CBA) | B to A Clock Input (LOW to HIGH, Edge Triggered) |
| 12 | GND | Ground (0V) |
| 24 | $V_{CC}$ | Positive Supply Voltage |

## TRUTH TABLE

| $\overline{G}$ | DIR | CAB | CBA | SAB | SBA | A | B | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| H | X | | | | | INPUTS | INPUTS | Both the A bus and the B bus are inputs |
| | | X | X | X | X | Z | Z | The Output functions of the A and B bus are disabled |
| | | ⎍ | ⎍ | X | X | INPUTS | INPUTS | Both the A and B bus are used as inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs. |
| L | H | | | | | INPUTS | OUTPUTS | The A bus are inputs and the B bus are outputs |
| | | X | X* | L | X | L | L | The data at the A bus are displayed at the B bus |
| | | | | | | H | H | |
| | | ⎍ | X* | L | X | L | L | The data at the A bus are displayed at the B bus. The data of the A bus are stored to internal flip-flop on low to high transition of the clock pulse |
| | | | | | | H | H | |
| | | X | X* | H | X | X | Qn | The data stored to the internal flip-flop are displayed at the B bus. |
| | | ⎍ | X* | H | X | L | L | The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus. |
| | | | | | | H | H | |
| L | L | | | | | OUTPUTS | INPUTS | The B bus are inputs and the A bus are outputs. |
| | | X* | X | X | L | L | L | The data at the B bus are displayed at the A bus |
| | | | | | | H | H | |
| | | X* | ⎍ | X | L | L | L | The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. |
| | | | | | | H | H | |
| | | X* | X | X | H | Qn | X | The data stored to the internal flip-flops are displayed at the A bus |
| | | X* | ⎍ | X | H | L | L | The data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus. |
| | | | | | | H | H | |

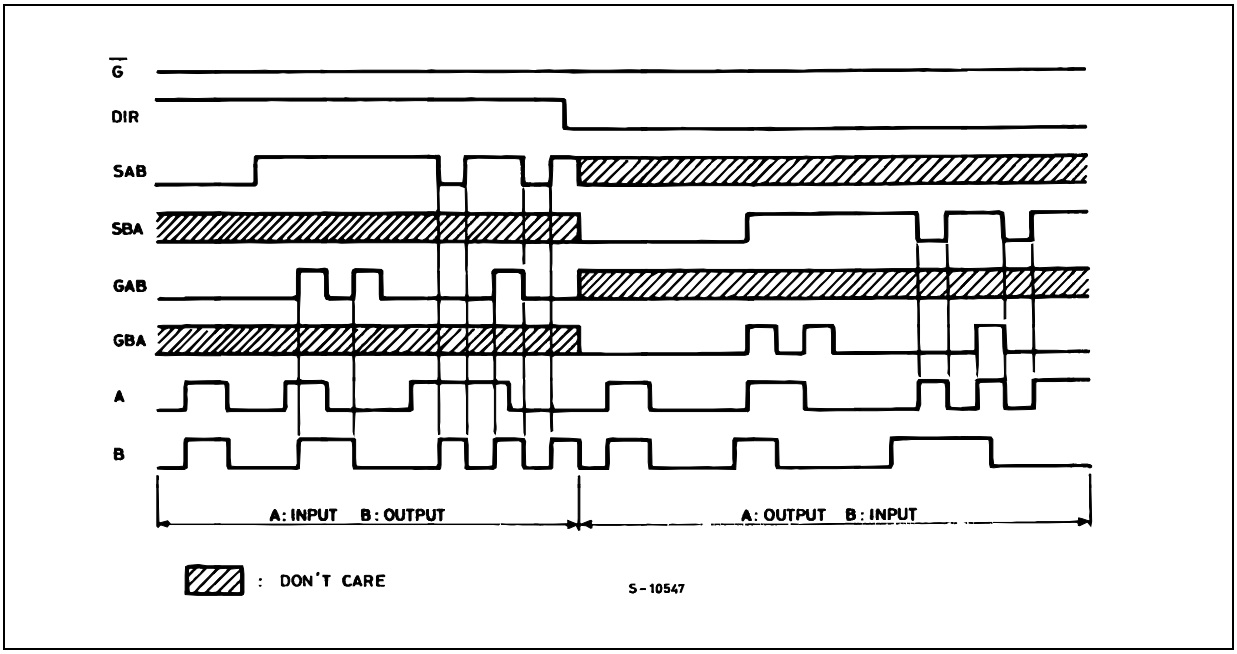
X : Don't Care
Z : High Impedance
Qn : The data stored to the internal flip-flops by most recent low to high transition of the clock inputs
* : The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

## LOGIC DIAGRAM




This logic diagram has not be used to estimate propagation delays

## TIMING CHART



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | -0.5 to +7.0 | V |
| $V_O$ | DC Output Voltage (OFF State) | -0.5 to +7.0 | V |
| $V_O$ | DC Output Voltage (High or Low State) (note 1) | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | - 50 | mA |
| $I_{OK}$ | DC Output Diode Current (note 2) | - 50 | mA |
| $I_O$ | DC Output Current | ± 50 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ± 100 | mA |
| $I_{GND}$ | DC Ground Current per Supply Pin | ± 100 | mA |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) $I_O$ absolute maximum rating must be observed
2) $V_O$ < GND

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage (note 1) | 2.0 to 3.6 | V |
| $V_I$ | Input Voltage | 0 to 5.5 | V |
| $V_O$ | Output Voltage (OFF State) | 0 to 5.5 | V |
| $V_O$ | Output Voltage (High or Low State) | 0 to $V_{CC}$ | V |
| $I_{OH}$, $I_{OL}$ | High or Low Level Output Current ($V_{CC}$ = 3.0 to 3.6V) | ± 24 | mA |
| $I_{OH}$, $I_{OL}$ | High or Low Level Output Current ($V_{CC}$ = 2.7V) | ± 12 | mA |
| $T_{op}$ | Operating Temperature | -55 to 125 | °C |
| dt/dv | Input Rise and Fall Time (note 2) | 0 to 10 | ns/V |

1) Truth Table guaranteed: 1.5V to 3.6V
2) $V_{IN}$ from 0.8V to 2V at $V_{CC}$ = 3.0V

## DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | -40 to 85 °C | | -55 to 125 °C | | |
| | | | | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.7 to 3.6 | | 2.0 | | 2.0 | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | | 0.8 | V |
| $V_{OH}$ | High Level Output Voltage | 2.7 to 3.6 | $I_O$=-100 µA | $V_{CC}$-0.2 | | $V_{CC}$-0.2 | | V |
| | | 2.7 | $I_O$=-12 mA | 2.2 | | 2.2 | | |
| | | 3.0 | $I_O$=-18 mA | 2.4 | | 2.4 | | |
| | | | $I_O$=-24 mA | 2.2 | | 2.2 | | |
| $V_{OL}$ | Low Level Output Voltage | 2.7 to 3.6 | $I_O$=100 µA | | 0.2 | | 0.2 | V |
| | | 2.7 | $I_O$=12 mA | | 0.4 | | 0.4 | |
| | | 3.0 | $I_O$=16 mA | | 0.4 | | 0.4 | |
| | | | $I_O$=24 mA | | 0.55 | | 0.55 | |
| $I_I$ | Input Leakage Current | 2.7 to 3.6 | $V_I$ = 0 to 5.5V | | ± 5 | | ± 5 | µA |
| $I_{off}$ | Power Off Leakage Current | 0 | $V_I$ or $V_O$ = 5.5V | | 10 | | 10 | µA |
| $I_{OZ}$ | High Impedance Output Leakage Current | 2.7 to 3.6 | $V_I$ = $V_{IH}$ or $V_{IL}$<br>$V_O$ = 0 to $V_{CC}$ | | ± 5 | | ± 5 | µA |
| $I_{CC}$ | Quiescent Supply Current | 2.7 to 3.6 | $V_I$ = $V_{CC}$ or GND | | 10 | | 10 | µA |
| | | | $V_I$ or $V_O$= 3.6 to 5.5V | | ± 10 | | ± 10 | |
| $\Delta I_{CC}$ | $I_{CC}$ incr. per Input | 2.7 to 3.6 | $V_{IH}$ = $V_{CC}$ - 0.6V | | 500 | | 500 | µA |

## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | |
| | | | | Min. | Typ. | Max. | |
| $V_{OLP}$ | Dynamic Low Level Quiet Output (note 1) | 3.3 | $C_L$ = 50pF<br>$V_{IL}$ = 0V, $V_{IH}$ = 3.3V | | 0.8 | | V |
| $V_{OLV}$ | | | | | -0.8 | | |

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | | | | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | $R_L$ (Ω) | $t_s = t_r$ (ns) | -40 to 85 °C | | -55 to 125 °C | | |
| | | | | | | Min. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CAB or CBA to An or Bn) | 2.7 | 50 | 500 | 2.5 | 1.5 | 9.5 | 1.5 | 9.5 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 8.5 | 1.5 | 8.5 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (An to Bn or Bn to An) | 2.7 | 50 | 500 | 2.5 | 1.5 | 8.0 | 1.5 | 8.0 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 7.0 | 1.5 | 7.0 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (SAB or SBA to An or Bn) | 2.7 | 50 | 500 | 2.5 | 1.5 | 9.5 | 1.5 | 9.5 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 8.5 | 1.5 | 8.5 | |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Time ($\overline{G}$, DIR to An, Bn) | 2.7 | 50 | 500 | 2.5 | 1.5 | 9.5 | 1.5 | 9.5 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 8.5 | 1.5 | 8.5 | |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Time ($\overline{G}$, DIR to An, Bn) | 2.7 | 50 | 500 | 2.5 | 1.5 | 9.5 | 1.5 | 9.5 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 8.5 | 1.5 | 8.5 | |
| $t_S$ | Setup Time, HIGH or LOW level Data to CAB, CBA | 2.7 | 50 | 500 | 2.5 | 2.5 | | 2.5 | | ns |
| | | 3.0 to 3.6 | | | | 2.5 | | 2.5 | | |
| $t_h$ | Hold Time, HIGH or LOW level Data to CAB, CBA | 2.7 | 50 | 500 | 2.5 | 1.5 | | 1.5 | | ns |
| | | 3.0 to 3.6 | | | | 1.5 | | 1.5 | | |
| $t_W$ | CAB, CBA Pulse Width, HIGH or LOW | 2.7 | 50 | 500 | 2.5 | 4.0 | | 4.0 | | ns |
| | | 3.0 to 3.6 | | | | 3.3 | | 3.3 | | |
| $f_{MAX}$ | Clock Pulse Frequency | 3.0 to 3.6 | 50 | 500 | 2.5 | 150 | | 150 | | MHz |
| $t_{OSLH}$ $t_{OSHL}$ | Output To Output Skew Time (note1, 2) | 3.0 to 3.6 | 50 | 500 | 2.5 | | 1.0 | | 1.0 | ns |

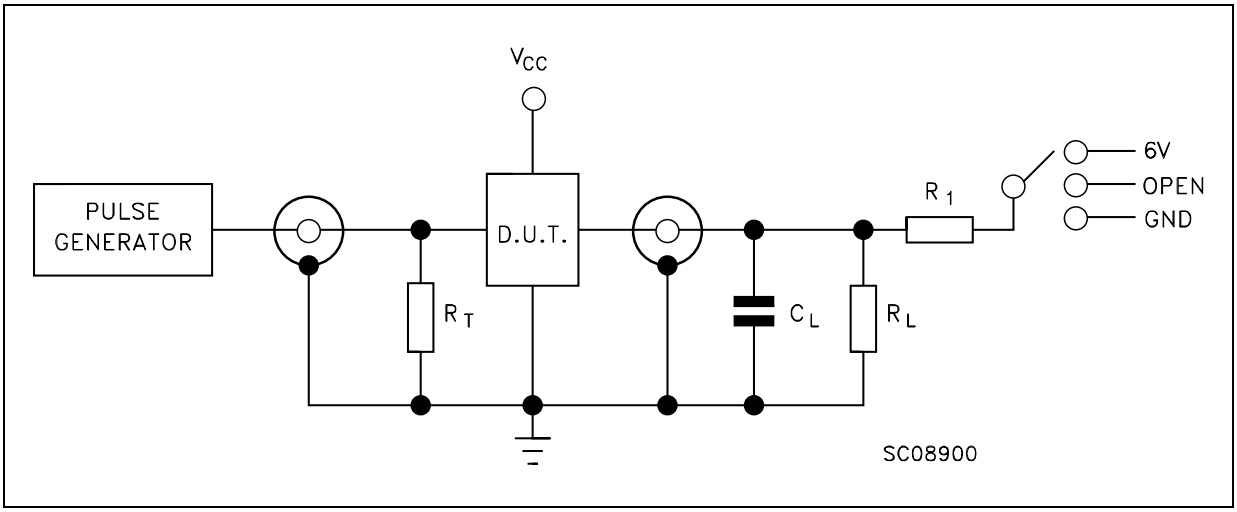
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | |
| | | | | Min. | Typ. | Max. | |
| $C_{IN}$ | Input Capacitance | 3.3 | $V_{IN}$ = 0 to $V_{CC}$ | | 6 | | pF |
| $C_{I/O}$ | I/O Capacitance | 3.3 | $V_{IN}$ = 0 to $V_{CC}$ | | 10 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (note 1) | 3.3 | $f_{IN}$ = 10MHz<br>$V_{IN}$ = 0 or $V_{CC}$ | | 37 | | pF |

1) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

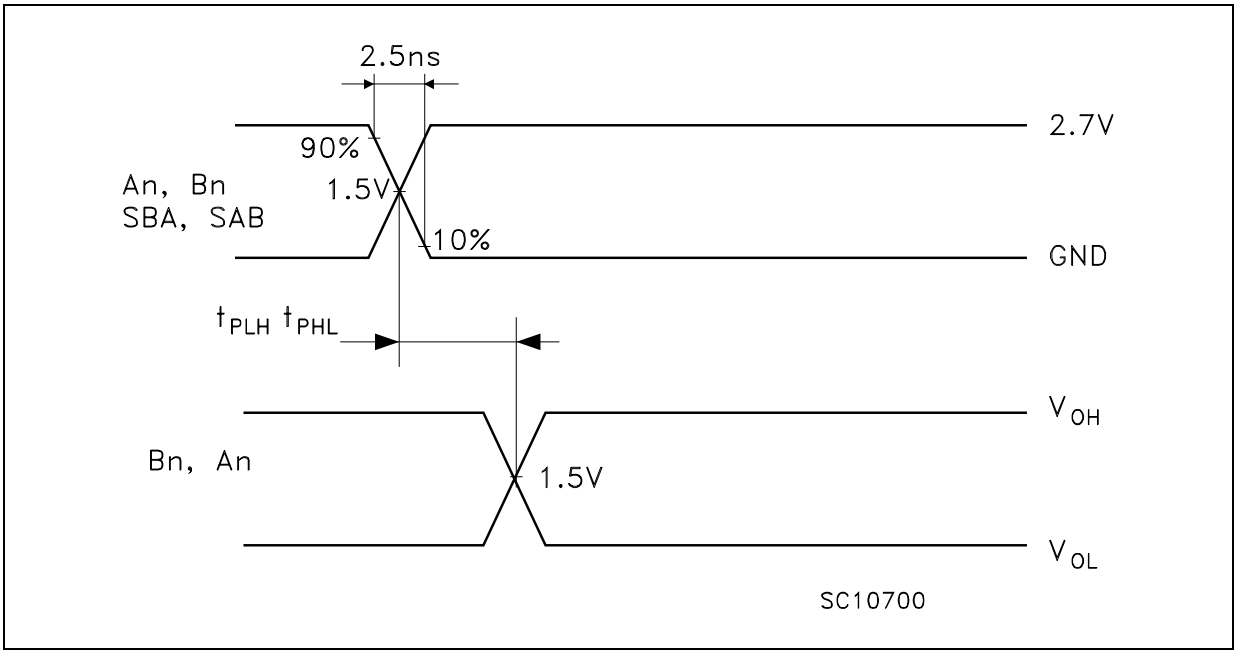
## TEST CIRCUIT



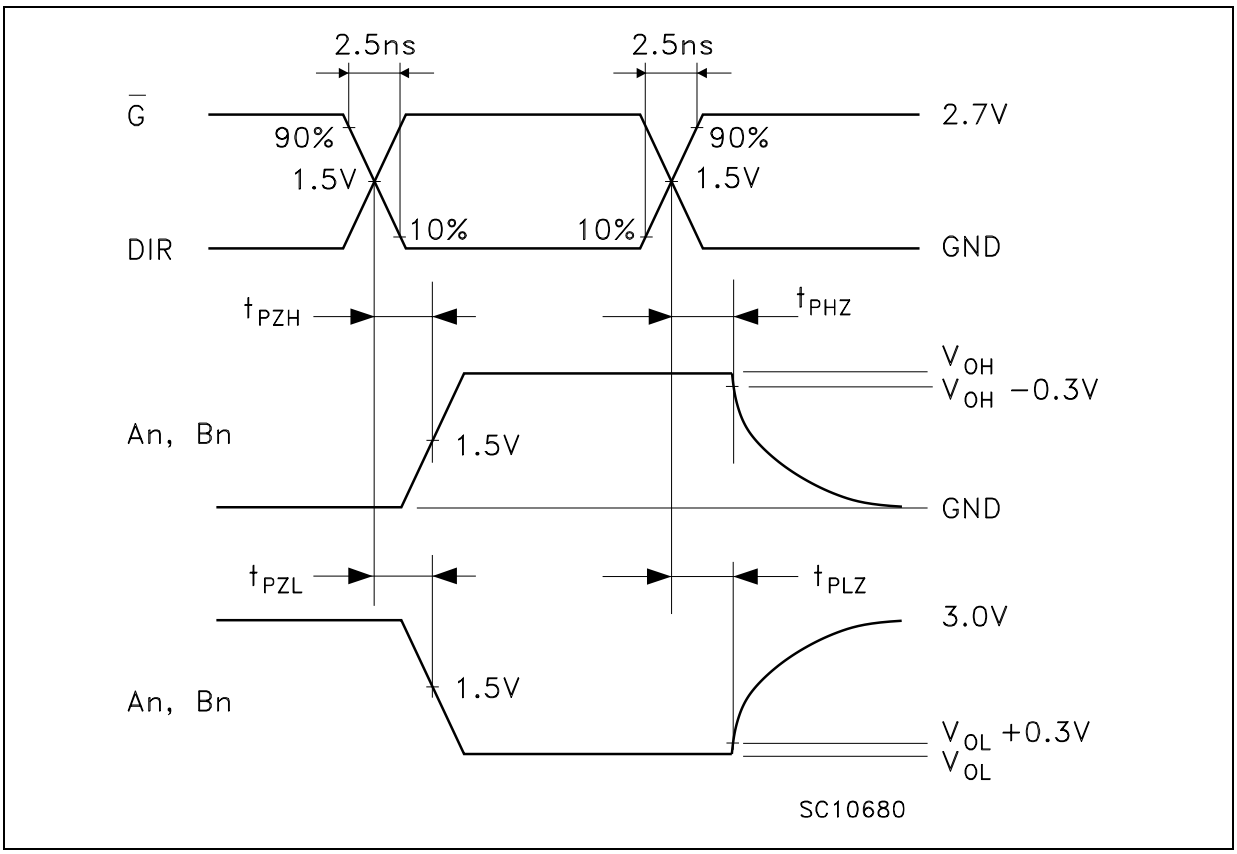

| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ = 50 pF or equivalent (includes jig and probe capacitance)
$R_L$ = R1 = 500Ω or equivalent
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)

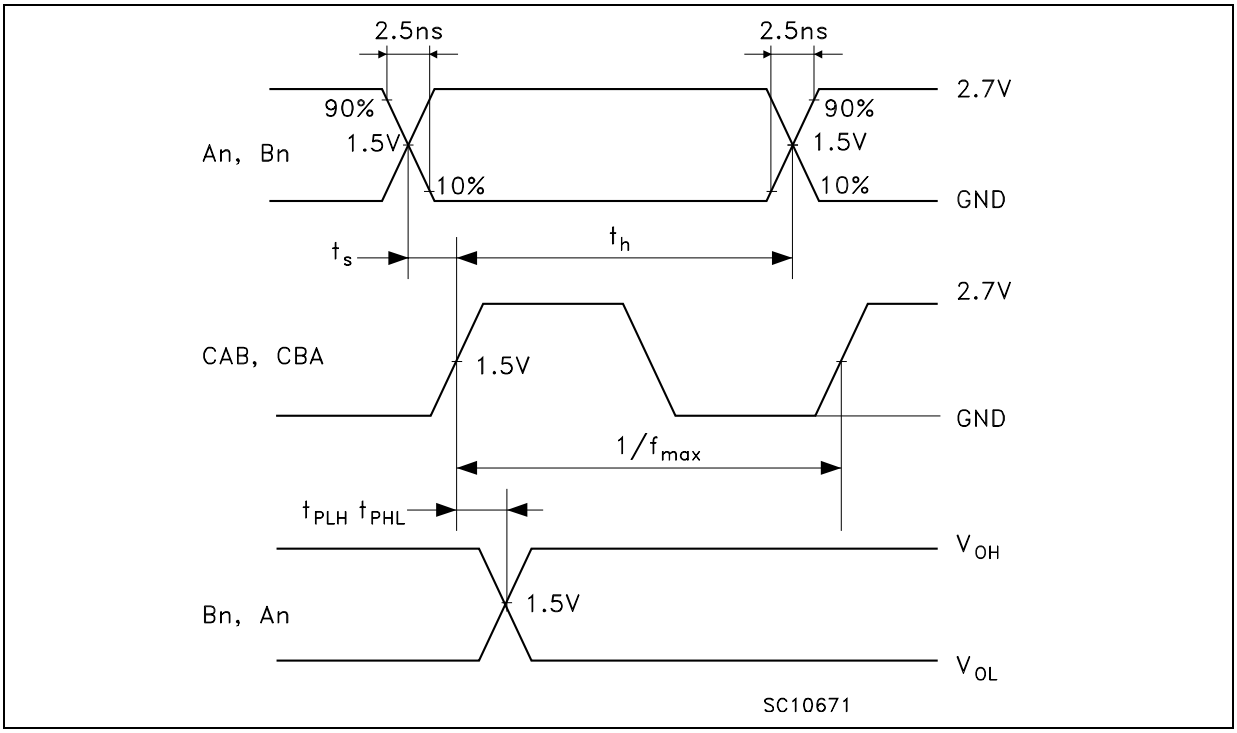
**WAVEFORM 1 : PROPAGATION DELAYS, SAB, SBA, An, Bn, TIMES** (f=1MHz; 50% duty cycle)



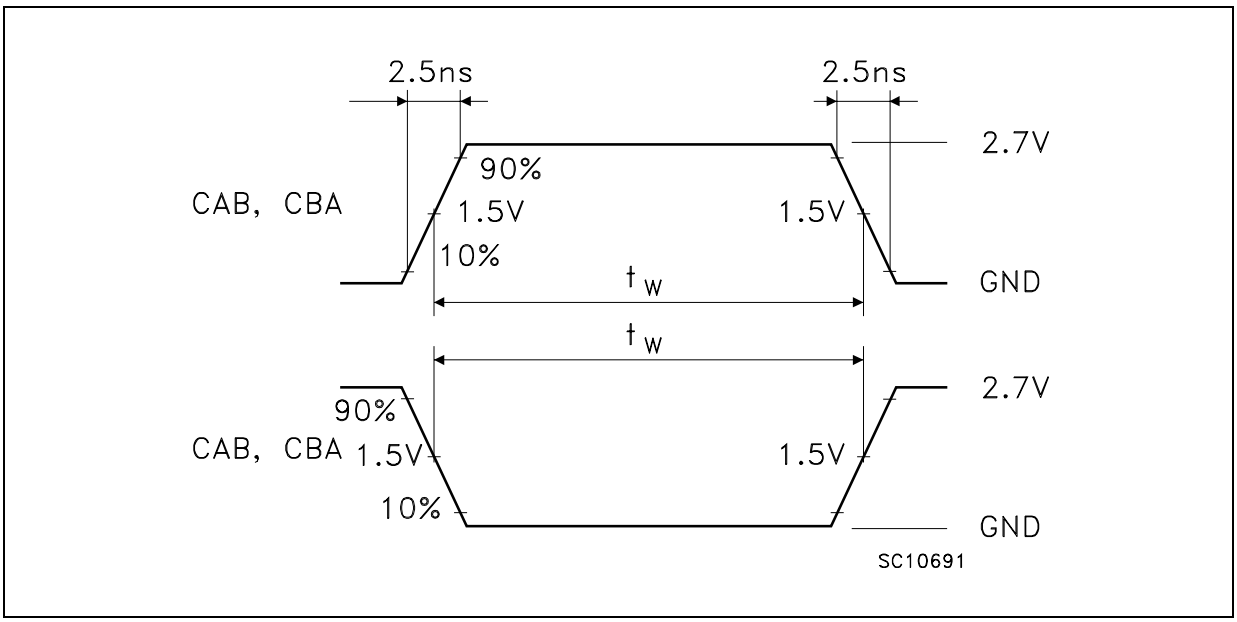
**WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIME** (f=1MHz; 50% duty cycle)



**WAVEFORM 3 : SETUP AND HOLD TIME, CAB, CBA MAXIMUM FREQUENCY** (f=1MHz; 50% duty cycle)

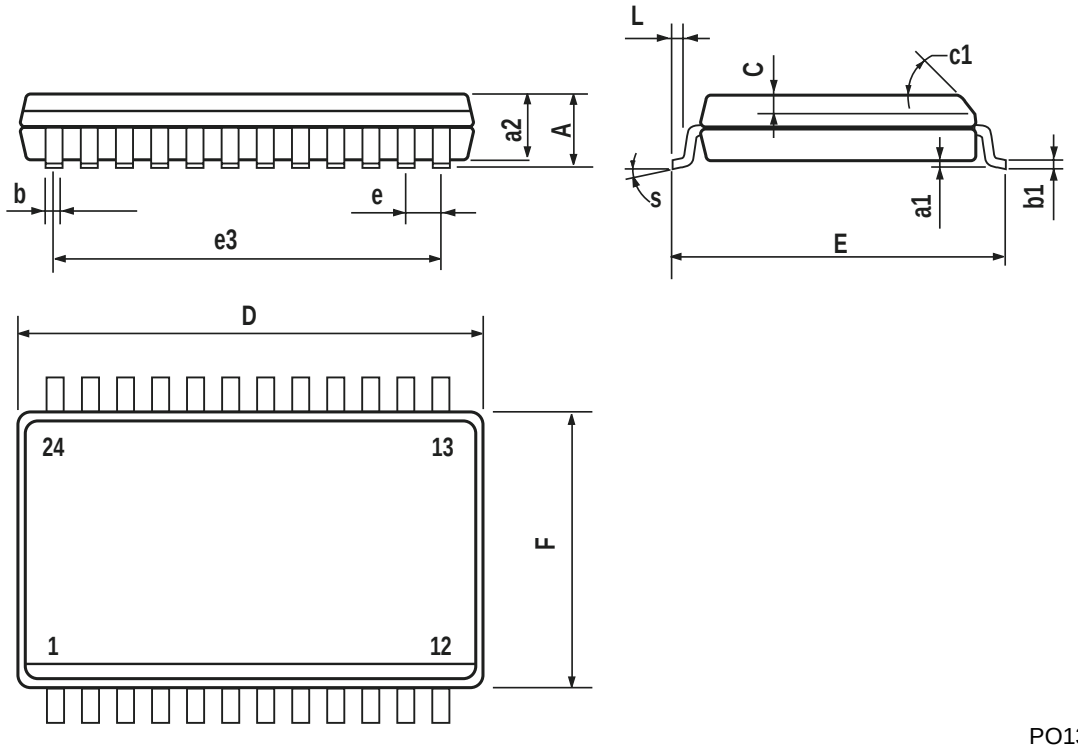



**WAVEFORM 4 : PULSE WIDTH** (f=1MHz; 50% duty cycle)



## SO-24 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 15.20 | | 15.60 | 0.598 | | 0.614 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 13.97 | | | 0.550 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| S | 8° (max.) | | | | | |




PO13T

## TSSOP24 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.1 | | | 0.043 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | | 0.9 | | | 0.035 | |
| b | 0.19 | | 0.30 | 0.0075 | | 0.0118 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | 7.7 | | 7.9 | 0.303 | | 0.311 |
| E | 6.25 | | 6.5 | 0.246 | | 0.256 |
| E1 | 4.3 | | 4.5 | 0.169 | | 0.177 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.50 | | 0.70 | 0.020 | | 0.028 |