FAIRCHILD SEMICONDUCTOR™

February 2001
Revised October 2001

74LCXH162374
Low Voltage 16-Bit D-Type Flip-Flop with Bushold and 26Ω Series Resistors in Outputs

General Description

The LCXH162374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 16-bit operation.

The LCXH162374 is designed for low voltage (2.5V or 3.3V) V_{CC} applications. The LCXH162374 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level. The 26Ω series resistor in the output helps reduce output overshoot and undershoot.

The LCXH162374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant control inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.0 ns t_{PD} max (V_{CC} = 3.3V), 20 µA I_{CC} max
- Power down high impedance inputs and outputs
- ±12 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Equivalent 26Ω series resistors on output
- Bushold on inputs eliminates the need for external pull-up/pull-down resistors
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

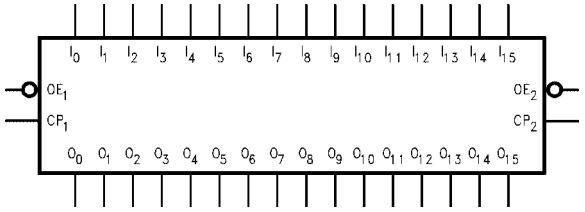
Ordering Code:

Order Number	Package Number	Package Description
74LCXH162374GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCXH162374MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBES]
74LCXH162374MEX (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LCXH162374MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBES]
74LCXH162374MTX (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Note 1: BGA package available in Tape and Reel only.

Note 2: Use this order number to receive devices in Tape and Reel.

Logic Symbol



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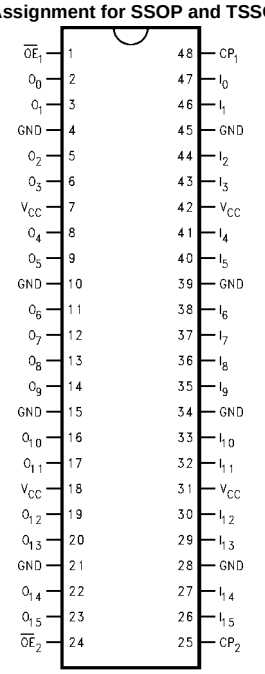
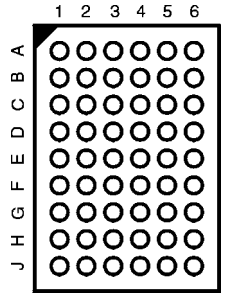
Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP_n	Clock Pulse Input
I_0–I_{15}	Inputs (Bushold)
O_0–O_{15}	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	$\overline{OE}_1$	CP_1	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	$\overline{OE}_2$	CP_2	NC	I_{15}

Truth Tables

Inputs			Outputs
CP_1	**$\overline{OE}_1$**	**I_0–I_7**	**O_0–O_7**
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

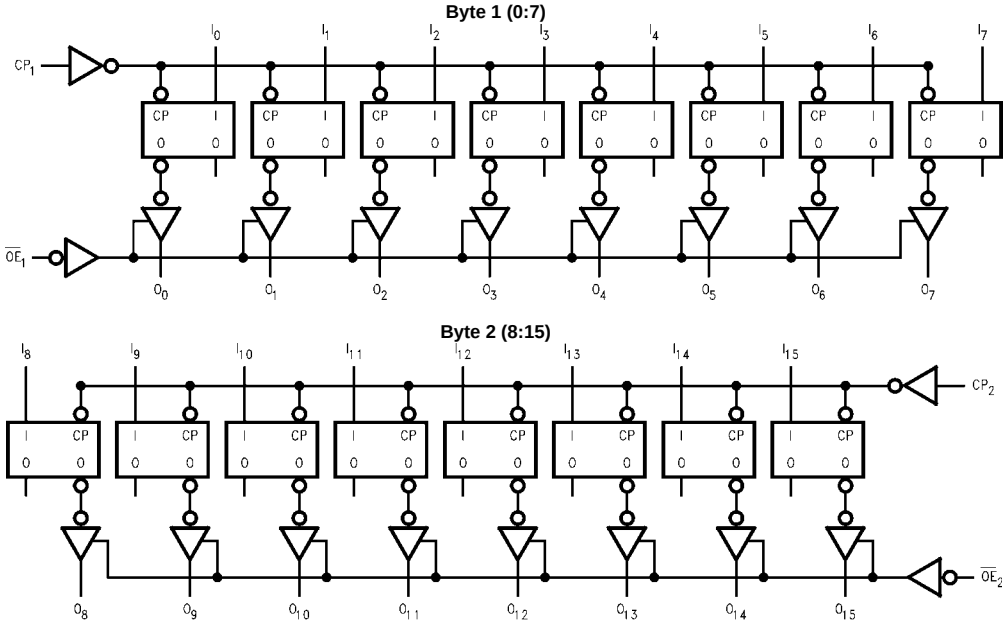
Inputs			Outputs
CP_2	**$\overline{OE}_2$**	**I_8–I_{15}**	**O_8–O_{15}**
↑	L	H	H
↑	L	L	L
L	L	X	O_0
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW of CP

Functional Description

The LCXH162374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}_n$ input does not affect the state of the flip-flops.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage I_0 - I_{15}	−0.5 to V_{CC} + 0.5		V
	$\overline{OE}_n$, LE_n	−0.5V to 7.0V		
V_O	DC Output Voltage	−0.5 to +7.0	3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 5)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current in I_{OH}/I_{OL}	V_{CC} = 3.0V – 3.6V		±12	mA
		V_{CC} = 2.7V – 3.0V		±8	
		V_{CC} = 2.3V – 2.7V		±4	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused control inputs must be HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter		Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
					Min	Max	
V_{IH}	HIGH Level Input Voltage			2.3 – 2.7	1.7		V
				2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage			2.3 – 2.7		0.7	V
				2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage		I_{OH} = −100 µA	2.3 – 3.6	V_{CC} − 0.2		V
			I_{OH} = −4 mA	2.3	1.8		
			I_{OH} = −4mA	2.7	2.2		
			I_{OH} = −6 mA	3.0	2.4		
			I_{OH} = −8 mA	2.7	2.0		
			I_{OH} = −12 mA	3.0	2.0		
V_{OL}	LOW Level Output Voltage		I_{OL} = 100 µA	2.3 – 3.6		0.2	V
			I_{OL} = 4 mA	2.3		0.6	
			I_{OL} = 4 mA	2.7		0.4	
			I_{OL} = 6 mA	3.0		0.55	
			I_{OL} = 8 mA	2.7		0.6	
			I_{OL} = 12 mA	3.0		0.8	
I_I	Input Leakage Current	Data	V_I = V_{CC} or GND	2.3 – 3.6		±5.0	µA
		Control	0V ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	$V_{IN} = 0.7V$	2.3	45		μA
		$V_{IN} = 1.7V$		−45		
		$V_{IN} = 0.8V$	3.0	75		
		$V_{IN} = 2.0V$		−75		
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State	(Note 7)	2.7	300		μA
		(Note 8)		−300		
		(Note 7)	3.6	450		
		(Note 8)		−450		
I_{OZ}	3-STATE Output Leakage	$V_O = V_{CC}$ or GND $V_I = V_{IH}$ or V_{IL}	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	$V_O = V_{CC}$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μA
		$3.6V \le V_O \le 5.5V$ (Note 6)	2.3 – 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	μA

Note 6: Outputs disabled or 3-STATE only.

Note 7: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 8: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170						MHz
t_{PHL}	Propagation Delay	1.5	7.0	1.5	7.3	1.5	8.4	ns
t_{PLH}	CP to O_n	1.5	7.0	1.5	7.3	1.5	8.4	
t_{PZL}	Output Enable time	1.5	6.9	1.5	7.1	1.5	9.0	ns
t_{PZH}		1.5	6.9	1.5	7.1	1.5	9.0	
t_{PLZ}	Output Disable Time	1.5	6.0	1.5	6.2	1.5	7.2	ns
t_{PHZ}		1.5	6.0	1.5	6.2	1.5	7.2	
t_S	Setup Time	2.5		2.5		3.0		ns
t_H	Hold Time	1.5		1.5		2.0		ns
t_W	Pulse Width	3.0		3.0		3.5		ns
t_{OSHL}	Output to Output Skew (Note 9)		1.0					ns
t_{OSLH}			1.0					

Note 9: Skew is defined as the absolute value of the differences between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.35	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.25	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.35	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.25	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

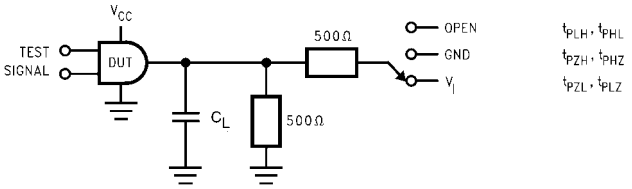
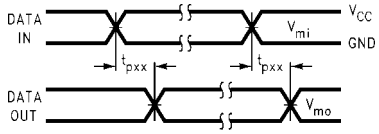
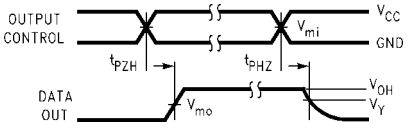


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

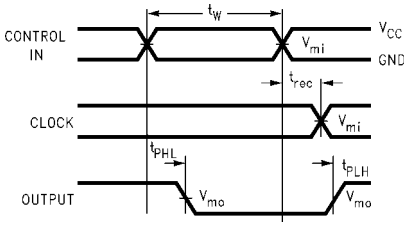
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V, and 2.7V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND



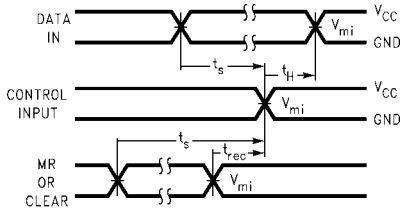
Waveform for Inverting and Non-Inverting Functions



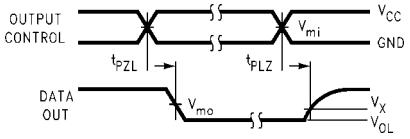
3-STATE Output High Enable and Disable Times for Logic



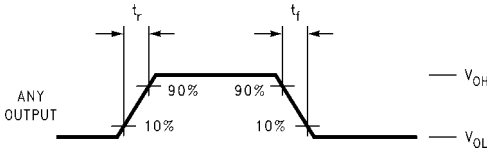
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

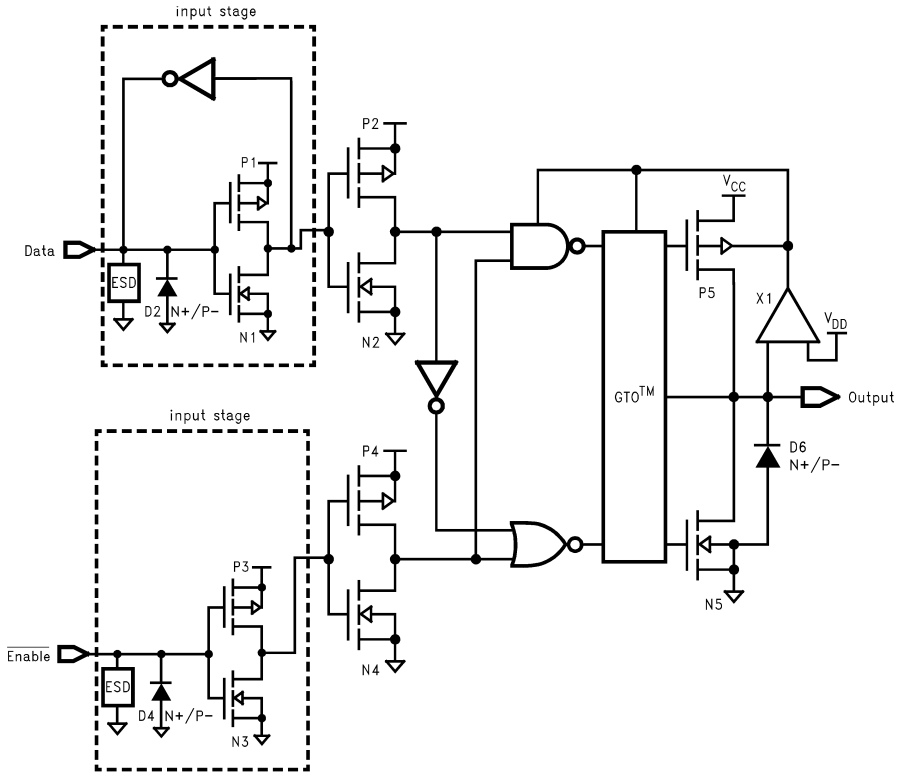


t_{rise} and t_{fall}

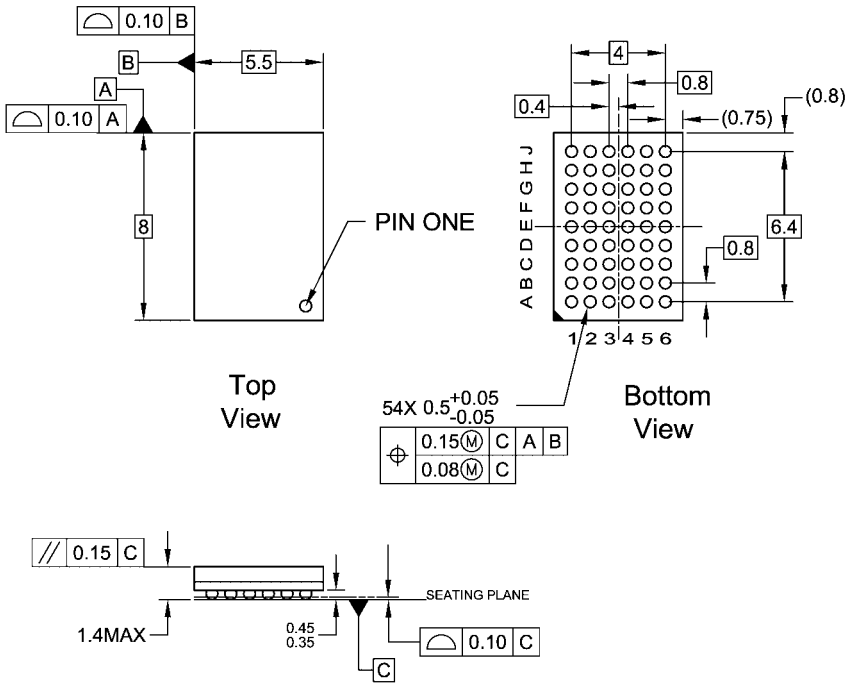
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCXH Family (with Bushold)



Physical Dimensions inches (millimeters) unless otherwise noted



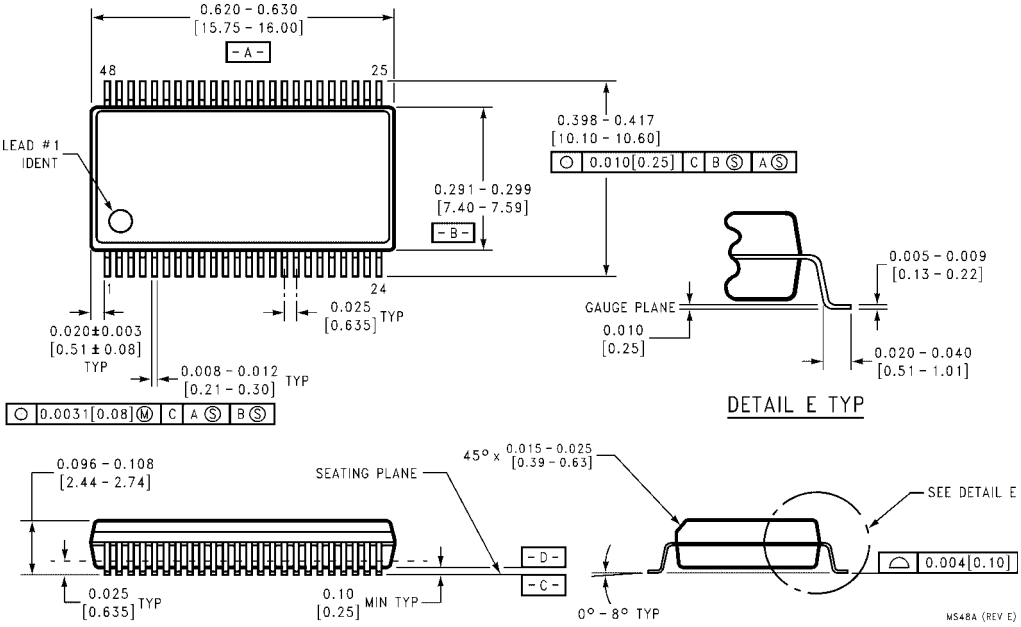
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

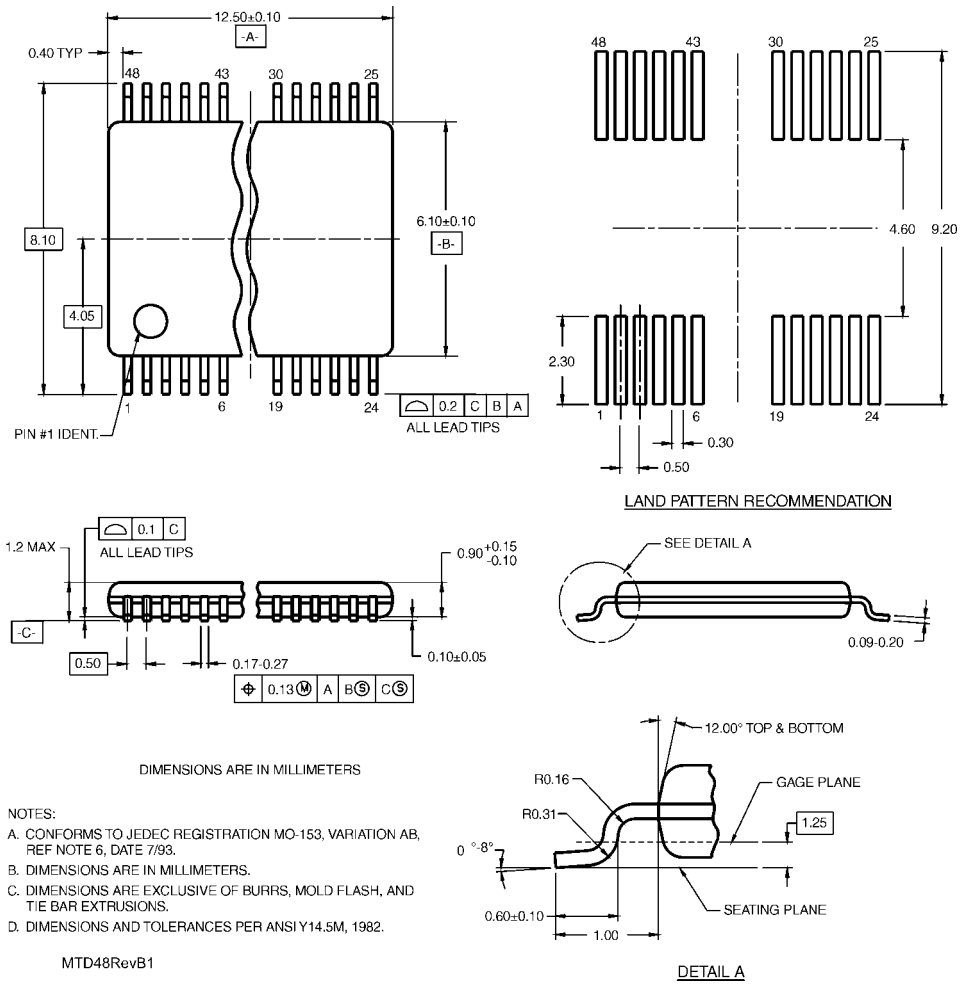
54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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