

## 74LCXH16374

### Low Voltage 16-Bit D-Type Flip-Flop with Bushold

#### General Description

The LCXH16374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

The LCXH16374 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications.

The LCXH16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

The LCXH16374 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

#### Features

- 5V tolerant control inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.2 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 20  $\mu A$   $I_{CC}$  max
- Bushold on inputs eliminating the need for external pull-up/pull-down resistors
- Power down high impedance outputs
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

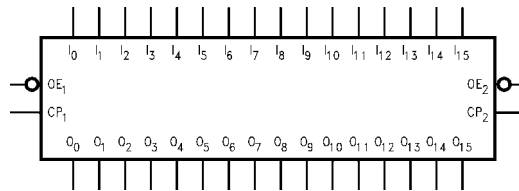
#### Ordering Code:

Order Number	Package Number	Package Description
74LCXH16374G (Note 1)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCXH16374MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCXH16374MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 1:** Ordering code "G" indicates Trays.

**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

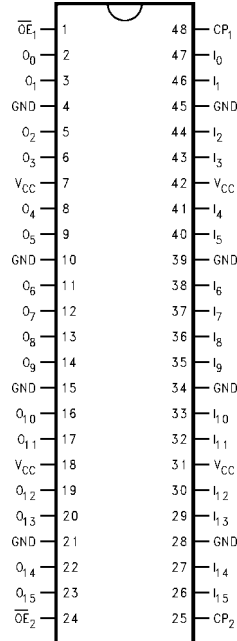
#### Logic Symbol



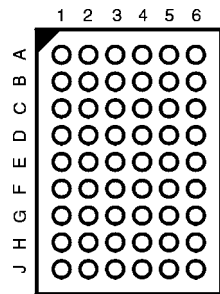
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### Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$CP_n$	Clock Pulse Input
$I_0-I_{15}$	Bushold Inputs
$O_0-O_{15}$	Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$CP_1$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_2$	$CP_2$	NC	$I_{15}$

### Truth Tables

Inputs			Outputs
$CP_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

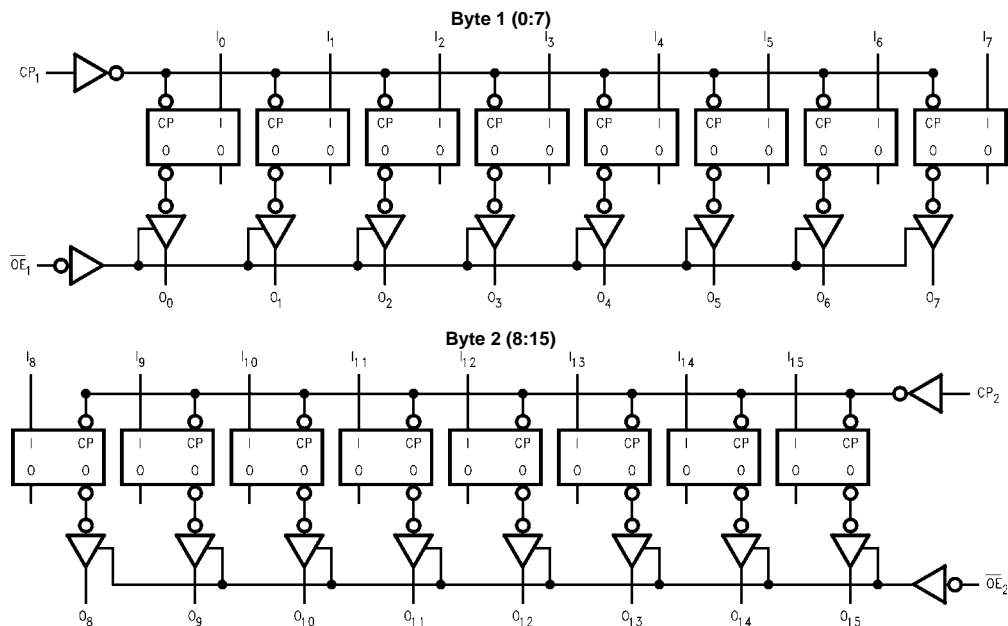
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW of CP

## Functional Description

The LCXH16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store

the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

## Logic Diagrams

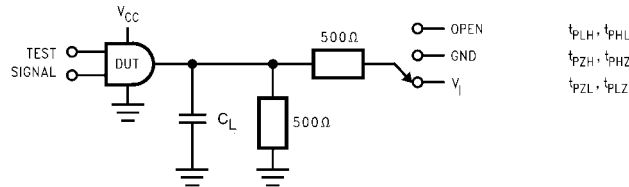


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)						
Symbol	Parameter	Value	Conditions	Units		
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V		
$V_I$	DC Input Voltage	$I_O - I_{15}$ $OE_1, CP_n$	-0.5 to $V_{CC} + 0.5$ -0.5V to 7.0V	V		
$V_O$	DC Output Voltage	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	3-STATE Output in HIGH or LOW State (Note 4)	V		
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA		
$I_{OK}$	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA		
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA		
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA		
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA		
$T_{STG}$	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 5)						
Symbol	Parameter	Min	Max	Units		
$V_{CC}$	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
$V_I$	Input Voltage	0	$V_{CC}$	V		
$V_O$	Output Voltage	HIGH or LOW State	0	$V_{CC}$	V	
		3-STATE	0	5.5		
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0V - 3.6V$		$\pm 24$	mA	
		$V_{CC} = 2.7V - 3.0V$		$\pm 12$		
		$V_{CC} = 2.3V - 2.7V$		$\pm 8$		
$T_A$	Free-Air Operating Temperature	-40	85	°C		
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V		
<p><b>Note 3:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p><b>Note 4:</b> <math>I_O</math> Absolute Maximum Rating must be observed.</p> <p><b>Note 5:</b> Floating or unused control inputs must be HIGH or LOW.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^\circ C \text{ to } +85^\circ C$		Units
				Min	Max	
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
$V_{IL}$	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
				2.3	1.8	
				2.7	2.2	
				3.0	2.4	
				3.0	2.2	
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	V
				2.3	0.6	
				2.7	0.4	
				3.0	0.4	
				3.0	0.55	
$I_I$	Input Leakage Current	Data	$V_I = V_{CC} \text{ or } GND$	2.3 - 3.6	$\pm 5.0$	$\mu A$
		Control	$0V \leq V_I \leq 5.5$	2.3 - 3.6	$\pm 5.0$	

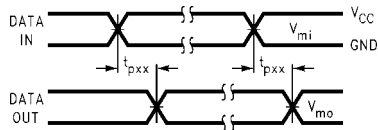
DC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units		
				Min	Max			
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive Hold Current	V <sub>IN</sub> = 0.7V	2.3	45		μA		
		V <sub>IN</sub> = 1.7V		-45				
		V <sub>IN</sub> = 0.8V	3.0	75				
		V <sub>IN</sub> = 2.0V		-75				
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	(Note 7)	2.7	300		μA		
		(Note 8)		-300				
		(Note 7)	3.6	450				
		(Note 8)		-450				
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 5.5V	2.3 – 3.6		±5.0	μA		
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>O</sub> = V <sub>CC</sub>	0		10	μA		
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		20	μA		
		3.6V ≤ V <sub>O</sub> ≤ 5.5V (Note 6)	2.3 – 3.6		±20			
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		500	μA		
<b>Note 6:</b> Outputs disabled or 3-STATE only. <b>Note 7:</b> An external driver must source at least the specified current to switch from LOW-to-HIGH. <b>Note 8:</b> An external driver must sink at least the specified current to switch from HIGH-to-LOW.								
AC Electrical Characteristics								
Symbol	Parameter	T <sub>A</sub> = -40° to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	170						MHz
t <sub>PHL</sub>	Propagation Delay	1.5	6.2	1.5	6.5	1.5	7.4	ns
t <sub>PLH</sub>	CP to O <sub>n</sub>	1.5	6.2	1.5	6.5	1.5	7.4	
t <sub>PZL</sub>	Output Enable time	1.5	6.1	1.5	6.3	1.5	7.9	ns
t <sub>PZH</sub>		1.5	6.1	1.5	6.3	1.5	7.9	
t <sub>PLZ</sub>	Output Disable Time	1.5	6.0	1.5	6.2	1.5	7.2	ns
t <sub>PHZ</sub>		1.5	6.0	1.5	6.2	1.5	7.2	
t <sub>S</sub>	Setup Time	2.5		2.5		3.0		ns
t <sub>H</sub>	Hold Time	1.5		1.5		2.0		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		3.5		ns
t <sub>OSSL</sub>	Output to Output Skew (Note 9)		1.0					ns
t <sub>OSLH</sub>			1.0					
<b>Note 9:</b> Skew is defined as the absolute value of the differences between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t <sub>OSSL</sub> ) or LOW-to-HIGH (t <sub>OSLH</sub> ). Parameter guaranteed by design.								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units			
				Typical				
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V			
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6				
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V			
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF				
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF				
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	20	pF				

**AC LOADING and WAVEFORMS** Generic for LCX Family

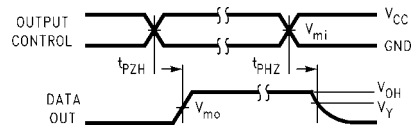


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

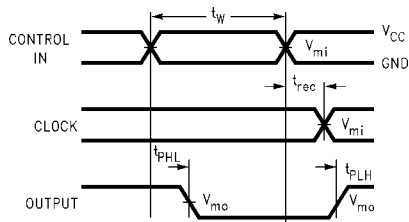
Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ , and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}$ , $t_{PHZ}$	GND



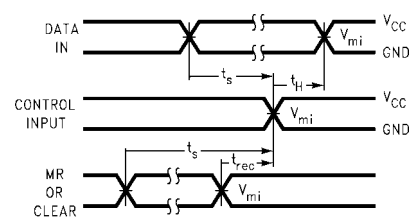
**Waveform for Inverting and Non-Inverting Functions**



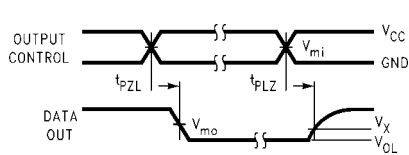
**3-STATE Output High Enable and Disable Times for Logic**



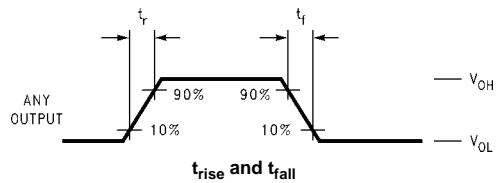
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



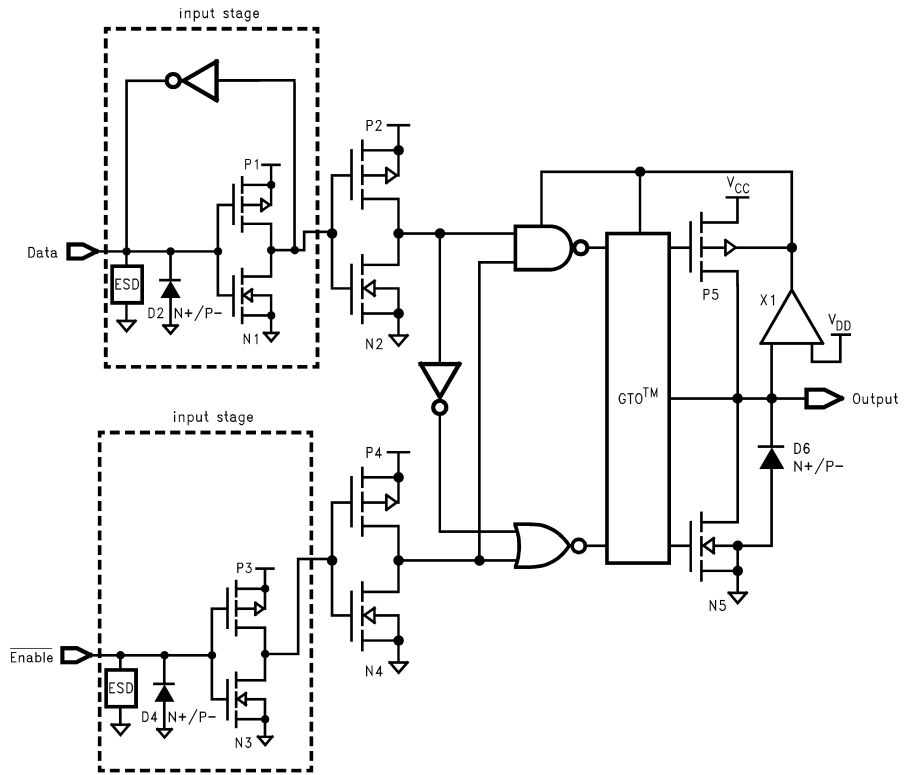
**3-STATE Output Low Enable and Disable Times for Logic**



**FIGURE 2. Waveforms (Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )**

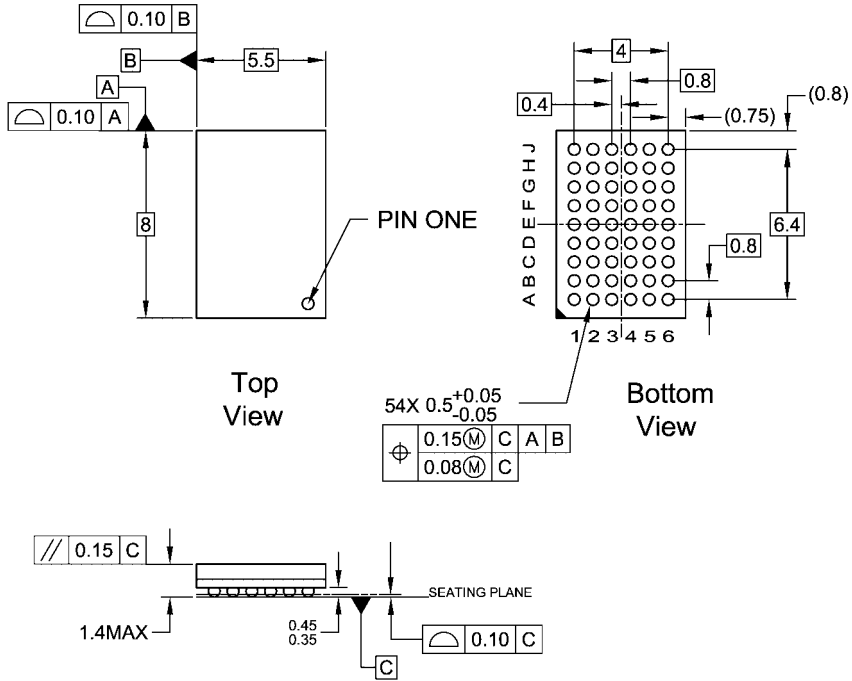
Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

**Schematic Diagram** Generic for LCXH Family (with Bushold)



74LCXH16374

**Physical Dimensions** inches (millimeters) unless otherwise noted



**NOTES:**

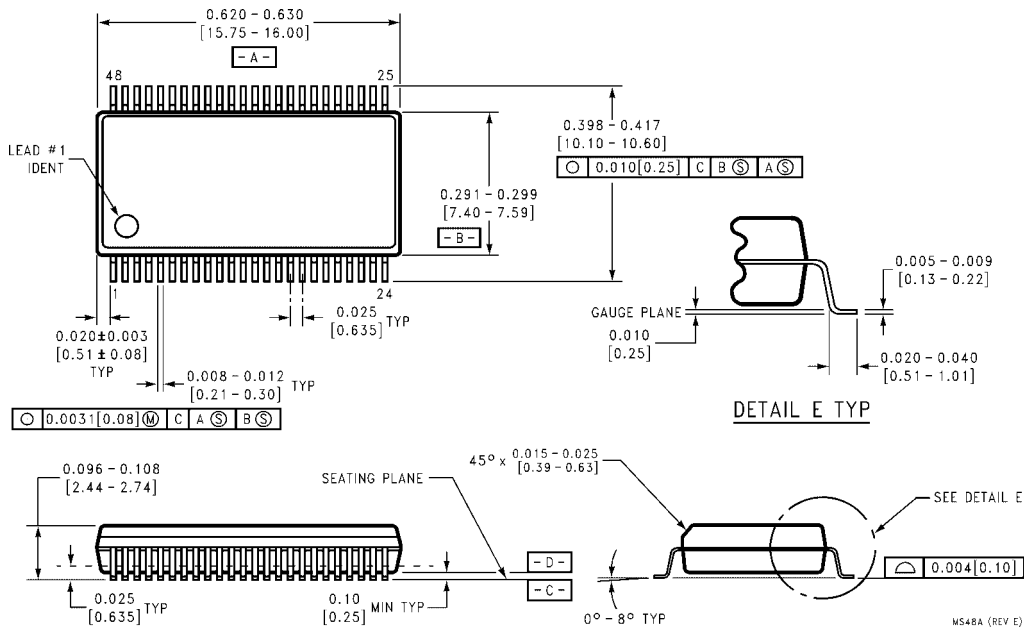
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A**



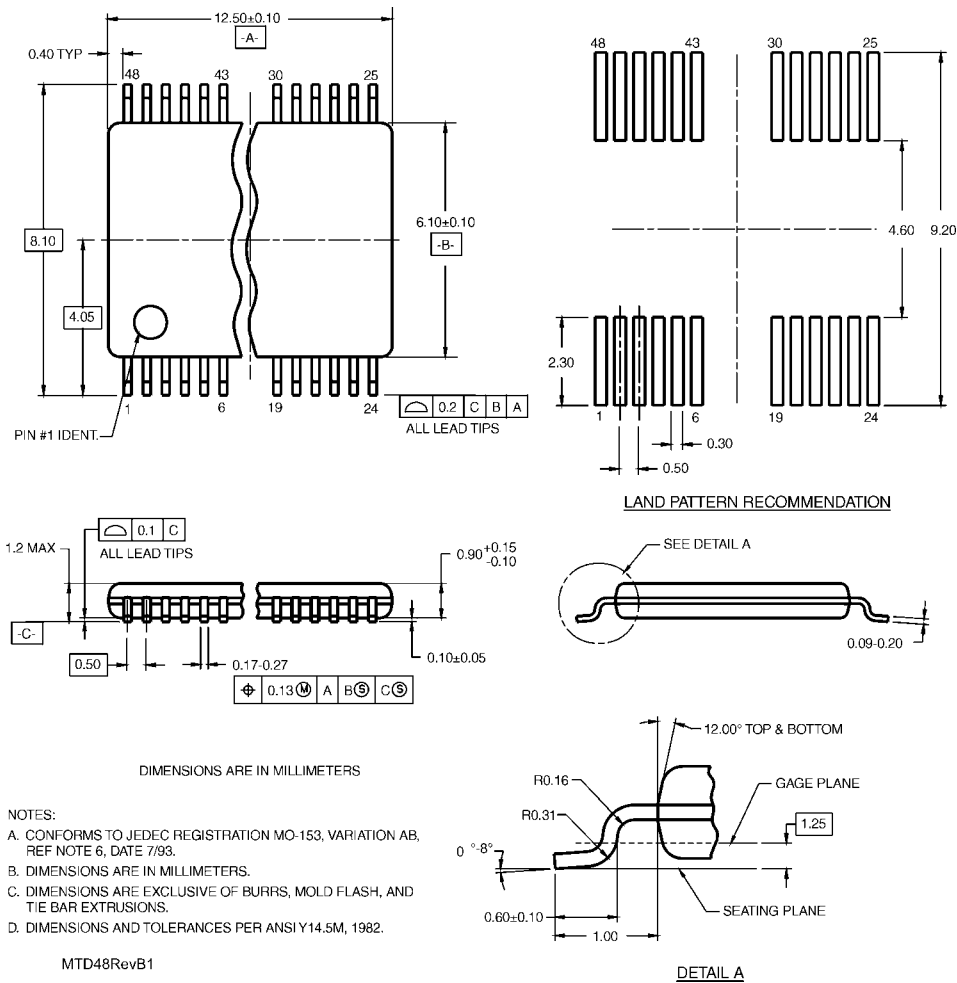
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

MS48A (REV E)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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