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T-46-09-05

# 54/74164 54LS/74LS164

## SERIAL-IN PARALLEL-OUT SHIFT REGISTER

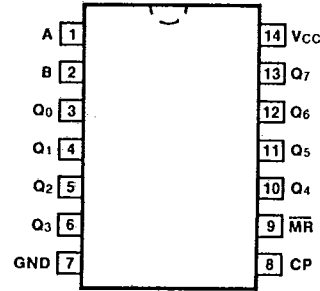
**DESCRIPTION** — The '164 is a high speed 8-bit serial-in parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds.

- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74164PC, 74LS164PC		9A
Ceramic DIP (D)	A	74164DC, 74LS164DC	54164DM, 54LS164DM	6A
Flatpak (F)	A	74164FC, 74LS164FC	54164FM, 54LS164FM	3I

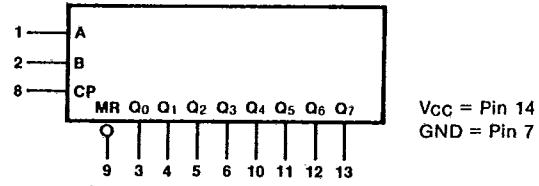
### CONNECTION DIAGRAM PINOUT A



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A, B	Data Inputs	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
Q <sub>0</sub> — Q <sub>7</sub>	Outputs	10/5.0	10/5.0 (2.5)

### LOGIC SYMBOL



**FUNCTIONAL DESCRIPTION** — The '164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q<sub>0</sub> the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

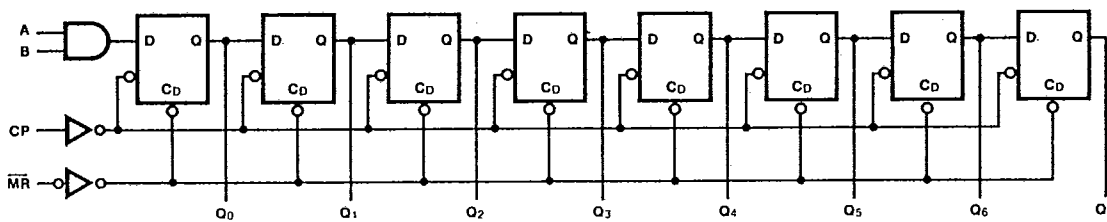
**MODE SELECT TABLE**

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q <sub>0</sub>	Q <sub>1</sub> — Q <sub>7</sub>
Reset (Clear)	L	X	X	L	L — L
Shift	H	l	l	L	q <sub>0</sub> — q <sub>6</sub>
	H	l	h	L	q <sub>0</sub> — q <sub>6</sub>
	H	h	l	L	q <sub>0</sub> — q <sub>6</sub>
	H	h	h	H	q <sub>0</sub> — q <sub>6</sub>

L (l) = LOW Voltage Levels  
 H (h) = HIGH Voltage Levels  
 X = Immaterial  
 q<sub>n</sub> = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

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
**LOGIC DIAGRAM**



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**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
I <sub>os</sub>	Output Short Circuit Current	XM	-10	-27.5	-20	-100	mA	V <sub>CC</sub> = Max
		XC	-9.0	-27.5	-20	-100		
I <sub>CC</sub>	Power Supply Current	54		27		mA	A, B = Gnd, V <sub>CC</sub> = Max CP = 2.4 V, MR = 	

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 800 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	25		25		MHz	Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	27 32		27 32		ns	Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	30 37				ns	Figs. 3-1, 3-8 C <sub>L</sub> = 50 pF
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	36		36		ns	Figs. 3-1, 3-16
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	42				ns	Figs. 3-1, 3-16 C <sub>L</sub> = 50 pF

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW A or B to CP	15		15		ns	Fig. 3-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW A or B to CP	0		5.0		ns	
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	20		20		ns	Fig. 3-8
t <sub>w</sub> (L)	MR Pulse Width LOW	20		20		ns	Fig. 3-16
t <sub>rec</sub>	Recovery Time MR to CP			20		ns	Fig. 3-16