MOTOROLA

SN54LS182
SN74LS182

CARRY LOOKAHEAD GENERATOR

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS182 is a high-speed Carry Lookahead Generator. It is generally used with the SN54LS/74LS181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The carry lookahead generator is fully compatible with all members of the Motorola TTL Family.

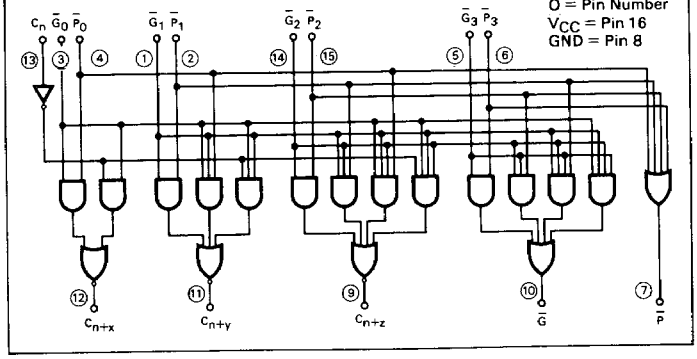
- PROVIDES CARRY LOOKAHEAD ACROSS A GROUP OF FOUR ALUs
- MULTI-LEVEL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

PIN NAMES

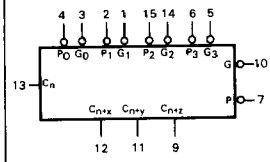
		LOADING (Note a) HIGH	LOW
C_n	Carry Input	0.5 U.L.	0.25 U.L.
$\overline{G}_0$, $\overline{G}_2$	Carry Generate (Active LOW) Inputs	3.5 U.L.	1.75 U.L.
$\overline{G}_1$	Carry Generate (Active LOW) Input	4.0 U.L.	2.0 U.L.
$\overline{G}_3$	Carry Generate (Active LOW) Input	2.0 U.L.	1.0 U.L.
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate (Active LOW) Inputs	2.0 U.L.	1.0 U.L.
$\overline{P}_2$	Carry Propagate (Active LOW) Input	1.5 U.L.	0.75 U.L.
$\overline{P}_3$	Carry Propagate (Active LOW) Input	1.0 U.L.	0.5 U.L.
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

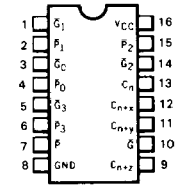


LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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FUNCTIONAL DESCRIPTION — The SN54LS/74LS182, carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The SN54LS/74LS182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$
$$C_{n+z} = \underline{G_2 + P_2G_1 = P_2P_2G_0 + P_2P_1P_0C_n}$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Also, the SN54LS/74LS182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5			V	I_{OH} = MAX	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7					
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8.0 mA	
I_{IH}	C_n $\overline{G}_0$, $\overline{G}_2$ $\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$ $\overline{P}_2$ $\overline{P}_3$ $\overline{G}_1$				20 140 80 60 40 160	μA	V_{IN} = 2.7 V V_{CC} = MAX	
	C_n $\overline{G}_0$, $\overline{G}_2$ $\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$ $\overline{P}_2$ $\overline{P}_3$ $\overline{G}_1$				0.1 0.7 0.4 0.3 0.2 0.8	mA	V_{IN} = 7.0 V V_{CC} = MAX	
I_{IL}	C_n $\overline{G}_0$, $\overline{G}_2$ $\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$ $\overline{P}_2$ $\overline{P}_3$ $\overline{G}_1$				−0.4 −2.8 −1.6 −1.2 −0.8 −3.2	mA	V_{IN} = 0.4 V V_{CC} = MAX	
I_{OS}	Output Short-Circuit Current		−20		−100	mA	V_{CC} = MAX V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				12	mA	V_{CC} = MAX	
	Total, Output LOW				16			

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AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	(C_n to C_{n+x}, C_{n+y}, C_{n+z})		12 17	25 30	ns	$\bar{P}_0 = \bar{P}_1 = \bar{P}_2 = \bar{G}$nd, $\bar{G}_0 = \bar{G}_1 = \bar{G}_2$ = 4.5 V, Fig. 1
t_{PLH} t_{PHL}	($\bar{P}_0$, $\bar{P}_1$, or $\bar{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z})		9.0 10	21 22	ns	$\bar{P}_x$ = Gnd (if not under test), $C_n = \bar{G}_0 = \bar{G}_1 = \bar{G}_2$ = 4.5 V, Fig. 2
t_{PLH} t_{PHL}	($\bar{G}_0$, $\bar{G}_1$, or $\bar{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z})		9.0 10	21 22	ns	$\bar{G}_x$ = 4.5 V (If not under test), $C_n = \bar{P}_0 = \bar{P}_1 = \bar{P}_2$ = Gnd, Fig. 2
t_{PLH} t_{PHL}	($\bar{P}_1$, $\bar{P}_2$ or $\bar{P}_3$ to $\bar{G}$)		12 8.0	24 20	ns	$\bar{P}_x$ = Gnd (If not under test), $\bar{G}_0 = \bar{G}_1 = \bar{G}_2 = \bar{G}_3 = C_n$ = 0.0 V, Fig. 1
t_{PLH} t_{PHL}	($\bar{G}_0$, $\bar{G}_1$, $\bar{G}_2$ or $\bar{G}_3$ to $\bar{G}$)		13 8.0	25 20	ns	$\bar{G}_x$ = 4.5 V (If not under test), $\bar{P}_1 = \bar{P}_2 = \bar{P}_3$ = Gnd, Fig. 1
t_{PLH} t_{PHL}	($\bar{P}_0$, $\bar{P}_1$, $\bar{P}_2$ or $\bar{P}_3$ to $\bar{P}$)		12 8.0	24 20	ns	$\bar{P}_x$ = Gnd (If not under test), Fig. 1

AC WAVEFORMS

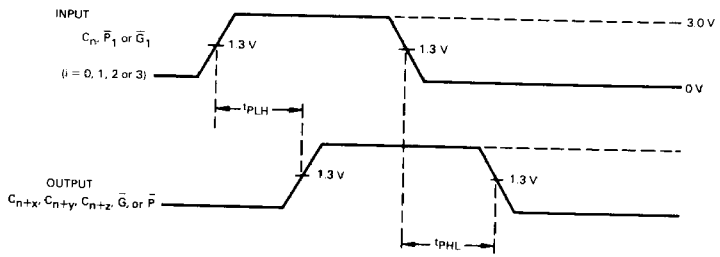

Fig.1

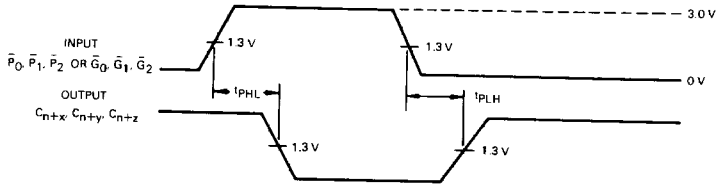

Fig. 2

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