

# HD74LS195A • 4-bit Parallel-Access Shift Registers

This 4-bit register features parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

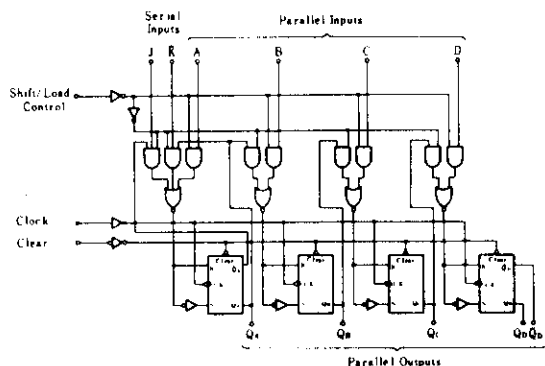
Parallel (broadside) load

Shift (in the direction  $Q_A$  toward  $Q_D$ )

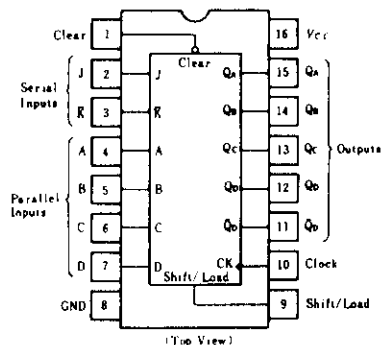
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data

is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

## ■ BLOCK DIAGRAM



## ■ PIN ARRANGEMENT



## ■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	$f_{clock}$	0	—	30	MHz
Clock pulse width	$t_w(CLK)$	16	—	—	ns
Clear pulse width	$t_w(CLR)$	12	—	—	ns
Setup time	Shift/load	25	—	—	ns
	Serial and parallel data	15	—	—	
	Clear inactive-state	25	—	—	
Release time	$t_{release}$	—	—	5	ns
Hold time	$t_h$	0	—	—	ns

## ■ FUNCTION TABLE

Clear	Shift/Load	Clock	Inputs							Outputs				
			Serial		Parallel				$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$	
			J	$\bar{K}$	A	B	C	D						
L	X	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\bar{d}$	
H	H	L	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\bar{Q}_{D0}$	
H	H	↑	L	H	X	X	X	X	$Q_{A0}$	$Q_{A0}$	$Q_{Bn}$	$Q_{Cn}$	$Q_{Cn}$	
H	H	↑	L	L	X	X	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$Q_{Cn}$	
H	H	↑	H	H	X	X	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$Q_{Cn}$	
H	H	↑	H	L	X	X	X	X	$\bar{Q}_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$	

- Notes
1. H; high level, L; low level, X; irrelevant
  2. ↑; transition from low to high level
  3. ↓; transition from high to low level
  4. a~d; the level of steady-state input at inputs A, B, C, or D, respectively

5.  $Q_{A0}$ ~ $Q_{D0}$ : the level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the indicated steady-state input conditions were established.
6.  $Q_{An}$ ~ $Q_{Dn}$ : the level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the most-recent ↑ transition of the clock.

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	$V_{IH}$		2.0	—	—	V
	$V_{IL}$		—	—	0.8	V
Output voltage	$V_{OH}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	$V_{OL}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	—	—	0.4	V
Input current	$I_{IH}$	$V_{CC}=5.25\text{V}, V_i=2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{IL}$	$V_{CC}=5.25\text{V}, V_i=0.4\text{V}$	—	—	-0.4	mA
	$I_i$	$V_{CC}=5.25\text{V}, V_i=7\text{V}$	—	—	0.1	mA
Short-circuit output current	$I_{OS}$	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current**	$I_{CC}$	$V_{CC}=5.25\text{V}$	—	14	21	mA
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V

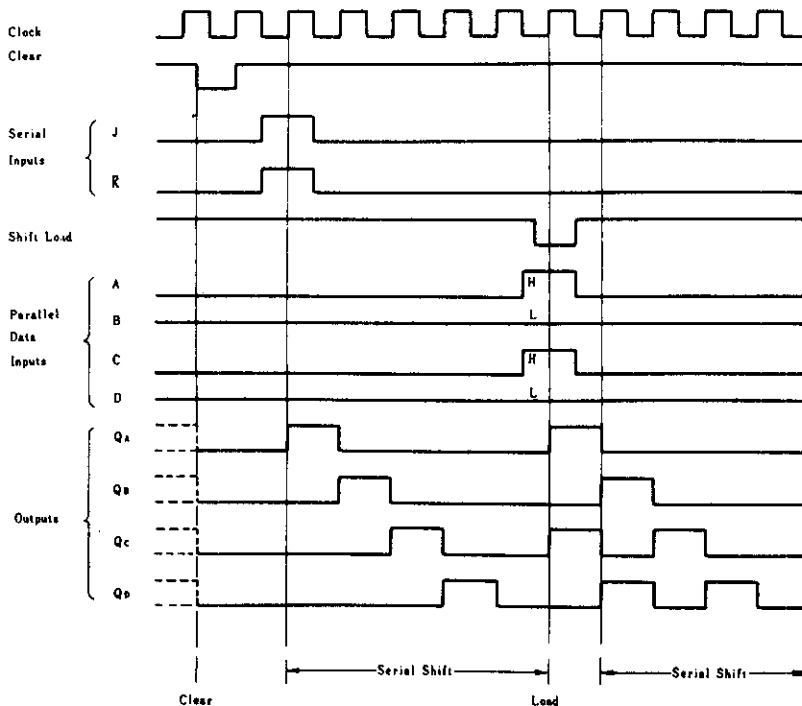
\*  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

\*\* With all outputs open, shift/load grounded, and 4.5V applied to the J,  $\bar{K}$ , and data inputs,  $I_{CC}$  is measured by applying a momentary ground, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

## ■ SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	Clock	$Q_A \sim Q_D$	$C_L=15\text{pF}$ $R_L=2\text{k}\Omega$	30	39	—	MHz
Propagation delay time	$t_{PHL}$	Clear	$Q_A \sim Q_D$		—	19	30	ns
	$t_{PLH}$	Clock	$Q_A \sim Q_D, \bar{Q}_D$		—	14	22	ns
	$t_{PHL}$				—	17	26	ns

## ■ COUNT SEQUENCE







Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g





\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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