



OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

D ₀ –D ₇	Data Inputs
LE	Latch Enable (Active HIGH) Input
CP	Clock (Active HIGH going edge) Input
OE	Output Enable (Active LOW) Input
O ₀ –O ₇	Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
D ₀ –D ₇	0.5 U.L.	0.25 U.L.
LE	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
OE	0.5 U.L.	0.25 U.L.
O ₀ –O ₇	65 (25) U.L.	15 (7.5) U.L.

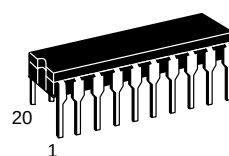
NOTES:

- a) 1 TTL Units Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

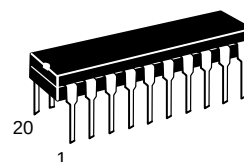
SN54/74LS373
SN54/74LS374

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WITH 3-STATE OUTPUTS;
OCTAL D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUT**

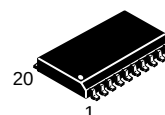
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



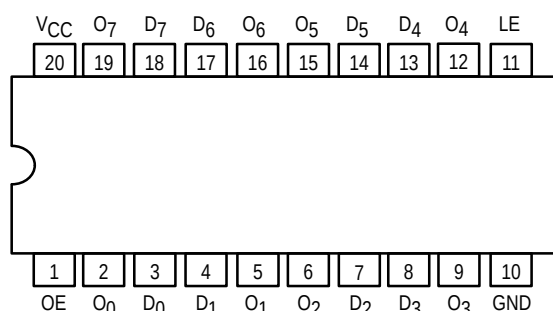
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

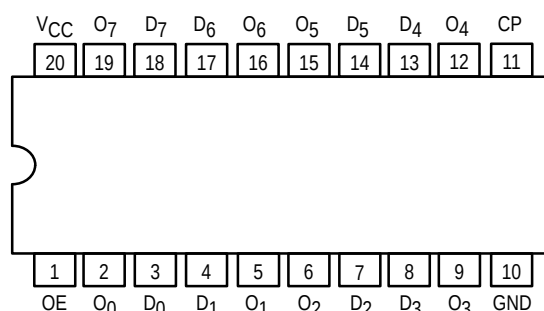
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

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NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

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TRUTH TABLE

LS373			
D _n	LE	OE	O _n
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z*

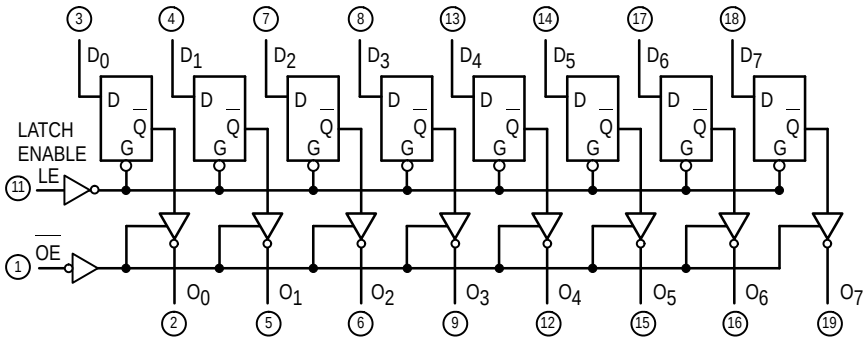
LS374			
D _n	LE	OE	O _n
H		L	H
L		L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

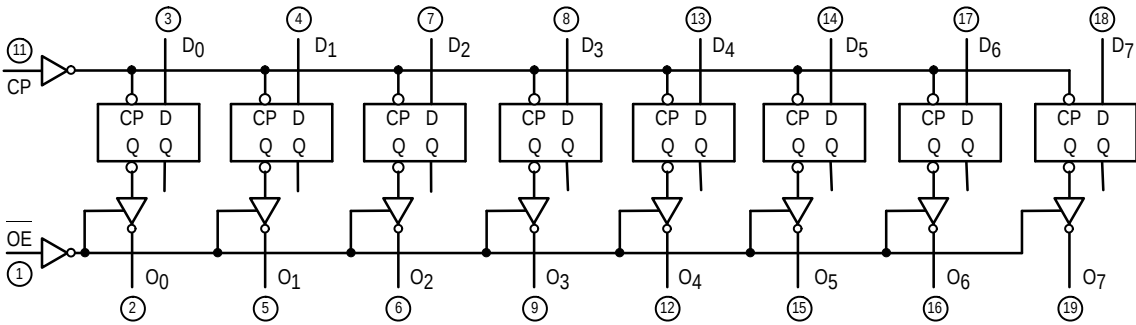
* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

LOGIC DIAGRAMS

SN54LS/74LS373



SN54LS/74LS374



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW				−20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				−0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				40	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
fMAX	Maximum Clock Frequency				35	50		MHz	C _L = 45 pF, R _L = 667 Ω
tPLH tPHL	Propagation Delay, Data to Output		12 12	18 18				ns	
tPLH tPHL	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
tPZH tPZL	Output Enable Time		15 25	28 36		20 21	28 28	ns	
tPHZ tPLZ	Output Disable Time		12 15	20 25		12 15	20 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t _W	Clock Pulse Width	15		15		ns
t _S	Setup Time	5.0		20		ns
t _H	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

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AC WAVEFORMS

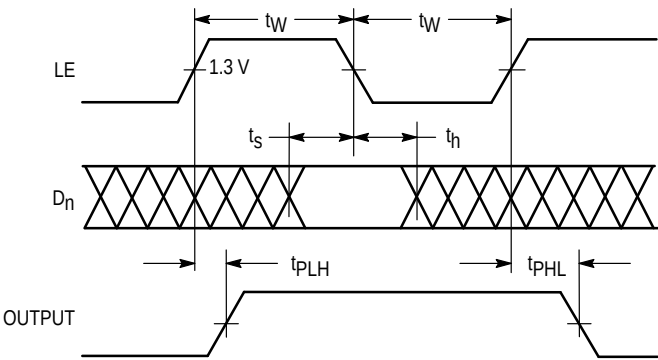


Figure 1

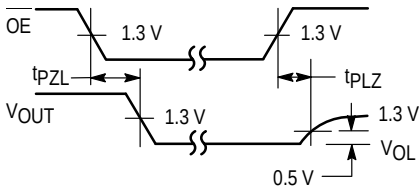


Figure 2

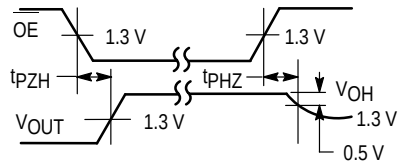
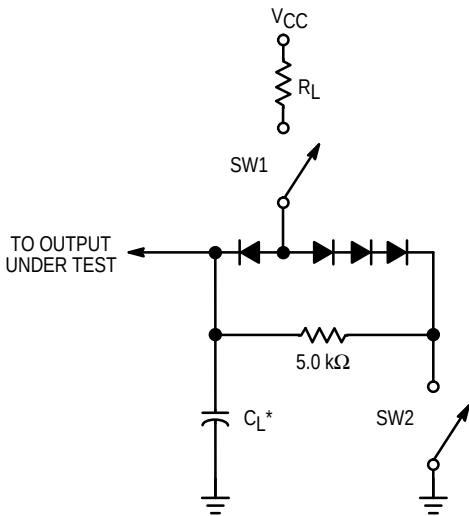


Figure 3

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 4

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

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AC WAVEFORMS

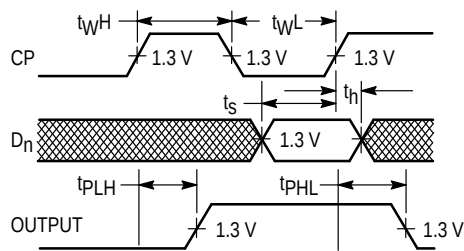


Figure 5

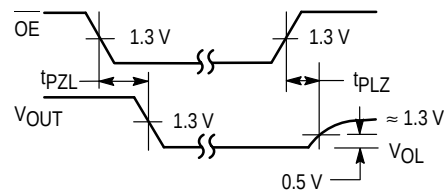


Figure 6

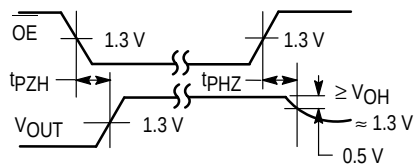
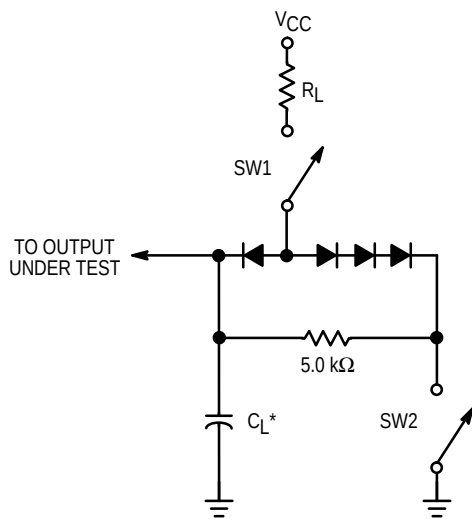


Figure 7

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

Figure 8