Signetics

Logic Products

74LS641, LS642, 74LS641-1, LS642-1 Transceivers

Octal Bus Transceiver (Open Collector)
Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **Open Collector Outputs**
  - **'LS641, non-inverting**
  - **'LS642, inverting**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**
- **48mA sink capability ('LS641-1, LS642-1)**

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	Inputs
L	H	Inputs	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z)= HIGH impedance "off" state

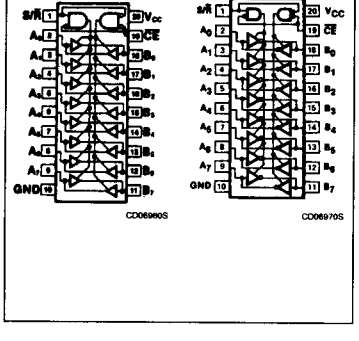
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

NOTE:
A 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

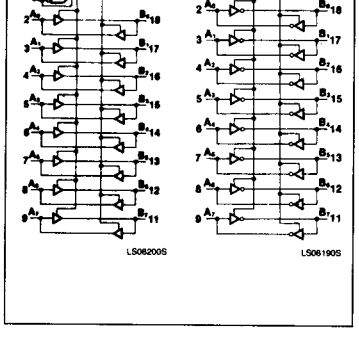
PIN CONFIGURATION

'LS641 'LS642



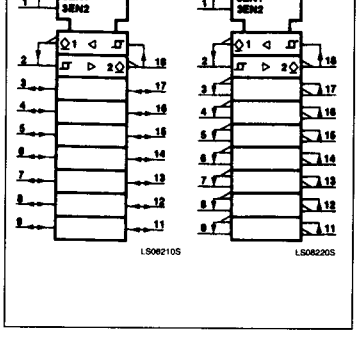
LOGIC SYMBOL

'LS641 'LS642



LOGIC SYMBOL (IEEE/IEC)

'LS641 'LS642



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.6	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current				24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74LS641			74LS641-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN, A or B input			0.2	0.4		0.2	0.4		V
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					100			100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA			0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA (74LS)			0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA (74LS-1)						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.4			−0.4	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			48	70		48	70	mA
			I_{CCL} Outputs LOW			62	90		62	90	mA
			I_{CCZ} Outputs OFF			64	95		64	95	mA

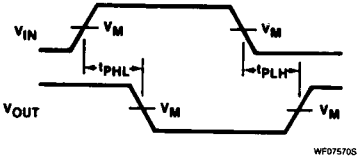
NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

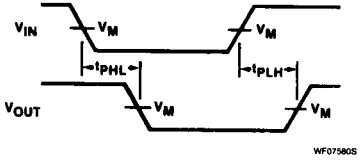
PARAMETER		TEST CONDITIONS	$C_L = 45pF$, $R_L = 667\Omega$		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1		25	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1		25	ns
t_{PLH}	Propagation delay $\overline{CE}$, S/$\overline{R}$ inputs to A output $\overline{CE}$ input to B output S/$\overline{R}$ input to B output	 Waveform 1 Waveform 1 Waveform 2		 40 40 40	ns
t_{PHL}	Propagation delay $\overline{CE}$, S/$\overline{R}$ inputs to A output $\overline{CE}$ input to B output S/$\overline{R}$ input to B output	 Waveform 2 Waveform 2 Waveform 1		 50 50 50	ns

AC WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

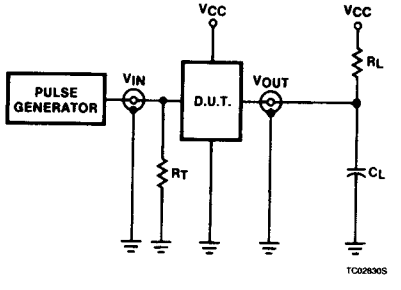
Waveform 1. Waveform For Inverting Outputs



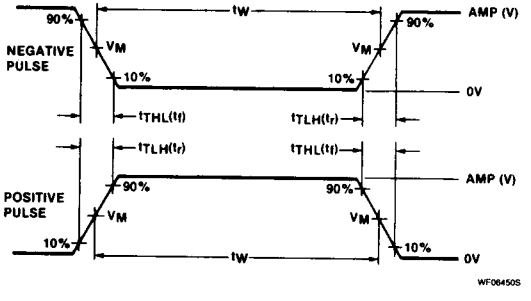
$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 2. Waveform For Non-Inverting Outputs

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns