

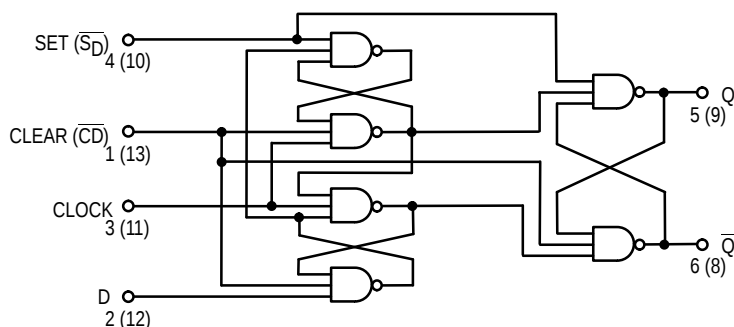


# DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and  $\bar{Q}$  outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

| OPERATING MODE   | INPUTS      |             |   | OUTPUTS |           |
|------------------|-------------|-------------|---|---------|-----------|
|                  | $\bar{S}_D$ | $\bar{C}_D$ | D | Q       | $\bar{Q}$ |
| Set              | L           | H           | X | H       | L         |
| Reset (Clear)    | H           | L           | X | L       | H         |
| *Undetermined    | L           | L           | X | H       | H         |
| Load "1" (Set)   | H           | H           | h | H       | L         |
| Load "0" (Reset) | H           | H           | l | L       | H         |

\* Both outputs will be HIGH while both  $\bar{S}_D$  and  $\bar{C}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{C}_D$  go HIGH simultaneously. If the levels at the set and clear are near  $V_{IL}$  maximum then we cannot guarantee to meet the minimum level for  $V_{OH}$ .

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

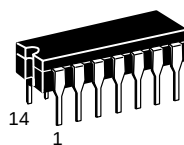
X = Don't Care

i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

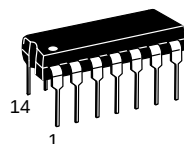
SN54/74LS74A

DUAL D-TYPE POSITIVE  
EDGE-TRIGGERED FLIP-FLOP

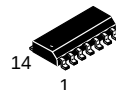
LOW POWER SCHOTTKY



J SUFFIX  
CERAMIC  
CASE 632-08



N SUFFIX  
PLASTIC  
CASE 646-06

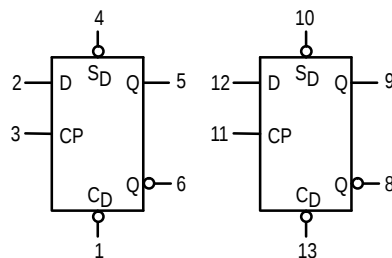


D SUFFIX  
SOIC  
CASE 751A-02

## ORDERING INFORMATION

SN54LSXXJ Ceramic  
SN74LSXXN Plastic  
SN74LSXXD SOIC

LOGIC SYMBOL



$V_{CC}$  = PIN 14  
GND = PIN 7

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## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | −55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | −0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                                       |        | Limits |       |              | Unit | Test Conditions                                                                                                    |                                                                                                             |
|-----------------|-------------------------------------------------|--------|--------|-------|--------------|------|--------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
|                 |                                                 |        | Min    | Typ   | Max          |      |                                                                                                                    |                                                                                                             |
| V <sub>IH</sub> | Input HIGH Voltage                              |        | 2.0    |       |              | V    | Guaranteed Input HIGH Voltage for All Inputs                                                                       |                                                                                                             |
| V <sub>IL</sub> | Input LOW Voltage                               | 54     |        |       | 0.7          | V    | Guaranteed Input LOW Voltage for All Inputs                                                                        |                                                                                                             |
|                 |                                                 | 74     |        |       | 0.8          |      |                                                                                                                    |                                                                                                             |
| V <sub>IK</sub> | Input Clamp Diode Voltage                       |        |        | −0.65 | −1.5         | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = −18 mA                                                                    |                                                                                                             |
| V <sub>OH</sub> | Output HIGH Voltage                             | 54     | 2.5    | 3.5   |              | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table |                                                                                                             |
|                 |                                                 | 74     | 2.7    | 3.5   |              | V    |                                                                                                                    |                                                                                                             |
| V <sub>OL</sub> | Output LOW Voltage                              | 54, 74 |        | 0.25  | 0.4          | V    | I <sub>OL</sub> = 4.0 mA                                                                                           | V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table |
|                 |                                                 | 74     |        | 0.35  | 0.5          | V    | I <sub>OL</sub> = 8.0 mA                                                                                           |                                                                                                             |
| I <sub>IH</sub> | Input High Current<br>Data, Clock<br>Set, Clear |        |        |       | 20<br>40     | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V                                                                     |                                                                                                             |
|                 | Data, Clock<br>Set, Clear                       |        |        |       | 0.1<br>0.2   | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V                                                                     |                                                                                                             |
| I <sub>IL</sub> | Input LOW Current<br>Data, Clock<br>Set, Clear  |        |        |       | −0.4<br>−0.8 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V                                                                     |                                                                                                             |
| I <sub>OS</sub> | Output Short Circuit Current (Note 1)           |        | −20    |       | −100         | mA   | V <sub>CC</sub> = MAX                                                                                              |                                                                                                             |
| I <sub>CC</sub> | Power Supply Current                            |        |        |       | 8.0          | mA   | V <sub>CC</sub> = MAX                                                                                              |                                                                                                             |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

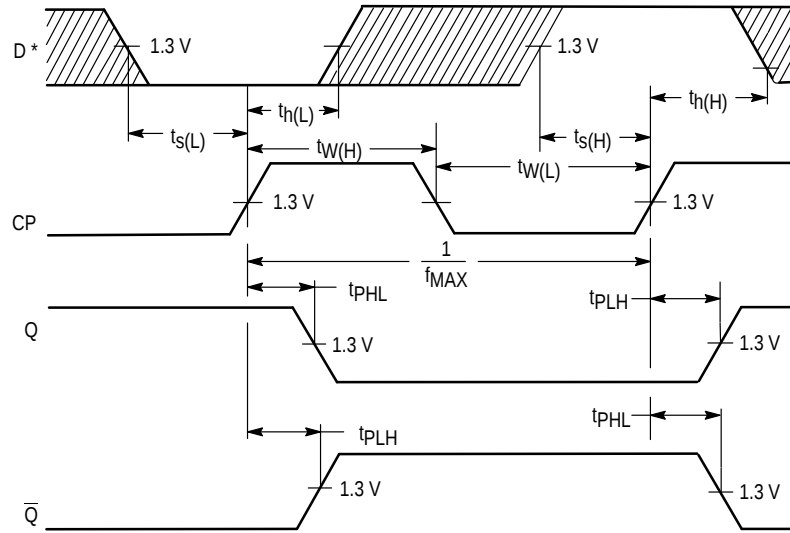
| Symbol                               | Parameter                   | Limits |     |     | Unit | Test Conditions |                                                   |
|--------------------------------------|-----------------------------|--------|-----|-----|------|-----------------|---------------------------------------------------|
|                                      |                             | Min    | Typ | Max |      |                 |                                                   |
| f <sub>MAX</sub>                     | Maximum Clock Frequency     | 25     | 33  |     | MHz  | Figure 1        | V <sub>CC</sub> = 5.0 V<br>C <sub>L</sub> = 15 pF |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Clock, Clear, Set to Output |        | 13  | 25  | ns   | Figure 1        |                                                   |
|                                      |                             |        | 25  | 40  | ns   |                 |                                                   |

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

| Symbol            | Parameter                     | Limits |     |     | Unit | Test Conditions |                         |
|-------------------|-------------------------------|--------|-----|-----|------|-----------------|-------------------------|
|                   |                               | Min    | Typ | Max |      |                 |                         |
| t <sub>W(H)</sub> | Clock                         | 25     |     |     | ns   | Figure 1        | V <sub>CC</sub> = 5.0 V |
| t <sub>W(L)</sub> | Clear, Set                    | 25     |     |     | ns   | Figure 2        |                         |
| t <sub>s</sub>    | Data Setup Time — HIGH<br>LOW | 20     |     |     | ns   | Figure 1        |                         |
|                   |                               | 20     |     |     | ns   |                 |                         |
| t <sub>h</sub>    | Hold Time                     | 5.0    |     |     | ns   | Figure 1        |                         |

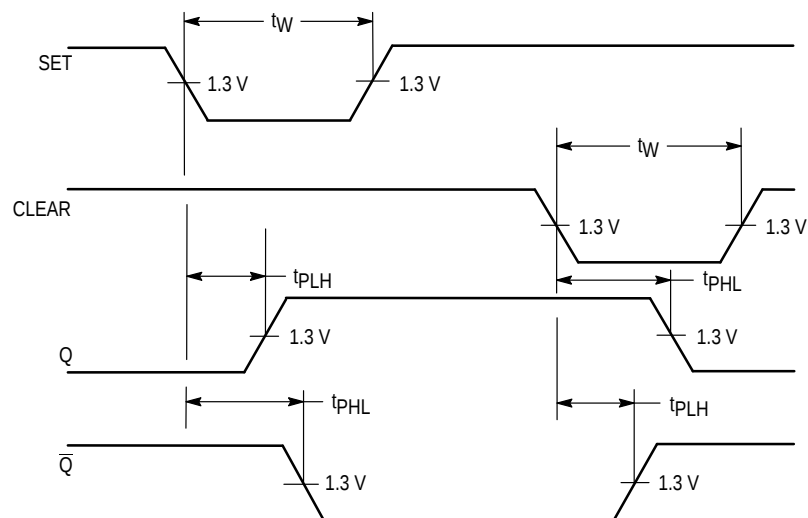
# SN54/74LS74A

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width**



**Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths**