DATA SHEET

74LV109
Dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 1997 Jun 06
IC24 Data Handbook

1998 Apr 20

Philips
Semiconductors

PHILIPS

Dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger — 74LV109

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV109 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT109.

The 74LV109 is a dual positive-edge triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table. The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The J$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF; V_{CC} = 3.3 V	 14 12 12	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	20	pF

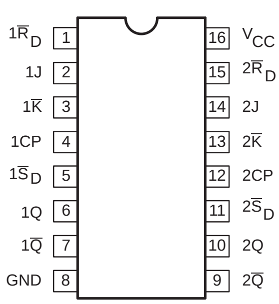
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV109 N	74LV109 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV109 D	74LV109 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV109 DB	74LV109 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV109 PW	74LV109PW DH	SOT403-1

PIN CONFIGURATION



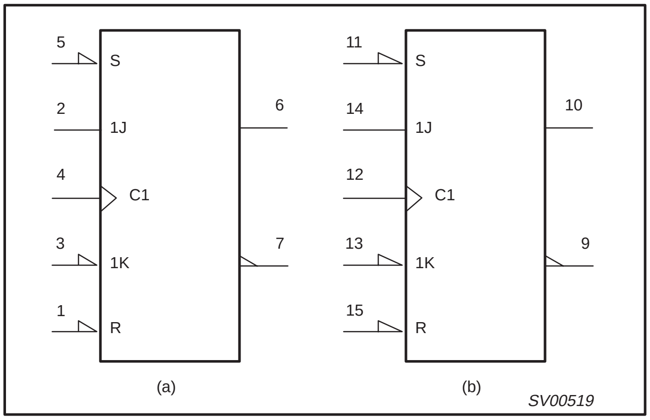
SV00517

PIN DESCRIPTION

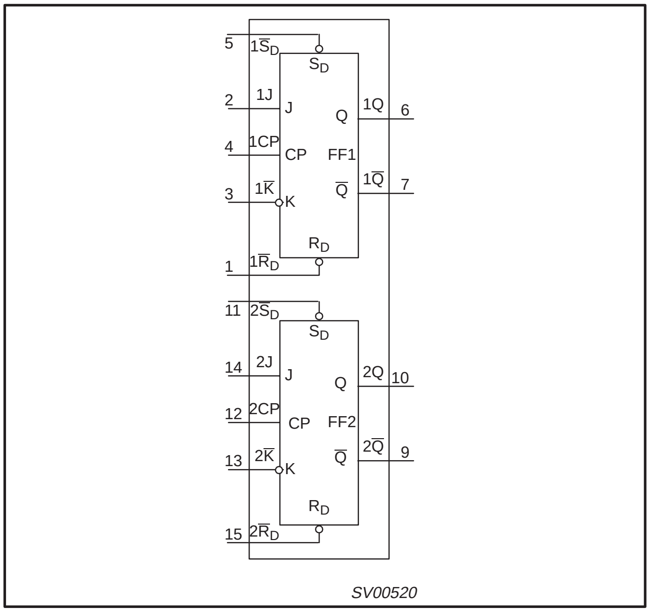
PIN NUMBER	SYMBOL	FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	Synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	True flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

Dual J$\overline{\text{K}}$ flip-flop with set and reset; positive-edge trigger 74LV109

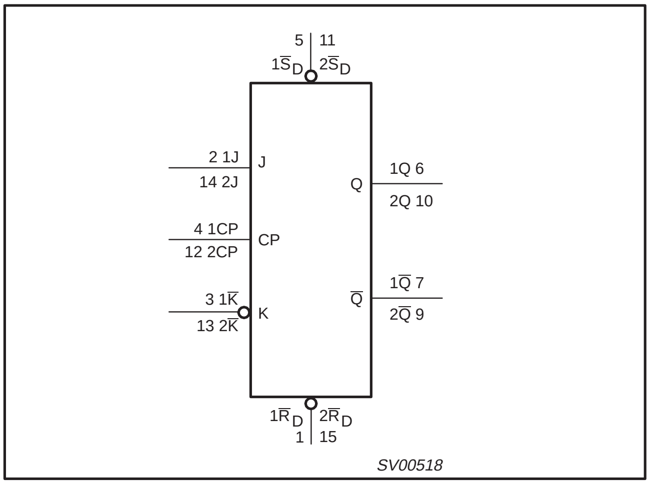
LOGIC SYMBOL (IEEE/IEC)



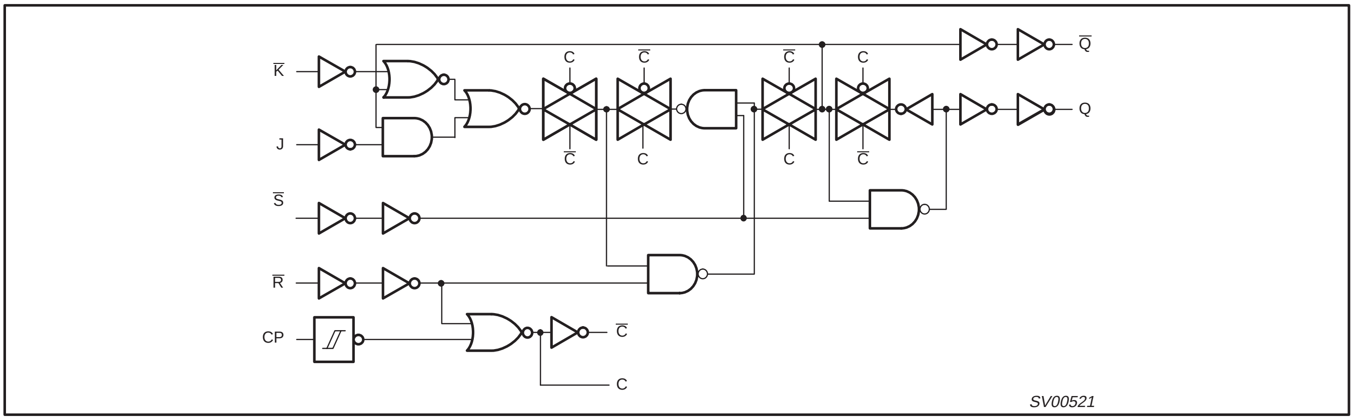
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load “0” (reset)	H	H	↑	l	l	L	H
Load “1” (set)	H	H	↑	h	h	H	L
Hold “no change”	H	H	↑	l	h	q	$\overline{q}$

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
X = don’t care
↑ = LOW-to-HIGH CP transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	V_I < –0.5 or V_I > V_{CC} + 0.5V	20	mA
$\pm I_{OK}$	DC output diode current	V_O < –0.5 or V_O > V_{CC} + 0.5V	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	–0.5V < V_O < V_{CC} + 0.5V	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTE:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40°C to +85°C MIN	TYP[1]	MAX	LIMITS -40°C to +125°C MIN	MAX	UNIT
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; flip-flops	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			20.0		80	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION V_{CC}(V)	LIMITS –40 to +85 °C MIN	TYP[1]	MAX	LIMITS –40 to +125 °C MIN	MAX	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, $n\overline{Q}$	Figure 1	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		18[2]	34		41	
t_{PLH}	Propagation delay $n\overline{S}_D$ to nQ	Figure 2	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}	Propagation delay $n\overline{S}_D$ to $n\overline{Q}$	Figure 2	1.2		75				ns
			2.0		26	46		60	
			2.7		19	36		44	
			3.0 to 3.6		17[2]	29		35	
t_{PHL}	Propagation delay $n\overline{R}_D$ to nQ	Figure 2	1.2		75				ns
			2.0		26	46		60	
			2.7		19	36		44	
			3.0 to 3.6		15[2]	29		35	
t_{PLH}	Propagation delay $n\overline{R}_D$ to $n\overline{Q}$	Figure 2	1.2		70				ns
			2.0		24	44		54	
			2.7		18	33		40	
			3.0 to 3.6		13[2]	26		32	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	12		41		ns
			2.7	25	9		30		
			3.0 to 3.6	20	7[2]		24		
t_W	Set or reset pulse width HIGH or LOW	Figure 2	2.0	34	9		41		ns
			2.7	25	6		30		
			3.0 to 3.6	20	5[2]		24		
t_{rem}	Removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	Figure 2	1.2		35				ns
			2.0	24	12		29		
			2.7	18	9		21		
			3.0 to 3.6	14	7[2]		17		
t_{su}	Set-up time nJ, $n\overline{K}$ to CP	Figure 1	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_h	Hold time nJ, $n\overline{K}$ to nCP	Figure 1	1.2		–5				ns
			2.0	5	–2		5		
			2.7	5	–1		5		
			3.0 to 3.6	5	0[2]		5		
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70[2]		20		

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

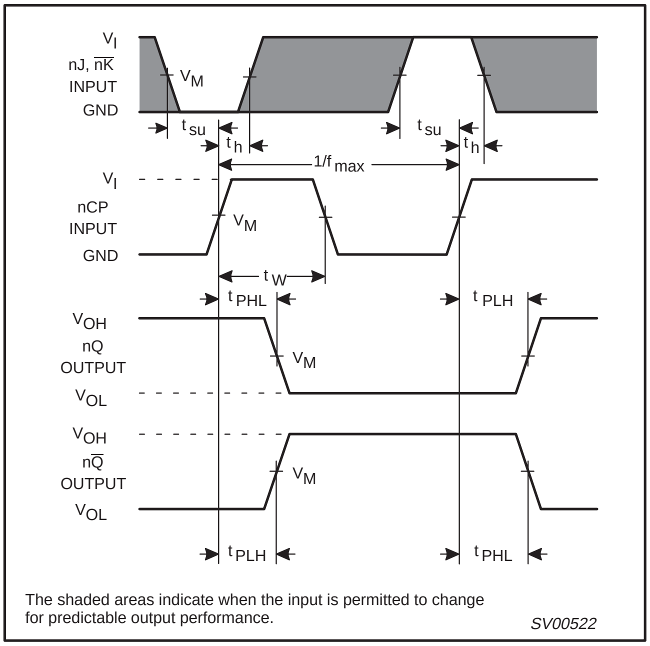


Figure 1. Clock (nCP) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the nJ and n$\overline{K}$ to nCP set-up, the nCP to nJ, n$\overline{K}$ hold times and the maximum clock pulse frequency.

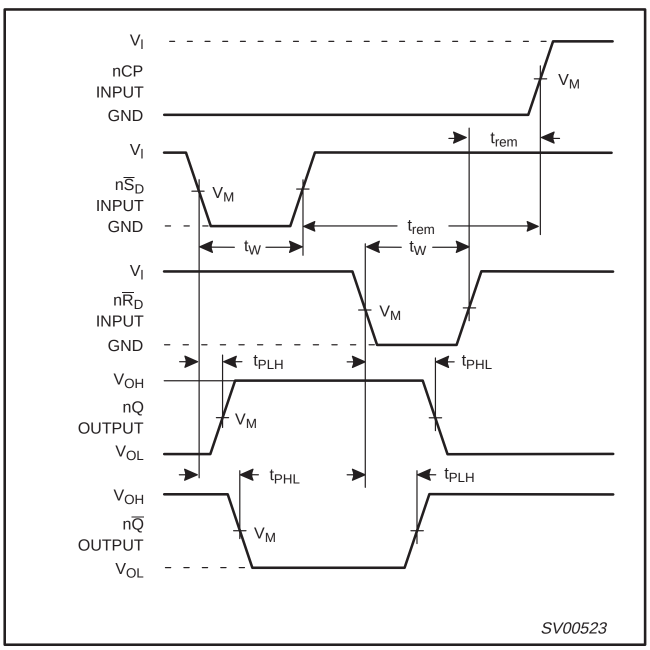
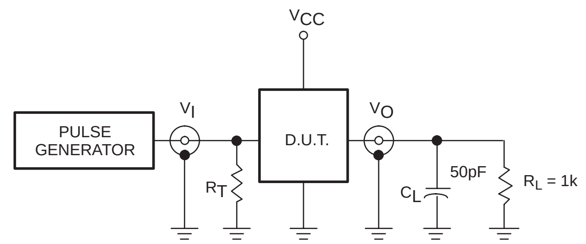


Figure 2. Set (n$\overline{S}_D$) and reset (n$\overline{R}_D$) input to output (nQ, n$\overline{Q}$) propagation delays, the set and reset pulse widths and the n$\overline{R}_D$, n$\overline{S}_D$ to nCP removal time.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

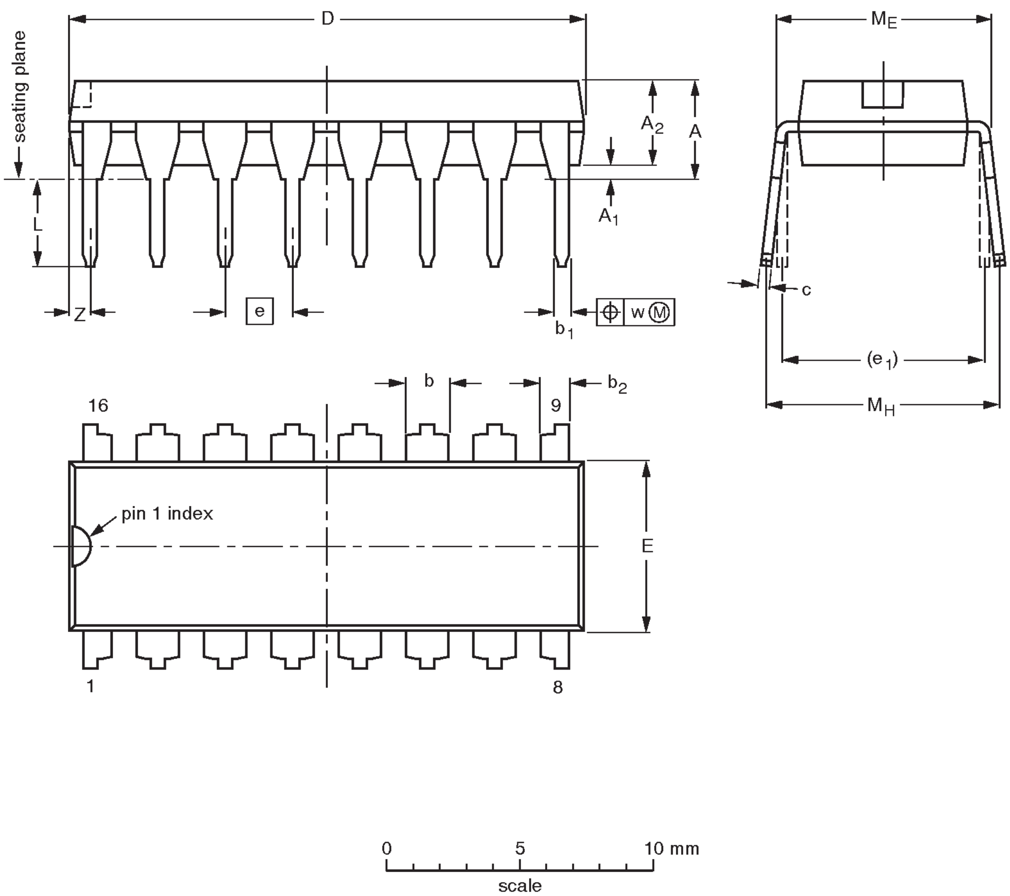
TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00901

Figure 3. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil) — SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

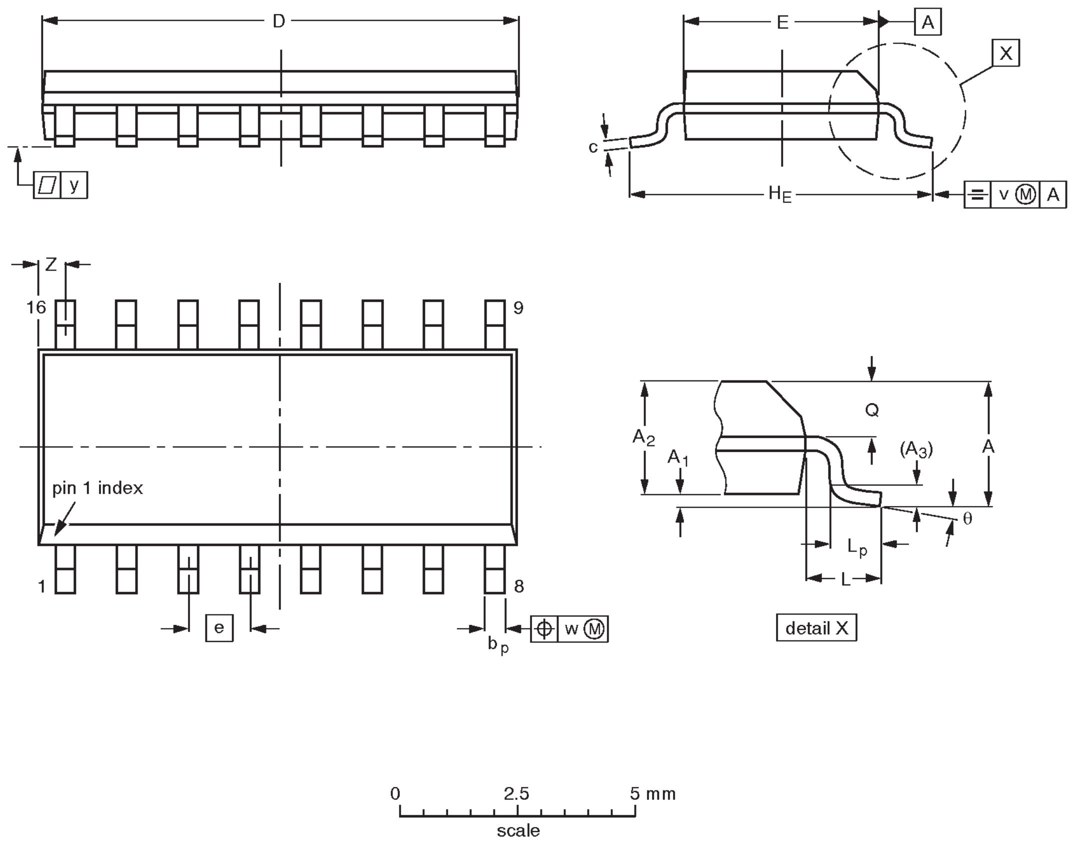
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

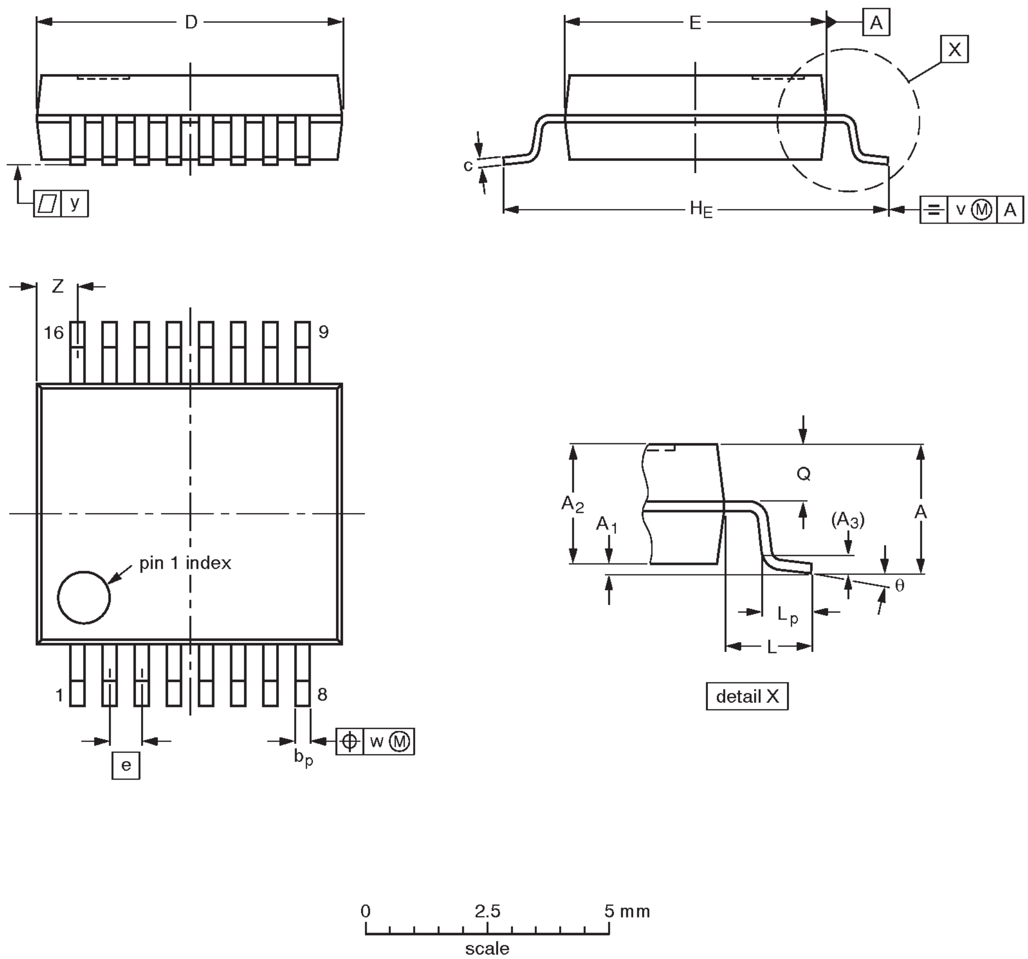
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

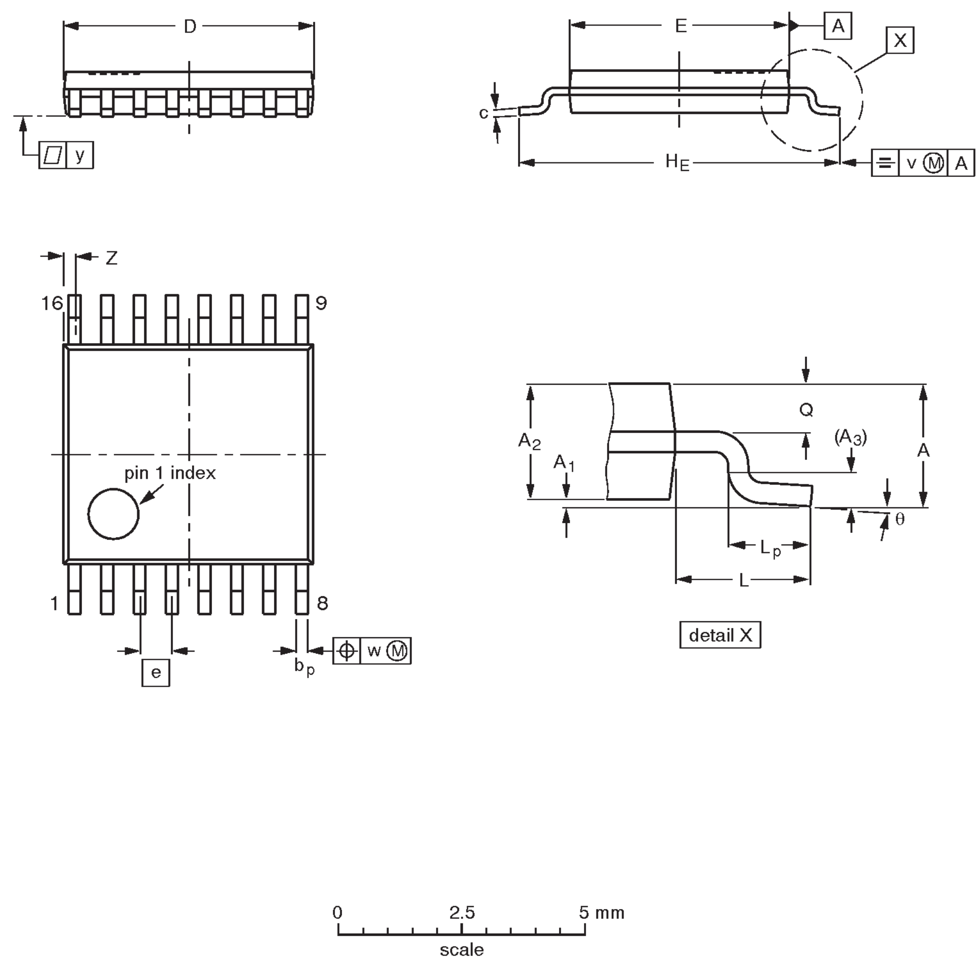
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [1]	E [2]	e	H_E	L	L_p	Q	v	w	y	Z [1]	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

Dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger 74LV109

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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