74LV14

Hex inverting Schmitt trigger

Rev. 6 — 12 December 2011 Product data sheet

1. General description

The 74LV14 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC14 and 74HCT14.

The 74LV14 provides six inverting buffers with Schmitt-trigger input. It is capable of transforming slowly-changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the input hysteresis voltage V_H.

2. Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV14N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV14D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV14DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV14PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV14BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

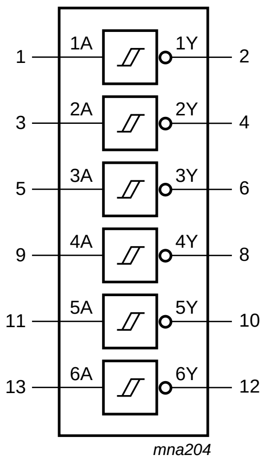


Fig 1. Logic symbol

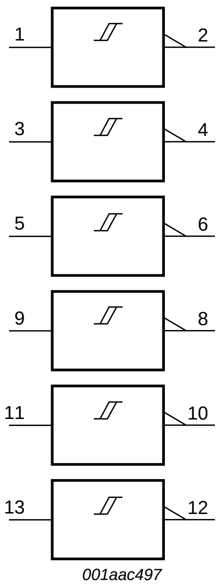


Fig 2. IEC logic symbol

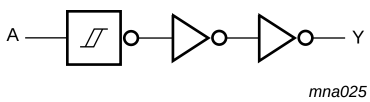


Fig 3. Logic diagram for one Schmitt trigger

6. Pinning information

6.1 Pinning

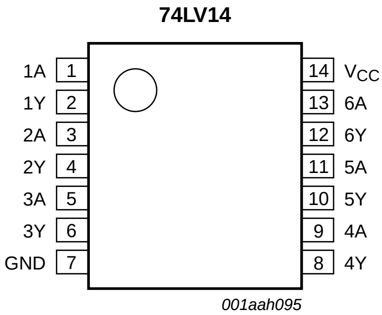
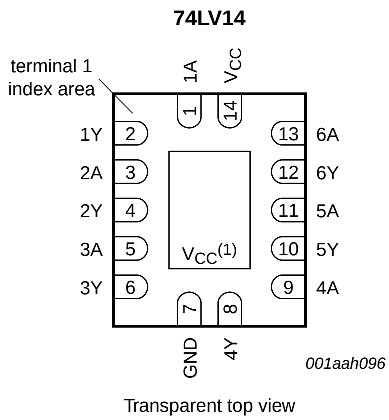


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V_{CC}	14	supply voltage

7. Functional description

Table 3. Function table
H = HIGH voltage level; L = LOW voltage level.

Input nA	Output nY
L	H
H	L

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	$V_O = –0.5$ V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
	DIP14 package		[2]	-	750	mW
	SO14 package		[3]	-	500	mW
	(T)SSOP14 package		[4]	-	500	mW
	DHVQFN14 package		[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature			–40	+25	+125	°C

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

10. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = –100 μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = –100 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = –100 μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = –100 μA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I_O = –100 μA; V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.6	4.2	-	3.5	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	-	40	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	80	-	-	-	ns
		V_{CC} = 2.0 V		-	27	37	-	48	ns
		V_{CC} = 2.7 V		-	20	28	-	35	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	13	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	15	22	-	28	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	18	-	23	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	15	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

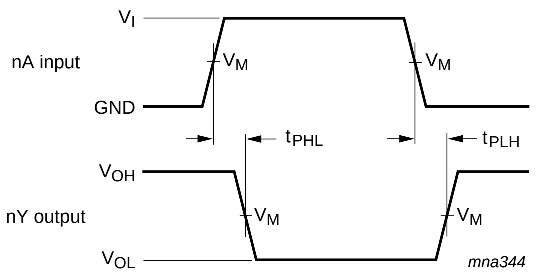
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms



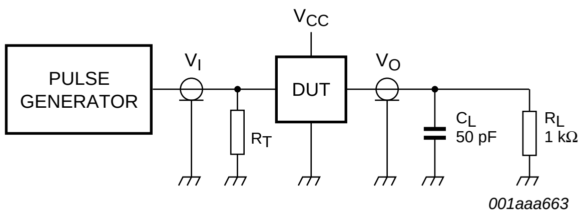
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage V_{CC}	Input V_M	Output V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Load circuit for switching times

Table 9. Test data

Supply voltage	Input	
V_{CC}	V_I	t_r, t_f
< 2.7 V	V_{CC}	≤ 2.5 ns
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns
≥ 4.5 V	V_{CC}	≤ 2.5 ns

13. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Figure 8 and Figure 9.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	V_{CC} = 1.2 V	-	0.70	-	-	-	V
		V_{CC} = 2.0 V	0.8	1.10	1.4	0.8	1.4	V
		V_{CC} = 2.7 V	1.0	1.45	2.0	1.0	2.0	V
		V_{CC} = 3.0 V	1.2	1.60	2.2	1.2	2.2	V
		V_{CC} = 3.6 V	1.5	1.95	2.4	1.5	2.4	V
		V_{CC} = 4.5 V	1.7	2.50	3.15	1.7	3.15	V
		V_{CC} = 5.5 V	2.1	3.00	3.85	2.1	3.85	V

Table 10. Transfer characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Figure 8 and Figure 9.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{T-}	negative-going threshold voltage	V_{CC} = 1.2 V	-	0.34	-	-	-	V
		V_{CC} = 2.0 V	0.3	0.65	0.9	0.3	0.9	V
		V_{CC} = 2.7 V	0.4	0.90	1.4	0.4	1.4	V
		V_{CC} = 3.0 V	0.6	1.05	1.5	0.6	1.5	V
		V_{CC} = 3.6 V	0.8	1.30	1.8	0.8	1.8	V
		V_{CC} = 4.5 V	0.9	1.60	2.0	0.9	2.0	V
		V_{CC} = 5.5 V	1.1	2.00	2.6	1.1	2.6	V
V_H	hysteresis voltage	V_{CC} = 1.2 V	-	0.3	-	-	-	V
		V_{CC} = 2.0 V	0.2	0.55	0.8	0.2	0.8	V
		V_{CC} = 2.7 V	0.3	0.60	1.1	0.3	1.1	V
		V_{CC} = 3.0 V	0.4	0.65	1.2	0.4	1.2	V
		V_{CC} = 3.6 V	0.4	0.70	1.2	0.4	1.2	V
		V_{CC} = 4.5 V	0.4	0.80	1.4	0.4	1.4	V
		V_{CC} = 5.5 V	0.6	1.00	1.5	0.6	1.5	V

[1] All typical values are measured at T_{amb} = 25 °C.

14. Waveforms transfer characteristics

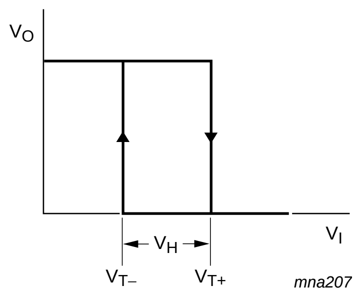
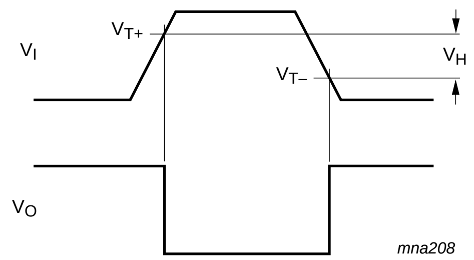
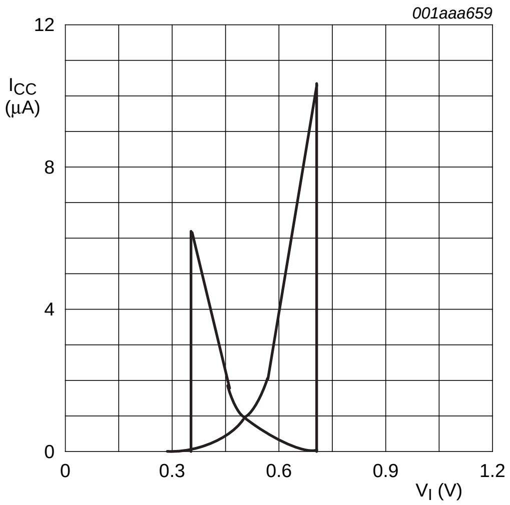


Fig 8. Transfer characteristic



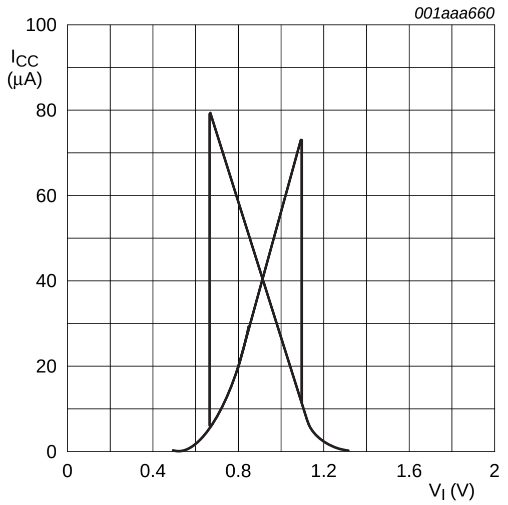
V_{T+} and V_{T-} limits at 70 % and 20 %.

Fig 9. Definition of V_{T+}, V_{T-} and V_H



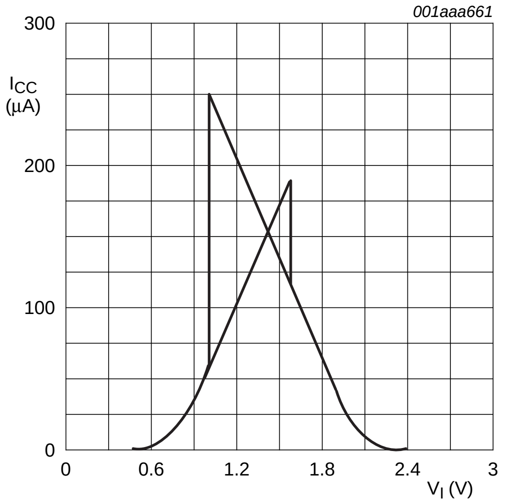
V_{CC} = 1.2 V.

Fig 10. Typical 74LV14 transfer characteristics



V_{CC} = 2.0 V.

Fig 11. Typical 74LV14 transfer characteristics



V_{CC} = 3.0 V.

Fig 12. Typical 74LV14 transfer characteristics

15. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

P_{add} = additional power dissipation (μW);

f_i = input frequency (MHz);

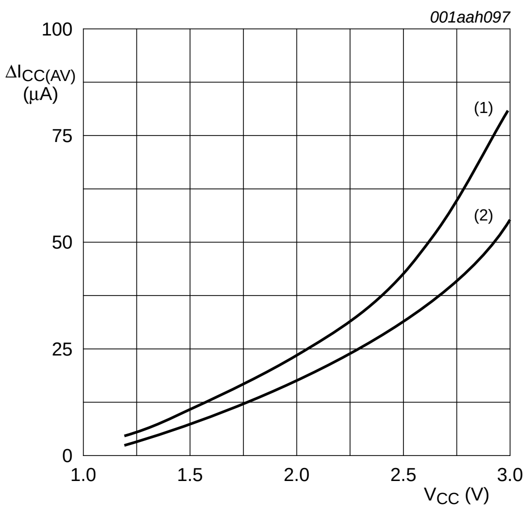
t_r = rise time (ns); 10 % to 90 %;

t_f = fall time (ns); 90 % to 10 %;

$\Delta I_{CC(AV)}$ = average additional supply current (μA).

Average $\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Figure 13.

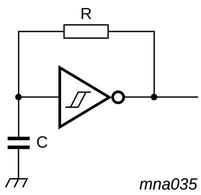
An example of a relaxation circuit using the 74LV14 is shown in Figure 14.



(1) Positive-going edge.

(2) Negative-going edge.

Fig 13. Average additional supply current as a function of V_{CC}

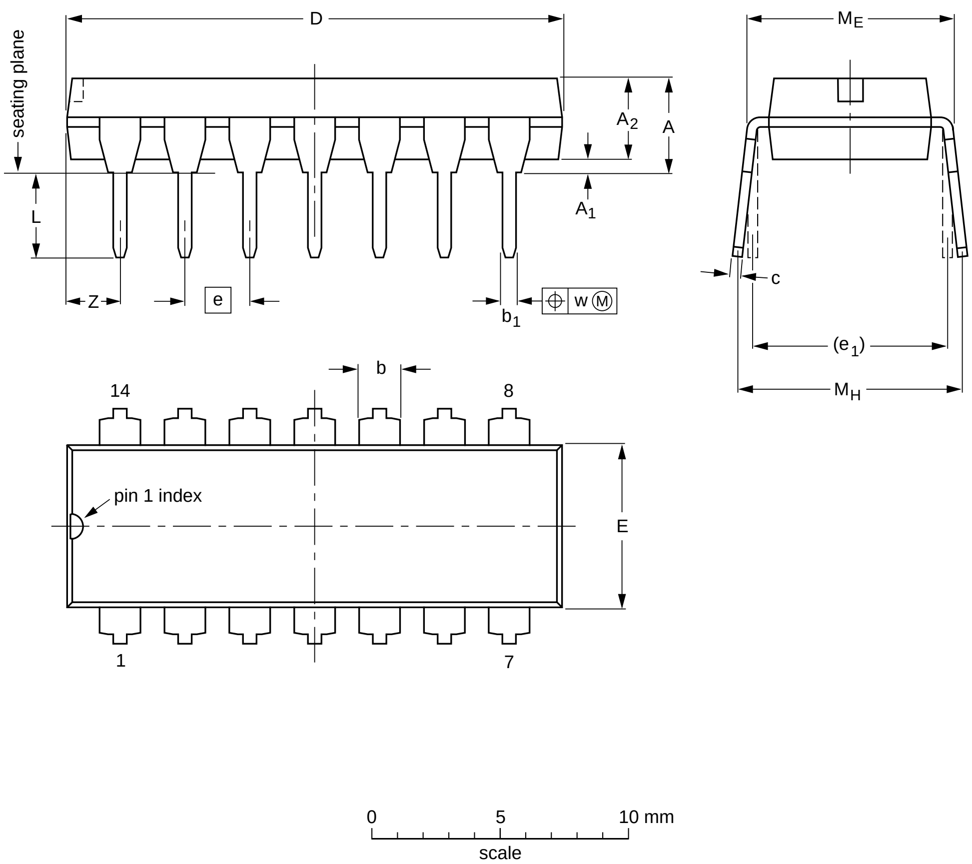


$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

Fig 14. Relaxation oscillator

16. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

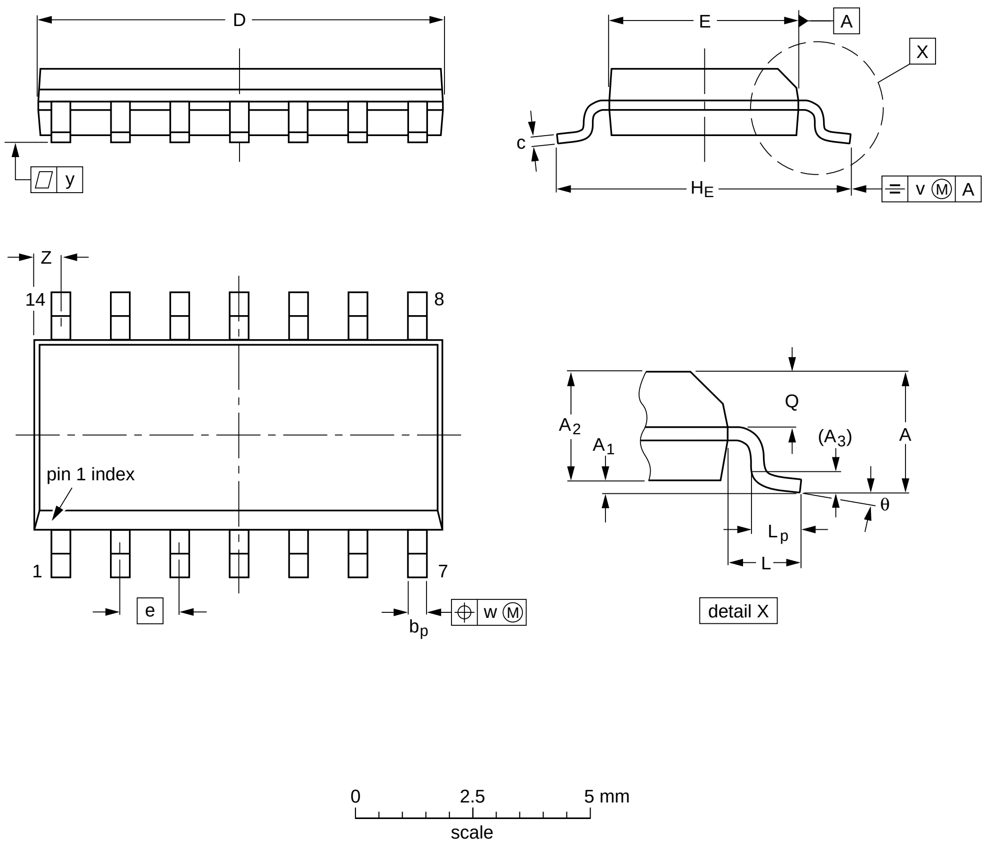
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 15. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

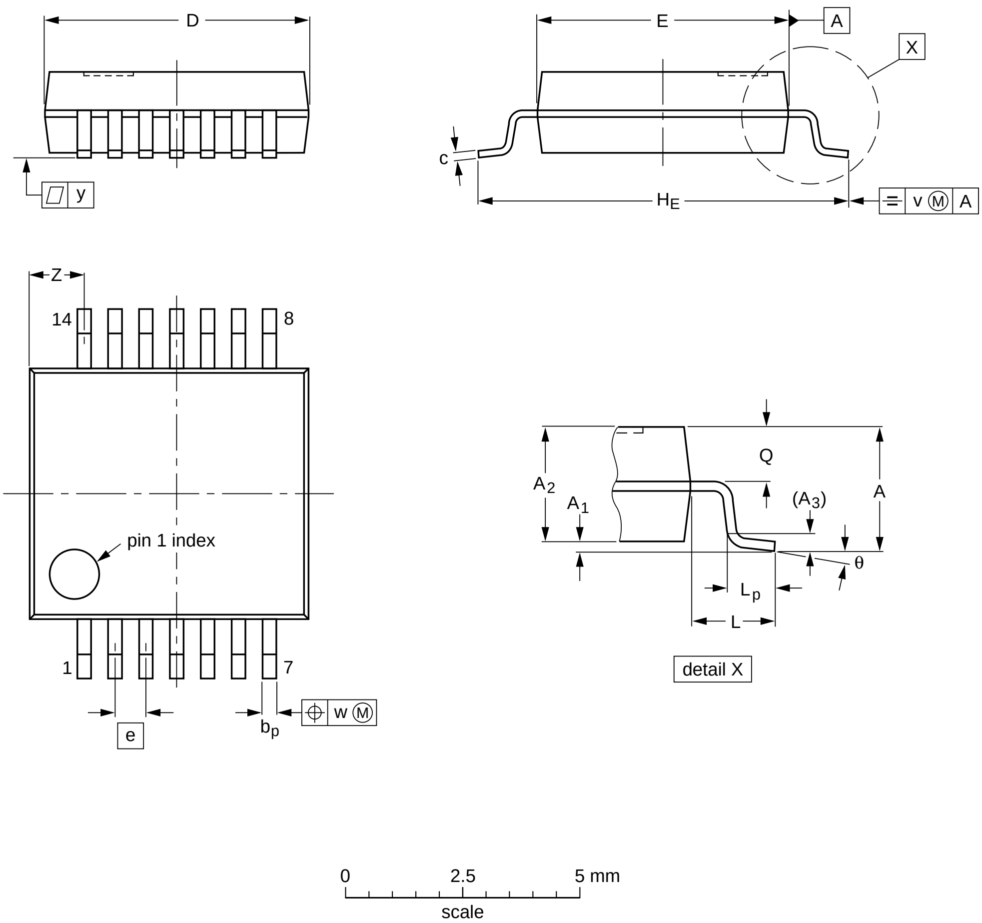
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

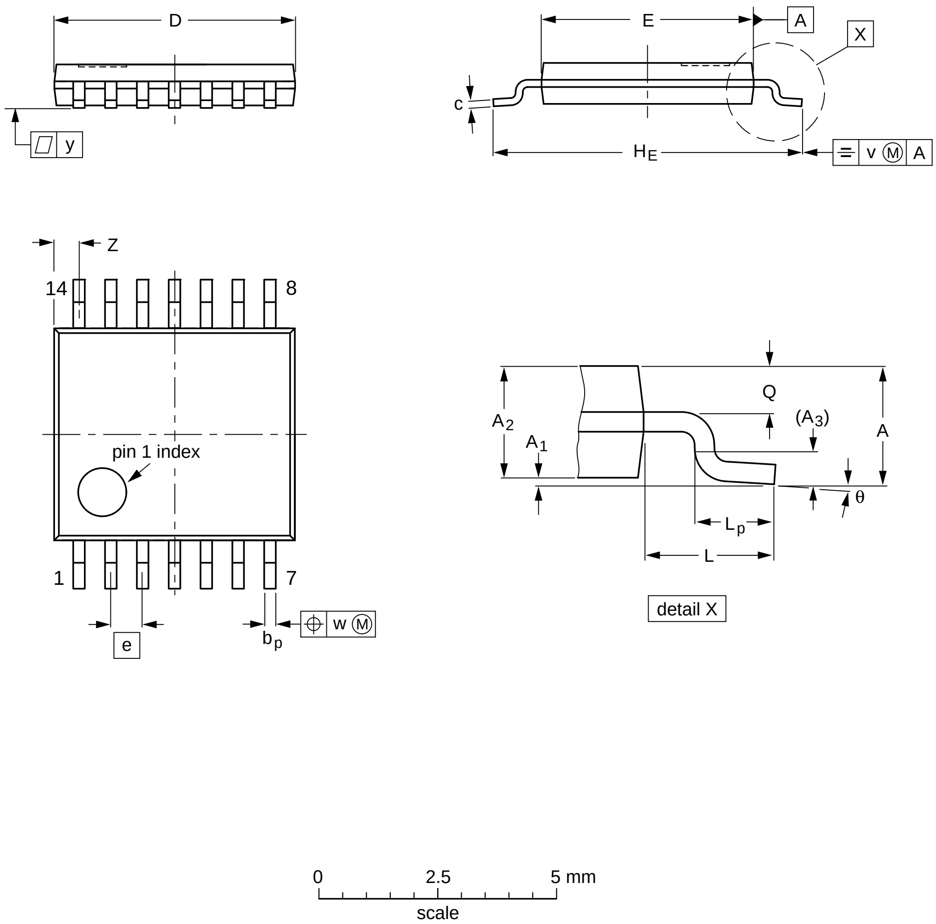
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

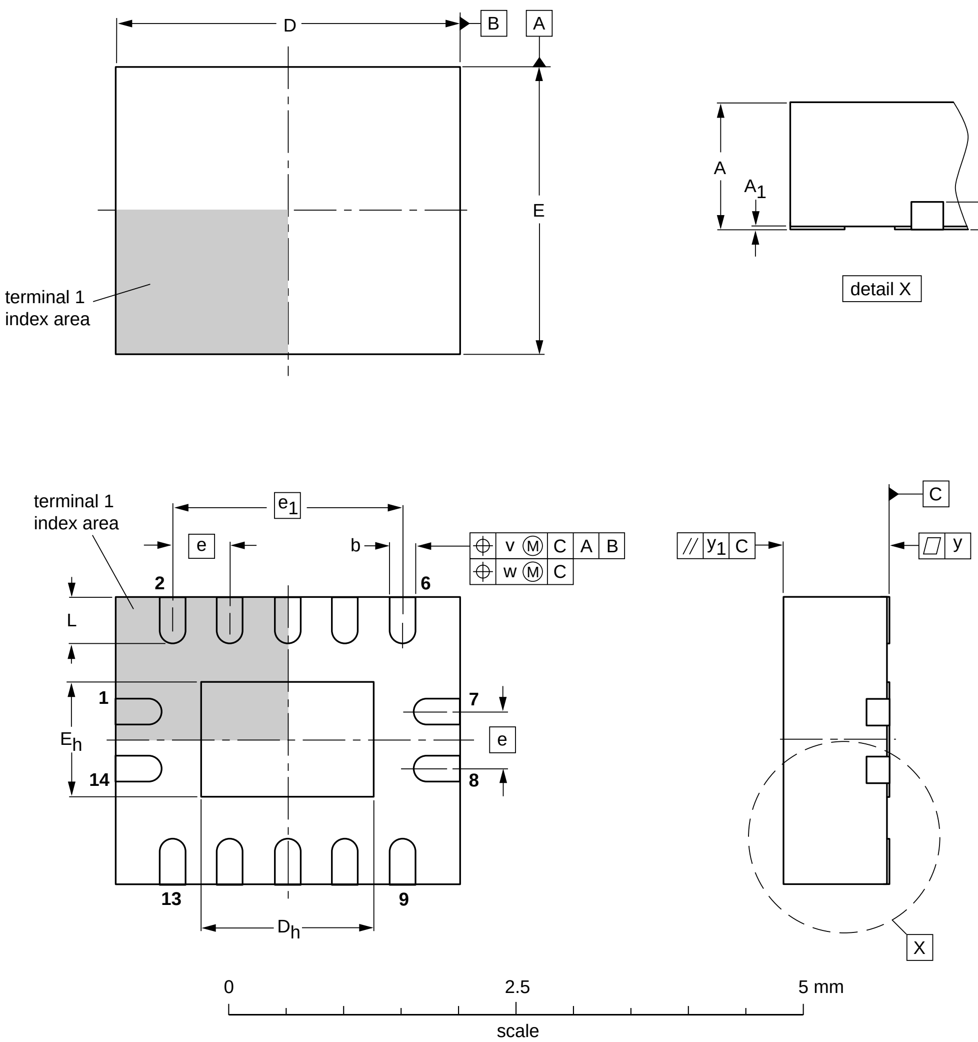
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 19. Package outline SOT762-1 (DHVQFN14)

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV14 v.6	20111212	Product data sheet	-	74LV14 v.5
Modifications:	• Legal pages updated.			
74LV14 v.5	20110105	Product data sheet	-	74LV14 v.4
74LV14 v.4	20090702	Product data sheet	-	74LV14 v.3
74LV14 v.3	20071220	Product data sheet	-	74LV14 v.2
74LV14 v.2	19980420	Product specification	-	74LV14 v.1
74LV14 v.1	19970203	Product specification	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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