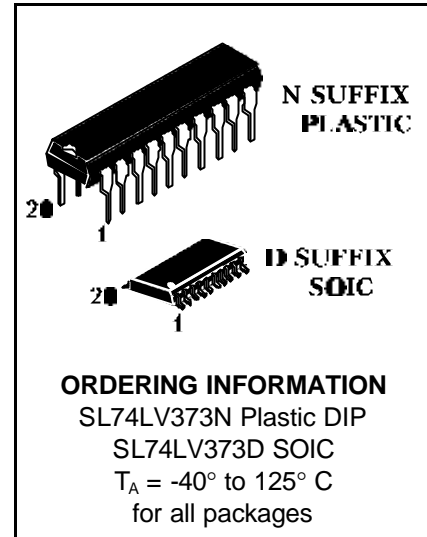


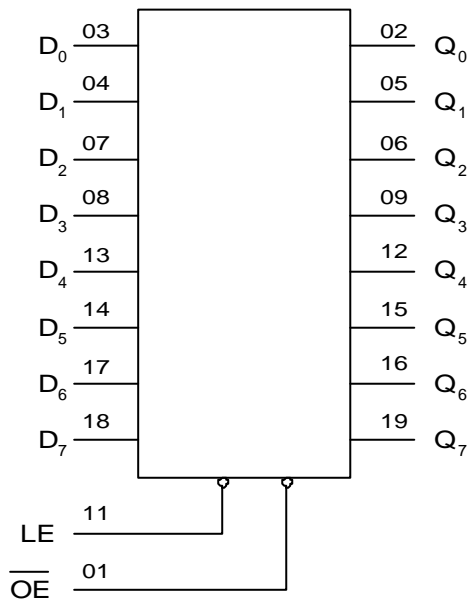
# OCTAL D-TYPE TRANSPARENT LATCH (3-State)

SL74LV373 are compatible by pinning with SL74HC373 and SL74HCT373 series. Input voltage levels are compatible with standard CMOS levels.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL ICs
- Voltage supply range: 2.0 to 3.2 V
- LOW input current: 1.0  $\mu\text{A}$ ; 0.1  $\mu\text{A}$  at  $\dot{O} = 25^\circ\text{N}$
- Input current LOW/HIGH: 8 mA
- Latch current: not less than 150 mA at  $\dot{O} = 125^\circ\text{N}$
- ESD acceptable value: not less than 2000 V as per HBM and not less than 200 V as per MM
- 

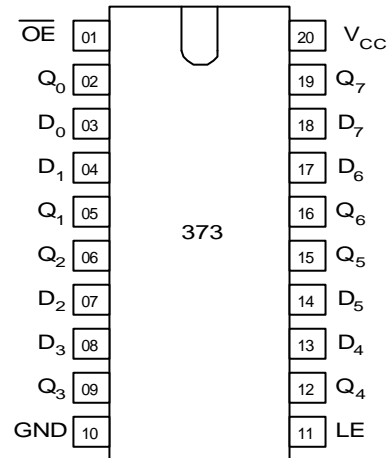


## BLOCK DIAGRAM



Pin 20 = V<sub>CC</sub>  
 Pin 10 = GND

## PIN ASSIGNMENT



## FUNCTION TABLE

Inputs			Output
$\overline{\text{OE}}$	LE	D <sub>n</sub>	Q <sub>n</sub>
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Rating	Unit
$V_{CC}$	Supply voltage	-0.5 to +5.0	V
$I_{IK}^{*1}$	Input diode current	$\pm 20$	mA
$I_{OK}^{*2}$	Output diode current	$\pm 50$	mA
$I_O^{*3}$	Output source or sink current	$\pm 35$	mA
$I_{CC}$	$V_{CC}$ current	$\pm 70$	mA
$I_{GND}$	GND current	$\pm 70$	mA
$P_D$	Power dissipation per package: Plastic DIP <sup>*4</sup> SOIC <sup>*4</sup>	750 500	mW
Tstg	Storage temperature range	-65 to +150	°C

\* In absolute maximum ratings modes functioning is not guaranteed. Upon lifting the absolute maximum ratings functioning is guaranteed at the recommended operating conditions.

\*1 Provided  $V_I < -0.5\text{ V}$  or  $V_I > V_{CC} + 0.5\text{ V}$ .

\*2 Provided  $V_O < -0.5\text{ V}$  or  $V_O > V_{CC} + 0.5\text{ V}$ .

\*3 Provided  $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ .

\*4 When operating in the temperature range of 70°C to 125°C power dissipation value decreases:

- for Plastic DIP by 12 mW/°C

- for SOIC by 8 mW/°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply voltage	1.2	3.6	V
$V_{IN}$	Input voltage	0	$V_{CC}$	V
$V_{OUT}$	Output voltage	0	$V_{CC}$	V
$T_A$	Operating ambient temperature range. For all types of packages	-40	125	°C
$t_{LH}, t_{HL}$	Input rise and fall times $V_{CC} = 1.2\text{ V}$ $V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 3.6\text{ V}$	0	1000 700 500 400	ns



## DC CHARACTERISTICS

Symbol	Parameter	Test conditions	V <sub>CC</sub> , V	Limits						Unit
				25° C		-40° C to 85° C		125° C		
				min	max	min	max	min	max	
V <sub>IH</sub>	HIGH level voltage	V <sub>O</sub> = V <sub>CC</sub> -0.1 V	1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V <sub>IL</sub>	LOW level voltage	V <sub>O</sub> = 0.1 V	1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
		3.0	2.48	-	2.34	-	2.20	-	V	
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.1	-	0.1	
		3.0	-	0.33	-	0.4	-	0.5	V	
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or 0 V	3.6	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	3-state outputs V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> or 0 V	3.6	-	±0.5	-	±5	-	±10	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 V I <sub>O</sub> = 0 μA	3.6	-	8.0	-	80	-	160	μA



**AC CHARACTERISTICS** ( $C_L=50$  pF,  $t_{LH} = t_{HL} = 6.0$  ns)

Symbol	Parameter	Test conditions	$V_{CC}$ , V	Limits						Unit
				25° C		-40° C to 85° C		125° C		
				min	max	min	max	min	max	
$t_{PHL}$ , $t_{PLH}$ from Dn to Qn	Propagation delay	Figure 1	1.2	-	150	-	190	-	220	ns
			2.0	-	38	-	48	-	58	
			3.0	-	23	-	29	-	35	
$t_{PHL}$ , $t_{PLH}$ from LE to Qn	Propagation delay	Figure 2	1.2	-	180	-	230	-	270	
			2.0	-	45	-	56	-	68	
			3.0	-	27	-	34	-	41	
$t_{PHZ}$ , $t_{PLZ}$ from OE to Qn	3-state output enable time	Figure 4	1.2	-	160	-	200	-	240	
			2.0	-	35	-	43	-	45	
			3.0	-	23	-	28	-	32	
$t_{PZH}$ , $t_{PZL}$ from OE to Qn	3-state disable time	Figure 4	1.2	-	160	-	200	-	240	
			2.0	-	40	-	50	-	60	
			3.0	-	24	-	30	-	36	
$t_{THL}$ , $t_{TLH}$	HIGH-to-LOW and LOW-to-HIGH transition time	Figures 1,2	1.2	-	75	-	100	-	120	
			2.0	-	16	-	20	-	24	
			3.0	-	10	-	13	-	15	
$t_W$	Clock pulse width HIGH or LOW	Figure 2	1.2	250	-	350	-	450	-	
			2.0	30	-	34	-	41	-	
			3.0	18	-	20	-	24	-	
$t_{SU}$	Set-up time Dn to LE	Figure 3	1.2	45	-	50	-	100	-	
			2.0	15	-	17	-	15	-	
			3.0	9	-	10	-	12	-	
$t_H$	Hold time Dn to LE	Figure 3	1.2	25	-	25	-	25	-	
			2.0	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
$C_I$	Input capacitance		3.0	-	7	-	-	-	pF	
$C_{PD}$	Power dissipation capacitance (per flip-flop)	$V_I = 0$ V or $V_{CC}$	3.0	-	80	-	-	-		

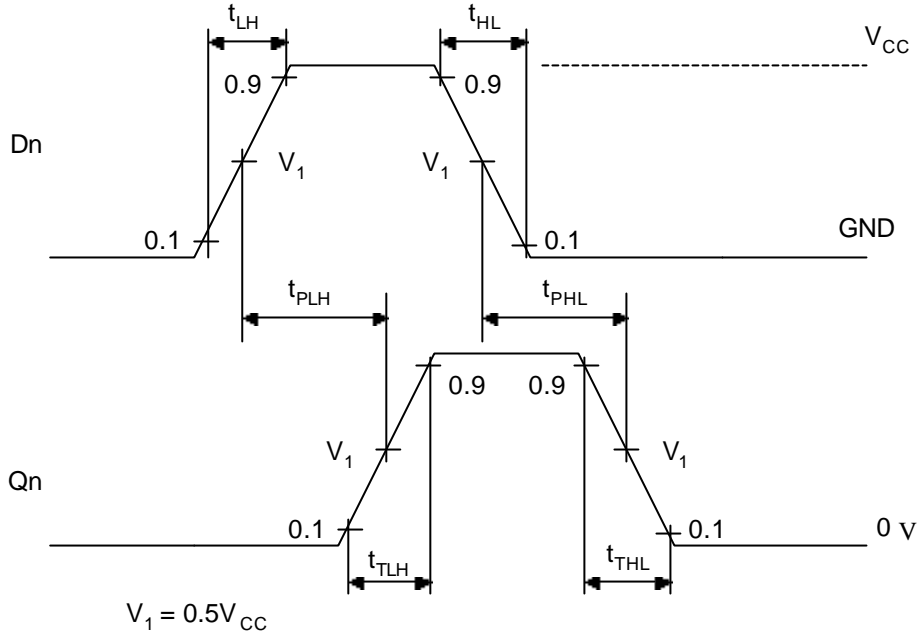


Figure 1 - Time diagram

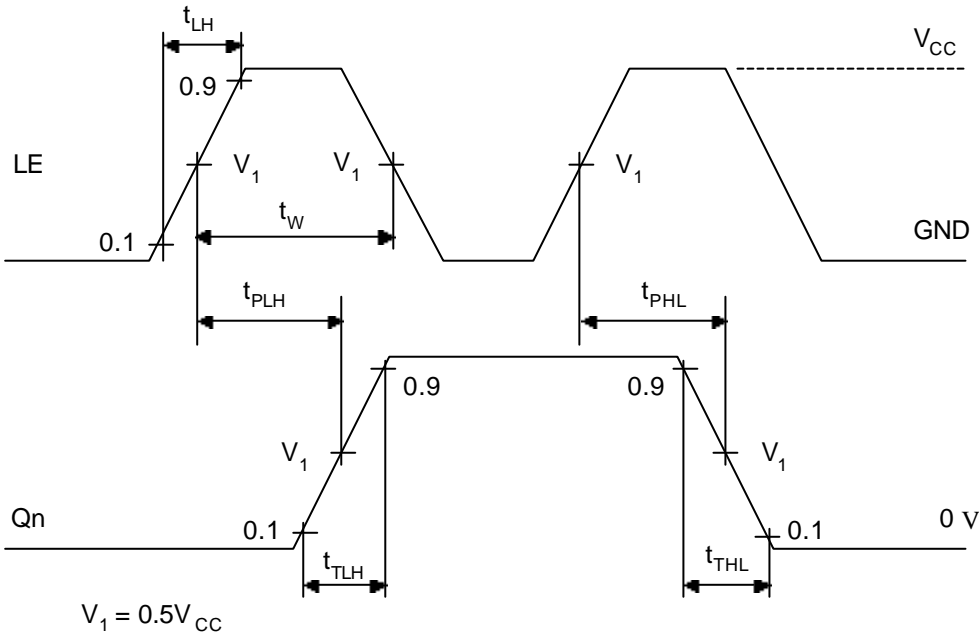


Figure 2 - Time diagram

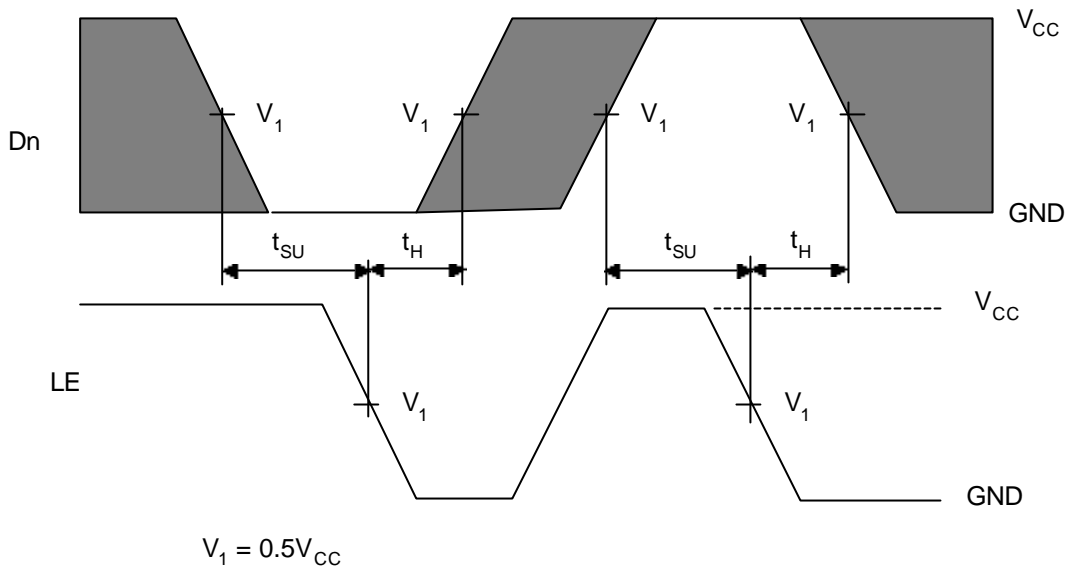


Figure 3 - Time diagram

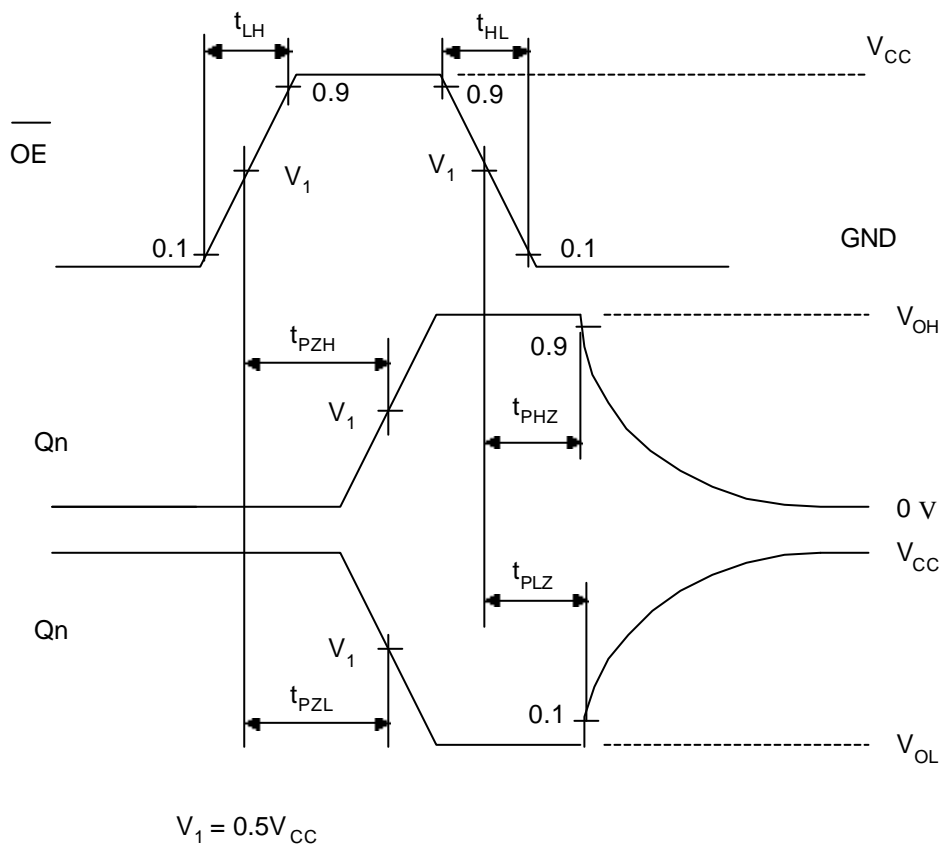
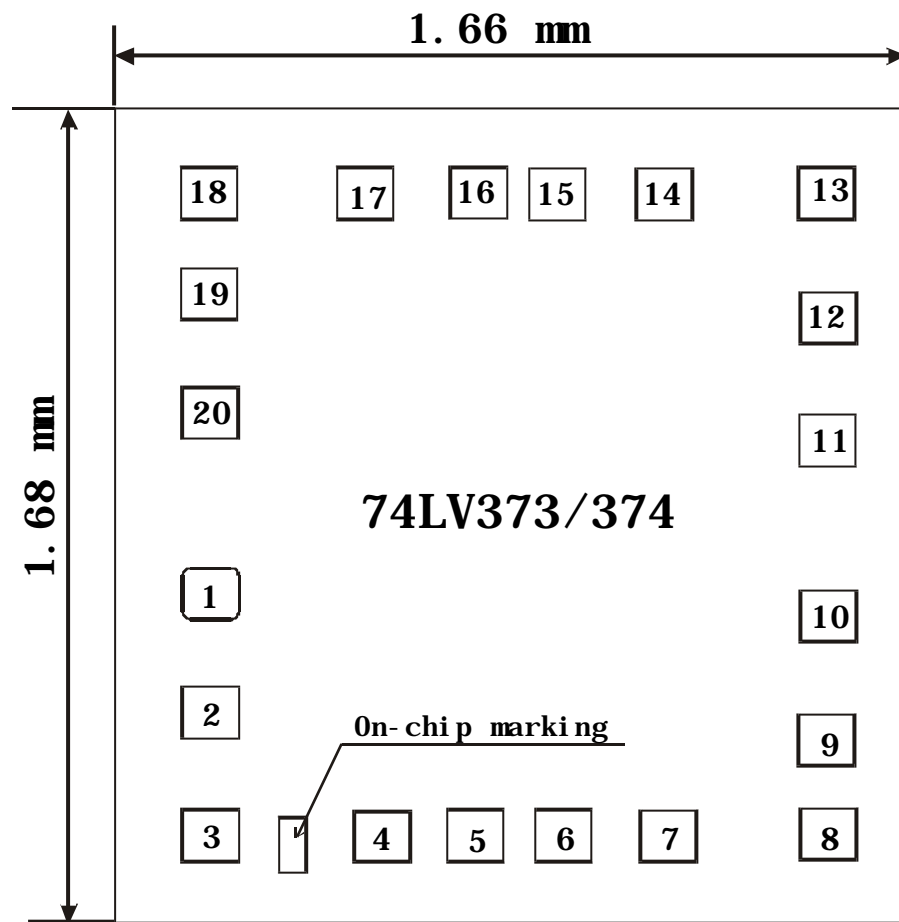


Figure 4 - Time diagram



Drawing of the chip

Pads allocation Table

Pad number	coordinates (counted from lower left corner), mm		Pad size, mm
	X	Y	
01	0.142	0.628	0.108 x 0.108
02	0.142	0.377	0.108 x 0.108
03	0.142	0.125	0.108 x 0.108
04	0.498	0.125	0.108 x 0.108
05	0.693	0.125	0.108 x 0.108
06	0.871	0.125	0.108 x 0.108
07	1.095	0.125	0.108 x 0.108
08	1.423	0.130	0.108 x 0.108
09	1.423	0.329	0.108 x 0.108
10	1.423	0.587	0.108 x 0.108
11	1.423	0.949	0.108 x 0.108
12	1.423	1.198	0.108 x 0.108
13	1.423	1.447	0.108 x 0.108
14	1.085	1.447	0.108 x 0.108
15	0.868	1.447	0.108 x 0.108
16	0.696	1.447	0.108 x 0.108
17	0.461	1.447	0.108 x 0.108
18	0.142	1.447	0.108 x 0.108

**SL74LV373**

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19	0.142	1.245	0.108 x 0.108
20	0.142	0.997	0.108 x 0.108