# 74LVC16240A

# 16-bit buffer/line driver with 5V tolerant inputs/outputs; inverting; 3-state

Rev. 5 — 25 April 2019

Product data sheet

### 1. General description

The 74LVC16240A is a 16-bit inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (10E, 20E, 30E and 40E), each controlling four of the 3-state outputs. A HIGH on noe causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

#### 2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- · CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- · Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

# 3. Ordering information

**Table 1. Ordering information** 

Type number	Package				
	Temperature range	Name	Description	Version	
74LVC16240ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1	



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# 4. Functional diagram

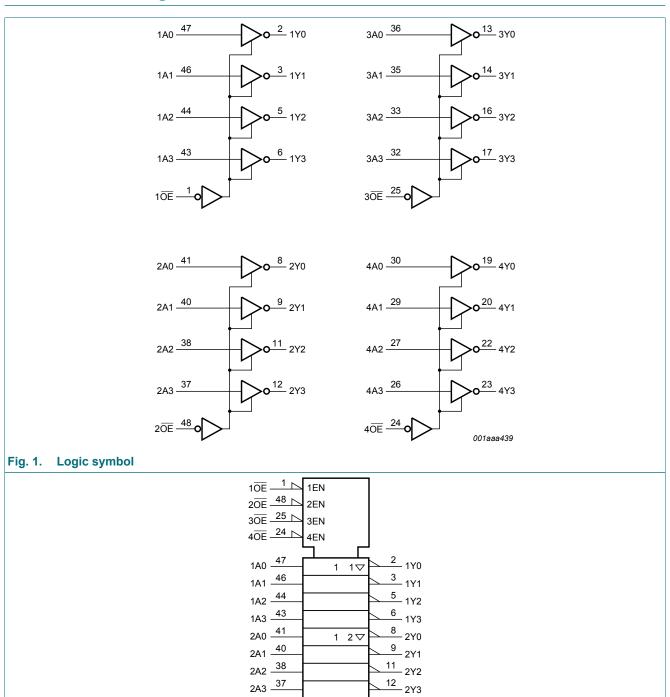


Fig. 2. IEC logic symbol

3A0 <u>36</u>

3A1 <u>35</u>

3A2 33 3A3 32

4A0 \_30

4A1 <u>29</u> 4A2 <u>27</u>

4A3 <u>26</u>

13\_3Y0

14 16 3Y2

17\_3Y3

19 4Y0

20\_\_4Y1

22 23 4Y3

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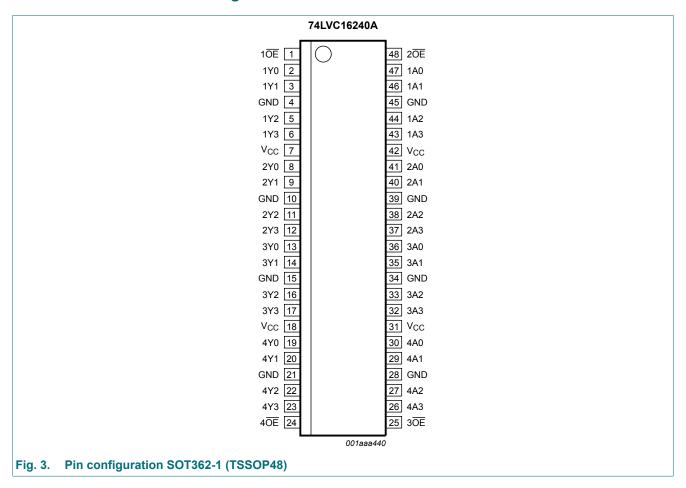
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# 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Name	Pin	Description
1 <del>OE</del> , 2 <del>OE</del> , 3 <del>OE</del> , 4 <del>OE</del>	1, 48, 25, 24	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data output
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data output
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data output
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data output
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data input
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data input
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data input
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data input

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# 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Input nOE	Output	
nŌE	nAn	nYn
L	L	Н
L	Н	L
Н	X	Z

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mΑ
VI	input voltage	[1]	-0.5	+6.5	V
I <sub>OK</sub>	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mΑ
Vo	output voltage	output HIGH or LOW state [2]	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state [2]	-0.5	+6.5	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mΑ
I <sub>CC</sub>	supply current		-	100	mΑ
I <sub>GND</sub>	ground current		-100	-	mΑ
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C to } +125  ^{\circ}\text{C}$ [3]	-	500	mW

<sup>[1]</sup> The minimum input voltage ratings may be exceeded if the input current ratings are observed.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	-	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	10	ns/V

<sup>[2]</sup> The output voltage ratings may be exceeded if the output current ratings are observed.

<sup>[3]</sup> Above 60 °C the value of Ptot derates linearly with 5.5 mW/K.

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### 9. Static characteristics

**Table 6. Static characteristics** 

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	1
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
	voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
	voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		$I_{O}$ = -12 mA; $V_{CC}$ = 2.7 V	2.2	-	-	2.05	-	V
		$I_{O}$ = -18 mA; $V_{CC}$ = 3.0 V	2.4	-	-	2.25	-	V
		$I_{O}$ = -24 mA; $V_{CC}$ = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 3.6 \text{ V}; V_{O} = 5.5 \text{ V or GND}$	-	0.1	±5	-	±20	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$	-	0.1	±10	-	±20	μΑ
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = V_{CC} \text{ or GND}; I_{O} = 0 \text{ A}$	-	0.1	20	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μΑ
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF

<sup>[1]</sup> All typical values are measured at  $V_{CC}$  = 3.3 V (unless stated otherwise) and  $T_{amb}$  = 25 °C.

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### 10. Dynamic characteristics

**Table 7. Dynamic characteristics** 

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nYn; see Fig. 4	[2]						
		V <sub>CC</sub> = 1.2 V		-	12.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		1.0	5.1	11.0	1.0	11.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.5	2.7	5.5	0.5	6.1	ns
		V <sub>CC</sub> = 2.7 V		1.0	2.7	5.2	1.0	6.5	ns
		$V_{CC}$ = 3.0 V to 3.6 V		1.0	2.3	4.2	1.0	5.5	ns
t <sub>en</sub>	enable time	nOE to nYn; see Fig. 5	[2]						
		V <sub>CC</sub> = 1.2 V		-	18.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		1.5	6.6	12.8	1.5	13.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.0	3.8	6.8	1.0	7.5	ns
		$V_{CC}$ = 2.7 V		1.5	3.5	5.8	1.5	7.5	ns
		$V_{CC}$ = 3.0 V to 3.6 V		1.0	3.0	5.0	1.0	6.5	ns
t <sub>dis</sub>	disable time	nOE to nYn; see Fig. 5	[2]						
		V <sub>CC</sub> = 1.2 V		-	11.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		2.9	4.7	9.2	2.9	9.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.0	2.6	5.0	1.0	5.6	ns
		V <sub>CC</sub> = 2.7 V		1.5	3.5	5.1	1.5	6.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V		1.5	3.2	4.9	1.5	6.5	ns
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation	per input; $V_I$ = GND to $V_{CC}$	[4]						
	capacitance	V <sub>CC</sub> = 1.65 V to 1.95 V		-	4.8	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V		-	8.3	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V		-	11.4	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

 $t_{\text{en}}$  is the same as  $t_{\text{PZL}}$  and  $t_{\text{PZH}}$ .

 $t_{\text{dis}}$  is the same as  $t_{\text{PLZ}}$  and  $t_{\text{PHZ}}.$ 

 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

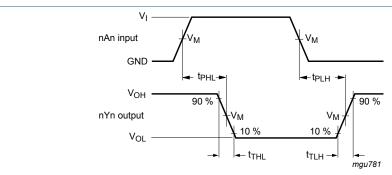
 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of the outputs

t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).  $P_D = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \Sigma (C_L \times {V_{CC}}^2 \times f_o)$  where:

#### 16-bit buffer/line driver with 5V tolerant inputs/outputs; inverting; 3-state

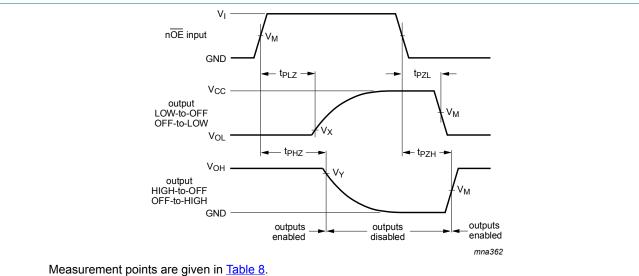
#### 10.1. Waveforms and test circuit



Measurement points are given in Table 8.

 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. The input nAn to output nYn propagation delays



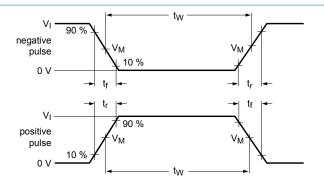
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

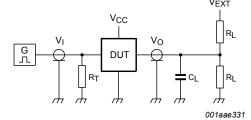
3-state enable and disable times Fig. 5.

**Table 8. Measurement points** 

Supply voltage	Input	Output		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.2 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.1 V	V <sub>OH</sub> - 0.1 V
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.1 V	V <sub>OH</sub> - 0.1 V
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.1 V	V <sub>OH</sub> - 0.1 V
2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V

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Test data is given in Table 9.

Definitions for test circuit:

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
1.2 V	V <sub>CC</sub>	≤ 2 ns	30 pF	1 kΩ	open	2 × V <sub>CC</sub>	GND
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2 ns	30 pF	1 kΩ	open	2 × V <sub>CC</sub>	GND
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND

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# 11. Package outline

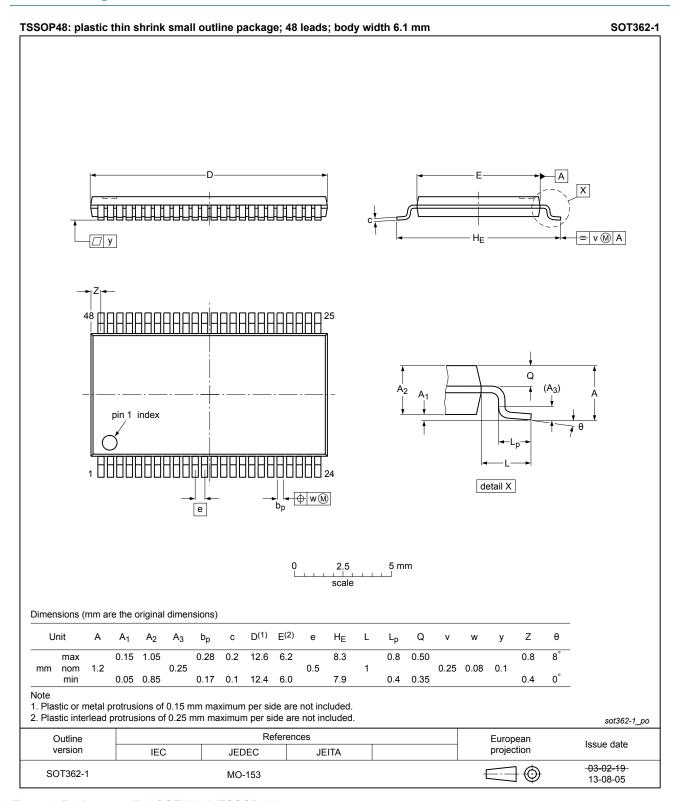


Fig. 7. Package outline SOT362-1 (TSSOP48)

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### 12. Abbreviations

#### **Table 10. Abbreviations**

Table 1417 Abbieviations				
Acronym	Description			
CDM	Charged Device Model			
CMOS	Complementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			
MM	Machine Model			
TTL	Transistor-Transistor Logic			

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74LVC16240A v.5	20190425	Product data sheet	-	74LVC16240A v.4			
Modifications:	of Nexperia. Legal texts h Type numbe Package out	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74LVC16240ADL (SOT370-1) removed.</li> <li>Package outline drawing SOT362-1 (TSSOP48) updated.</li> <li>Typo corrected in Section 5.2.</li> </ul>					
74LVC16240A v.4	20111103	Product data sheet	-	74LVC16240A v.3			
Modifications:	guidelines of • Legal texts h	<ul> <li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges.</li> </ul>					
74LVC16240A v.3	20040305	Product specification	-	74LVC16240A v.2			
74LVC16240A v.2	19970729	Product specification	-	74LVC16240A v.1			
74LVC16240A v.1	19951226	Product specification	-	-			

#### 16-bit buffer/line driver with 5V tolerant inputs/outputs; inverting; 3-state

### 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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#### 16-bit buffer/line driver with 5V tolerant inputs/outputs; inverting; 3-state

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