

DATA SHEET

74LVC1G17

Single Schmitt-trigger buffer

Product specification
Supersedes data of 2004 Oct 18

2004 Nov 30

Single Schmitt-trigger buffer

74LVC1G17

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V).
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Unlimited rise and fall times
- Input accepts voltages up to 5 V
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

DESCRIPTION

The 74LVC1G17 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G17 provides a buffer function with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A to Y	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k Ω	4.1	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω	2.8	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω	3.0	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.2	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	16.6	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

Single Schmitt-trigger buffer

74LVC1G17

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
A	Y
L	L
H	H

Note

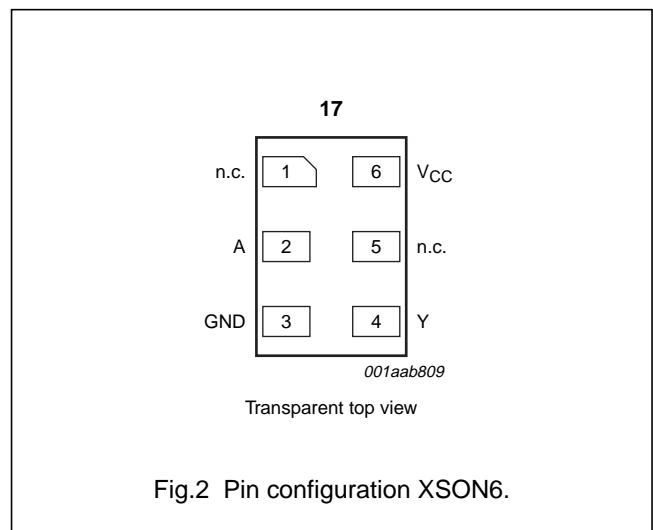
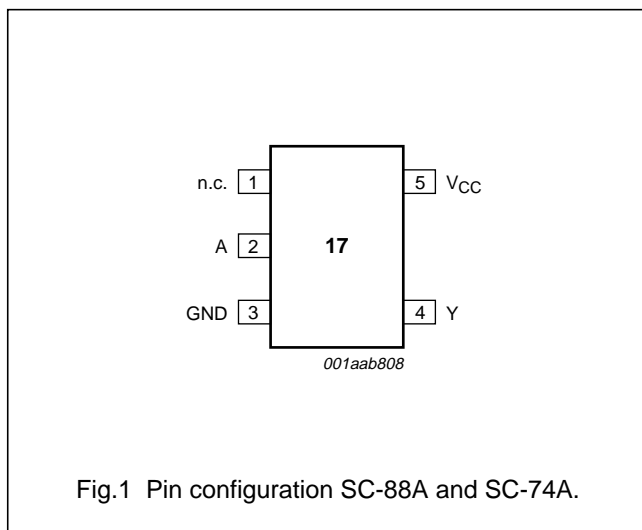
- 1. H = HIGH voltage level;
L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G17GW	-40 °C to +125 °C	5	SC-88A	plastic	SOT353	VJ
74LVC1G17GV	-40 °C to +125 °C	5	SC-74A	plastic	SOT753	V17
74LVC1G17GM	-40 °C to +125 °C	6	XSON6	plastic	SOT886	VJ

PINNING

PIN SC-88A; SC-74A	PIN XSON6	SYMBOL	DESCRIPTION
1	1	n.c.	not connected
2	2	A	data input A
3	3	GND	ground (0 V)
4	4	Y	data output Y
-	5	n.c.	not connected
5	6	V _{CC}	supply voltage



Single Schmitt-trigger buffer

74LVC1G17

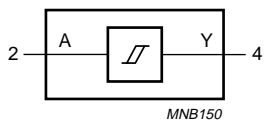


Fig.3 Logic symbol.

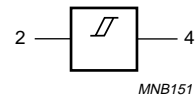


Fig.4 IEEE/IEC logic symbol.

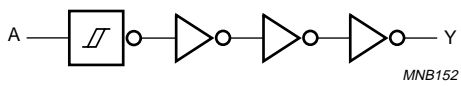


Fig.5 Logic diagram.

Single Schmitt-trigger buffer

74LVC1G17

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
T_{amb}	operating ambient temperature		-40	+125	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	active mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

Single Schmitt-trigger buffer

74LVC1G17

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
V _{OL}	LOW-level output voltage	V _I = V _{CC} or GND					
		I _O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I _O = 4 mA	1.65	–	–	0.45	V
		I _O = 8 mA	2.3	–	–	0.3	V
		I _O = 12 mA	2.7	–	–	0.4	V
		I _O = 24 mA	3.0	–	–	0.55	V
V _{OH}	HIGH-level output voltage	V _I = V _{CC} or GND					
		I _O = -100 μA	1.65 to 5.5	V _{CC} - 0.1	–	–	V
		I _O = -4 mA	1.65	1.2	–	–	V
		I _O = -8 mA	2.3	1.9	–	–	V
		I _O = -12 mA	2.7	2.2	–	–	V
		I _O = -24 mA	3.0	2.3	–	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	–	±0.1	±5	μA
		I _O = 0 A	0	–	±0.1	±10	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	±0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	–	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0 A	2.3 to 5.5	–	5	500	μA

Single Schmitt-trigger buffer

74LVC1G17

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
V _{OL}	LOW-level output voltage	V _I = V _{CC} or GND					
		I _O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I _O = 4 mA	1.65	–	–	0.7	V
		I _O = 8 mA	2.3	–	–	0.45	V
		I _O = 12 mA	2.7	–	–	0.6	V
		I _O = 24 mA	3.0	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{CC} or GND					
		I _O = -100 μA	1.65 to 5.5	V _{CC} - 0.1	–	–	V
		I _O = -4 mA	1.65	0.95	–	–	V
		I _O = -8 mA	2.3	1.7	–	–	V
		I _O = -12 mA	2.7	1.9	–	–	V
		I _O = -24 mA	3.0	2.0	–	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	–	–	±100	μA
		I _O = 0 A	0	–	–	±200	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	–	±200	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	–	–	200	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0 A	2.3 to 5.5	–	–	5000	μA

Note

1. All typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

Single Schmitt-trigger buffer

74LVC1G17

TRANSFER CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
V _{T+}	positive-going threshold voltage	see Figs 6 and 7	1.8	0.82	1.0	1.14	V
			2.3	1.03	1.2	1.40	V
			3.0	1.29	1.5	1.71	V
			4.5	1.84	2.1	2.36	V
			5.5	2.19	2.5	2.79	V
V _{T-}	negative-going threshold voltage	see Figs 6 and 7	1.8	0.46	0.6	0.75	V
			2.3	0.65	0.8	0.96	V
			3.0	0.88	1.0	1.24	V
			4.5	1.32	1.5	1.84	V
			5.5	1.58	1.8	2.24	V
V _H	hysteresis voltage (V _{T+} - V _{T-})	see Figs 6 and 7	1.8	0.26	0.4	0.51	V
			2.3	0.28	0.4	0.57	V
			3.0	0.31	0.5	0.64	V
			4.5	0.40	0.6	0.77	V
			5.5	0.47	0.6	0.88	V
T_{amb} = -40 °C to +125 °C							
V _{T+}	positive-going threshold voltage	see Figs 6 and 7	1.8	0.79	–	1.14	V
			2.3	1.00	–	1.40	V
			3.0	1.26	–	1.71	V
			4.5	1.81	–	2.36	V
			5.5	2.16	–	2.79	V
V _{T-}	negative-going threshold voltage	see Figs 6 and 7	1.8	0.46	–	0.78	V
			2.3	0.65	–	0.99	V
			3.0	0.88	–	1.27	V
			4.5	1.32	–	1.87	V
			5.5	1.58	–	2.27	V
V _H	hysteresis voltage (V _{T+} - V _{T-})	see Figs 6 and 7	1.8	0.19	–	0.51	V
			2.3	0.22	–	0.57	V
			3.0	0.25	–	0.64	V
			4.5	0.34	–	0.77	V
			5.5	0.41	–	0.88	V

Note1. All typical values are measured at T_{amb} = 25 °C.

Single Schmitt-trigger buffer

74LVC1G17

TRANSFER CHARACTERISTIC WAVEFORMS

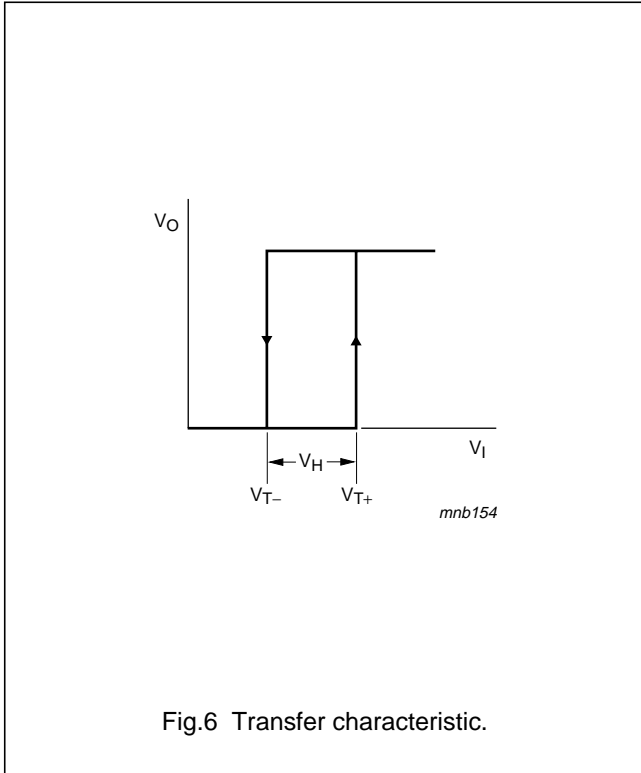


Fig.6 Transfer characteristic.

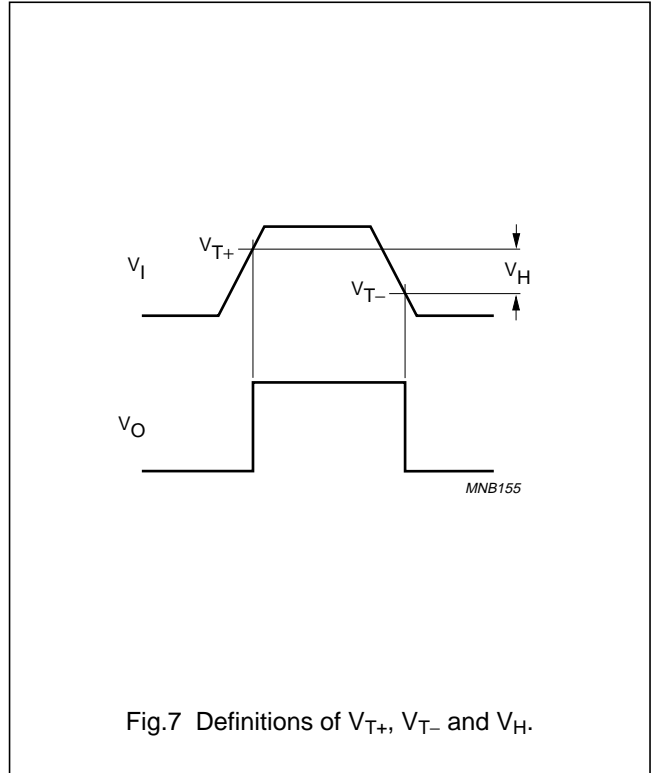
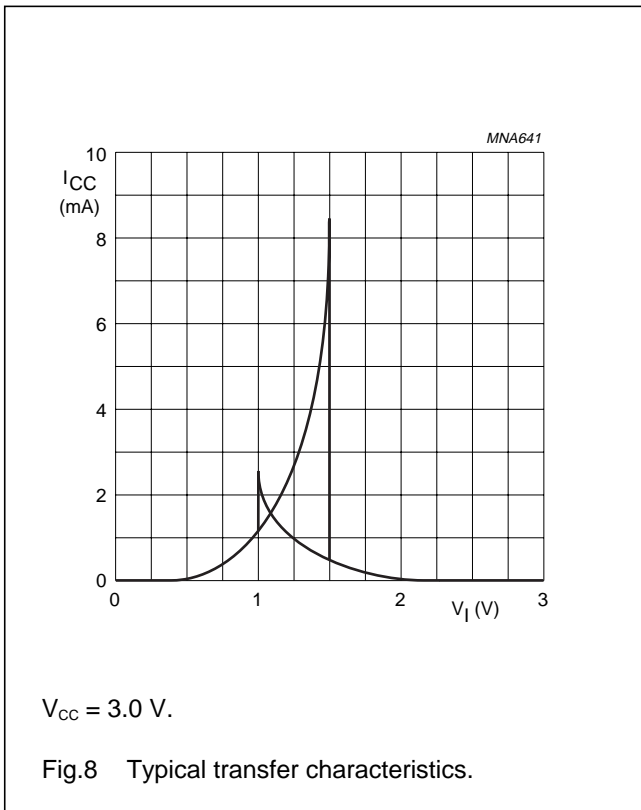


Fig.7 Definitions of V_{T+} , V_{T-} and V_H .



$V_{CC} = 3.0$ V.

Fig.8 Typical transfer characteristics.

Single Schmitt-trigger buffer

74LVC1G17

AC CHARACTERISTICS

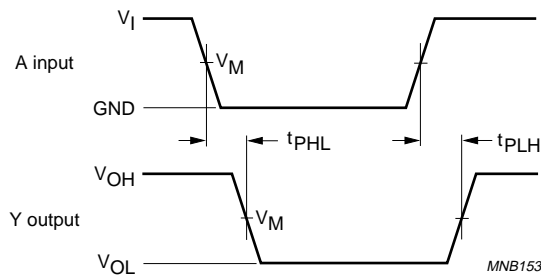
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay A to Y	see Figs 9 and 10	1.65 to 1.95	1.0	4.1	11.0	ns
			2.3 to 2.7	0.7	2.8	6.5	ns
			2.7	0.7	3.2	6.5	ns
			3.0 to 3.6	0.7	3.0	5.5	ns
			4.5 to 5.5	0.7	2.2	5.0	ns
T_{amb} = -40 °C to +125 °C							
t _{PHL} /t _{PLH}	propagation delay A to Y	see Figs 9 and 10	1.65 to 1.95	1.0	–	14.0	ns
			2.3 to 2.7	0.7	–	8.5	ns
			2.7	0.7	–	8.5	ns
			3.0 to 3.6	0.7	–	7.0	ns
			4.5 to 5.5	0.7	–	6.5	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



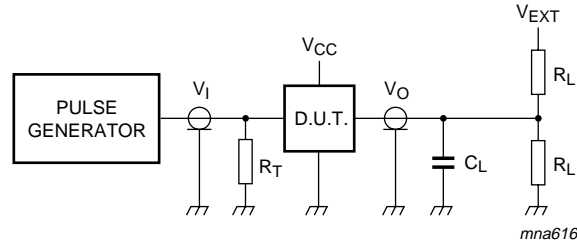
V _{CC}	V _M	INPUT	
		V _I	t _r = t _f
1.65 V to 1.95 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V _{CC}	V _{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.9 Input A to output Y propagation delay times.

Single Schmitt-trigger buffer

74LVC1G17



V _{CC}	V _I	C _L	R _L	V _{EXT}		
				t _{PLH} /t _{PHL}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.65 V to 1.95 V	V _{CC}	30 pF	1 kΩ	open	GND	2 × V _{CC}
2.3 V to 2.7 V	V _{CC}	30 pF	500 Ω	open	GND	2 × V _{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V _{CC}	50 pF	500 Ω	open	GND	2 × V _{CC}

Definitions for test circuit:

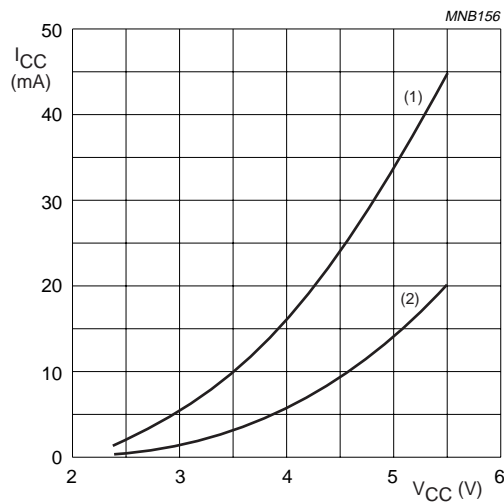
R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

APPLICATION INFORMATION



- (1) Positive-going edge. Linear change of V_I between 0.8 V to 2.0 V.
- (2) Negative-going edge.

Fig.11 Average supply current as a function of supply voltage.

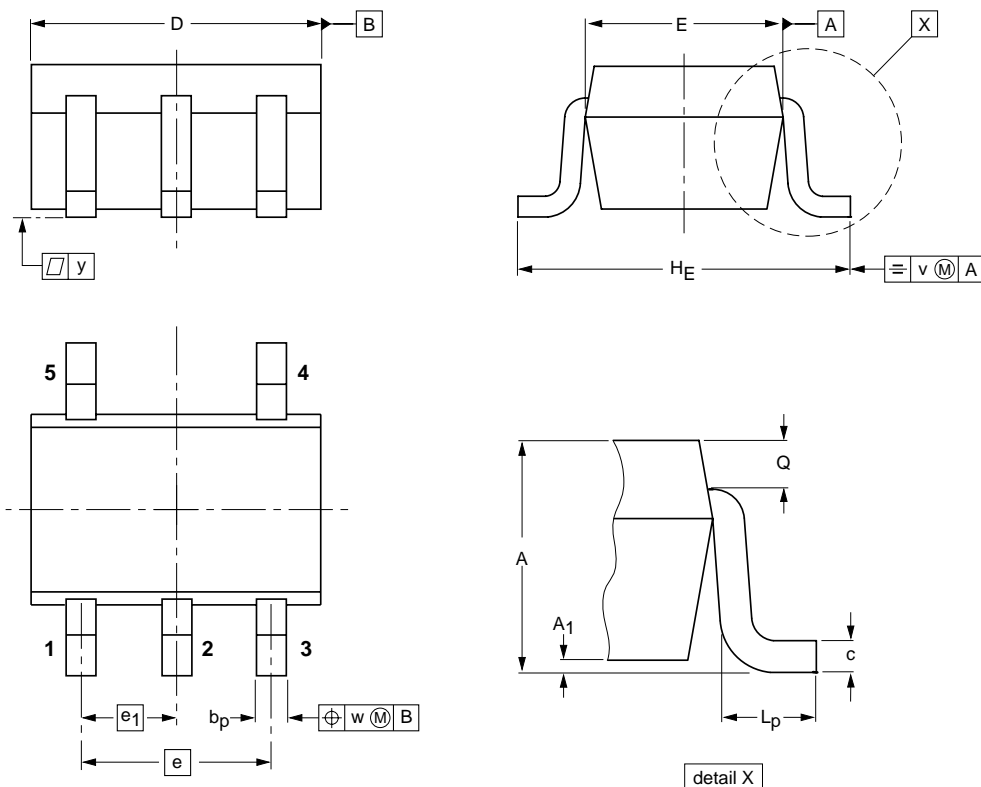
Single Schmitt-trigger buffer

74LVC1G17

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E ⁽²⁾	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.3 0.2	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

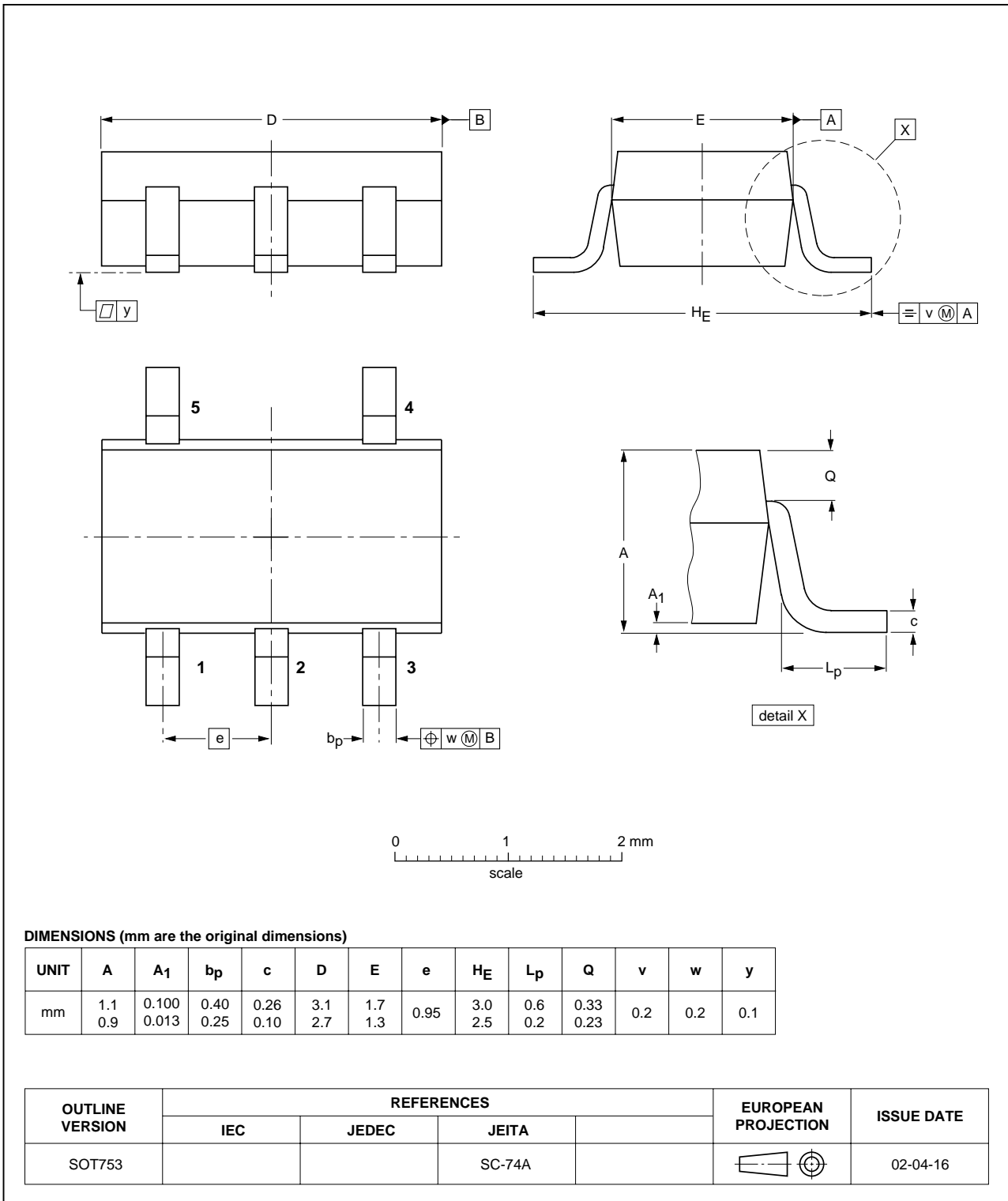
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353			SC-88A			-97-02-28 04-11-16

Single Schmitt-trigger buffer

74LVC1G17

Plastic surface mounted package; 5 leads

SOT753

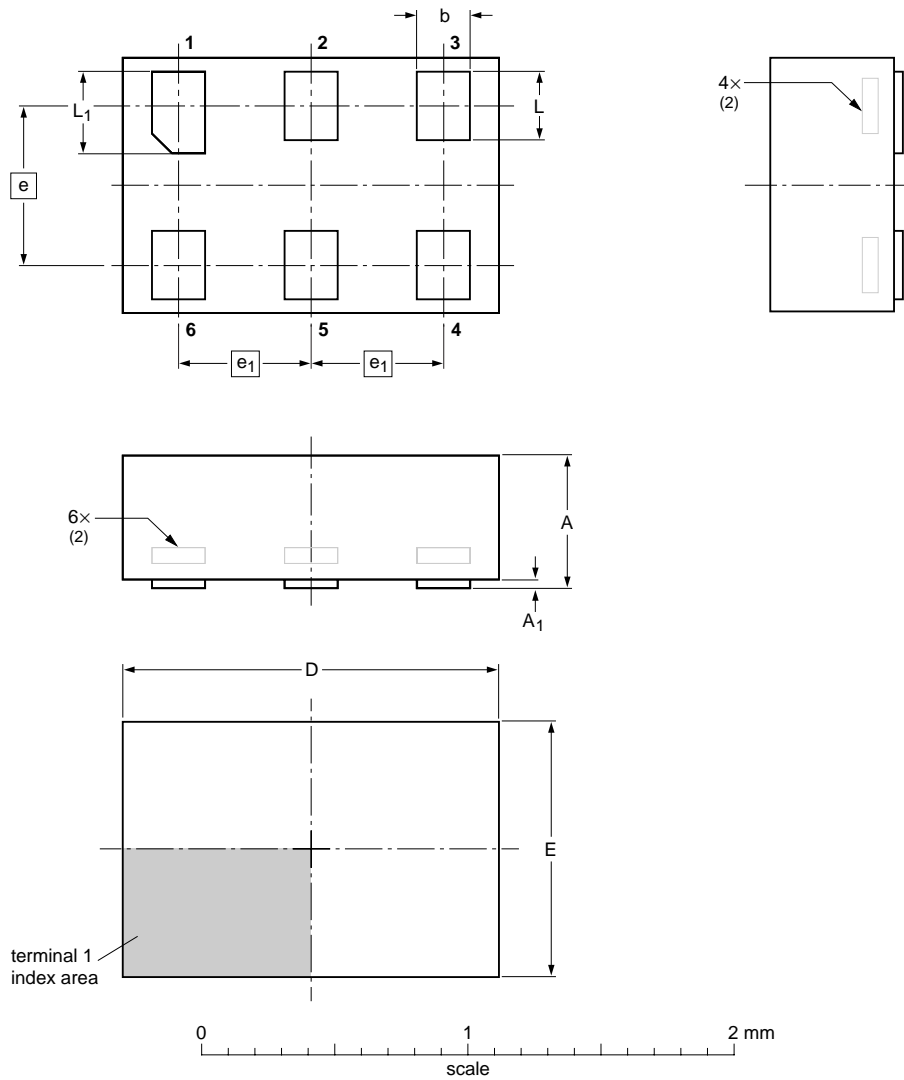


Single Schmitt-trigger buffer

74LVC1G17

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT886		MO-252			04-07-15 04-07-22

Single Schmitt-trigger buffer

74LVC1G17

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2004

SCA76

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R20/04/pp16

Date of release: 2004 Nov 30

Document order number: 9397 750 14375

Let's make things better.

**Philips
Semiconductors**



PHILIPS