74LVC1G57

Low-power configurable multiple function gate

Rev. 01 — 6 September 2004 Product data sheet

1. General description

The 74LVC1G57 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G57 provides configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer. All inputs can be connected to V_{CC} or GND.

All inputs (A, B and C) have Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay input A, B and C to output Y	C_L = 30 pF; R_L = 1 kΩ; V_{CC} = 1.8 V		-	6.0	-	ns
		C_L = 30 pF; R_L = 500 Ω; V_{CC} = 2.5 V		-	3.5	-	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 2.7 V		-	4.2	-	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3.3 V		-	3.8	-	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 5.0 V;		-	3.0	-	ns
C_I	input capacitance			-	2.5	-	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V	[1] [2]	-	22	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G57GW	–40 °C to +125 °C	-	plastic surface mounted package; 6 leads	SOT363
74LVC1G57GV	–40 °C to +125 °C	-	plastic surface mounted package; 6 leads	SOT457
74LVC1G57GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

5. Marking

Table 3: Marking

Type number	Marking code
74LVC1G57GW	YC
74LVC1G57GV	V57
74LVC1G57GM	YC

6. Functional diagram

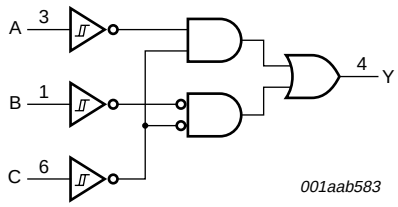


Fig 1. Logic symbol.

7. Pinning information

7.1 Pinning

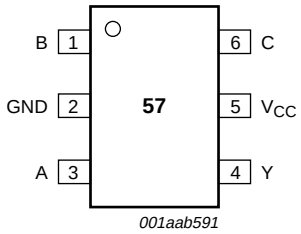
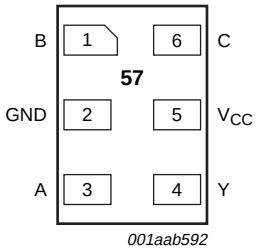


Fig 2. Pin configuration SOT363 and SOT457.



Transparent top view

Fig 3. Pin configuration SOT886.

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
B	1	data input B
GND	2	ground (0 V)
A	3	data input A
Y	4	data output Y
V_{CC}	5	supply voltage
C	6	data input C

8. Functional description

8.1 Function table

Table 5: Function table [1]

Input			Output
C	**B**	**A**	**Y**
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

[1] H = HIGH voltage level;
L = LOW voltage level.

8.2 Logic configurations

Table 6: Function selection table

Logic function	Figure
2-input AND	see Figure 4
2-input AND with both inputs inverted	see Figure 7
2-input NAND with inverted input	see Figure 5 and 6
2-input OR with inverted input	see Figure 5 and 6
2-input NOR	see Figure 7
2-input NOR with both inputs inverted	see Figure 4
2-input XNOR	see Figure 8
Inverter	see Figure 9
Buffer	see Figure 10

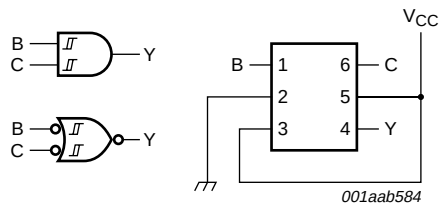


Fig 4. 2-input AND gate or 2-input NOR gate with both inputs inverted.

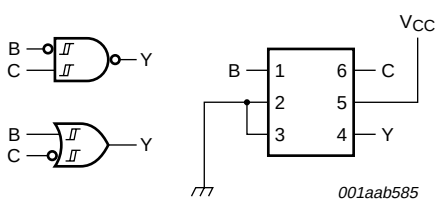


Fig 5. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input.

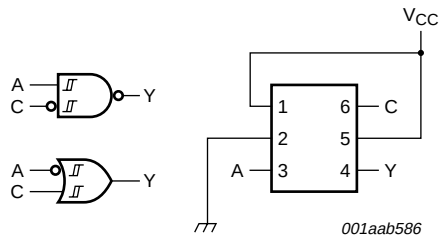


Fig 6. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input.

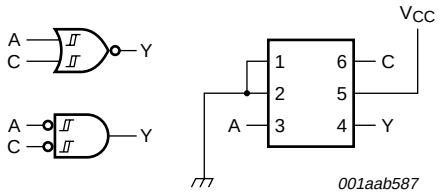


Fig 7. 2-input NOR gate or 2-input AND gate with both inputs inverted.

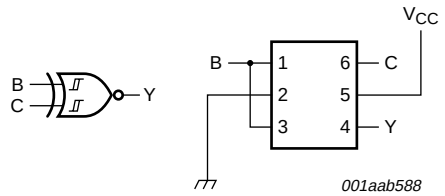


Fig 8. 2-input XNOR gate.

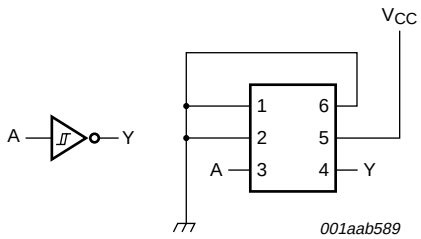


Fig 9. Inverter.

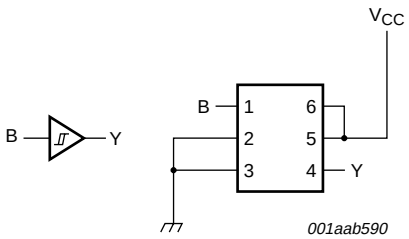


Fig 10. Buffer.

9. Limiting values

Table 7: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	active mode	[1] [2]	–0.5	+6.5	V
		Power-down mode	[1] [2]	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA

Table 7: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 8: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	-	5.5	V
T_{amb}	operating ambient temperature		–40	-	+125	°C

11. Static characteristics

Table 9: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{OL}	LOW-level output voltage	V_I = V_{CC} or GND				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{CC} or GND				
		I_O = –100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.8	-	-	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V	-	±0.1	±5	µA

Table 9: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	µA
C_I	input capacitance		-	2.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{OL}	LOW-level output voltage	$V_I = V_{CC}$ or GND				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.7	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{CC}$ or GND				
		I_O = –100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.4	-	-	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V	-	-	±100	µA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±200	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	200	µA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	µA

[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

12. Dynamic characteristics

Table 10: Dynamic characteristics

GND = 0 V.

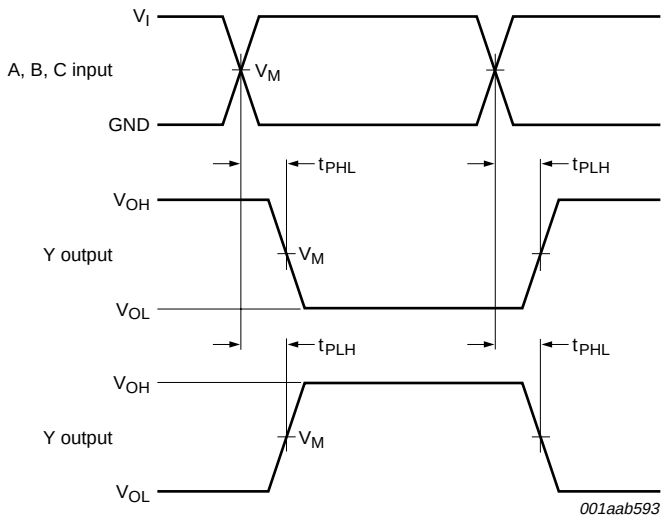
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay A, B, C to Y	see Figure 11 and 12					
		V_{CC} = 1.65 V to 1.95 V		1.0	6.0	14.4	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	3.5	8.3	ns
		V_{CC} = 2.7 V		0.5	4.2	8.5	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	3.8	6.3	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	3.0	5.1	ns
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V	[2] [3]	-	22	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay A, B, C to Y	see Figure 11 and 12					
		V_{CC} = 1.65 V to 1.95 V		1.0	-	18	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	-	10.4	ns
		V_{CC} = 2.7 V		0.5	-	10.6	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	-	7.9	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	6.4	ns

[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[3] The condition is V_I = GND to V_{CC}.

13. Waveforms



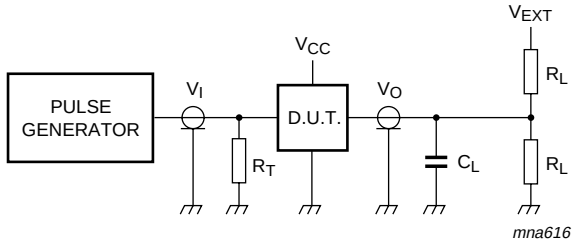
Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 11. Input A, B and C to output Y propagation delay times.

Table 11: Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	$0.5 \times V_{CC}$
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	$0.5 \times V_{CC}$



Measurement points are given in Table 12.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = Test voltage for switching times.

Fig 12. Load circuitry for switching times.

Table 12: Measurement points

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

14. Transfer characteristics

Table 13: Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{T+}	positive-going threshold voltage	see Figure 13, 14, 15 and 16				
		V_{CC} = 1.8 V	0.70	1.02	1.20	V
		V_{CC} = 2.3 V	1.11	1.42	1.60	V
		V_{CC} = 3.0 V	1.50	1.79	2.00	V
		V_{CC} = 4.5 V	2.16	2.52	2.74	V
		V_{CC} = 5.5 V	2.61	2.99	3.33	V
V_{T-}	negative-going threshold voltage	see Figure 13, 14, 15 and 16				
		V_{CC} = 1.8 V	0.30	0.53	0.72	V
		V_{CC} = 2.3 V	0.58	0.77	1.00	V
		V_{CC} = 3.0 V	0.80	1.04	1.30	V
		V_{CC} = 4.5 V	1.21	1.55	1.90	V
		V_{CC} = 5.5 V	1.45	1.86	2.29	V

Table 13: Transfer characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_H	hysteresis voltage ($V_{T+} - V_{T-}$)	see Figure 13, 14, 15 and 16				
		V_{CC} = 1.8 V	0.30	0.48	0.62	V
		V_{CC} = 2.3 V	0.40	0.64	0.80	V
		V_{CC} = 3.0 V	0.50	0.75	1.00	V
		V_{CC} = 4.5 V	0.71	0.97	1.20	V
		V_{CC} = 5.5 V	0.71	1.13	1.40	V
T_{amb} = −40 °C to +125 °C						
V_{T+}	positive-going threshold voltage	see Figure 13, 14, 15 and 16				
		V_{CC} = 1.8 V	0.67	-	1.20	V
		V_{CC} = 2.3 V	1.08	-	1.60	V
		V_{CC} = 3.0 V	1.47	-	2.00	V
		V_{CC} = 4.5 V	2.13	-	2.74	V
		V_{CC} = 5.5 V	2.58	-	3.33	V
V_{T-}	negative-going threshold voltage	see Figure 13, 14, 15 and 16				
		V_{CC} = 1.8 V	0.30	-	0.75	V
		V_{CC} = 2.3 V	0.58	-	1.03	V
		V_{CC} = 3.0 V	0.80	-	1.33	V
		V_{CC} = 4.5 V	1.21	-	1.93	V
		V_{CC} = 5.5 V	1.45	-	2.32	V
V_H	hysteresis voltage ($V_{T+} - V_{T-}$)	see Figure 13, 14, 15 and 16				
		V_{CC} = 1.8 V	0.23	-	0.62	V
		V_{CC} = 2.3 V	0.34	-	0.80	V
		V_{CC} = 3.0 V	0.44	-	1.00	V
		V_{CC} = 4.5 V	0.65	-	1.20	V
		V_{CC} = 5.5 V	0.65	-	1.40	V

[1] Typical values are measured at T_{amb} = 25 °C.

15. Waveforms transfer characteristics

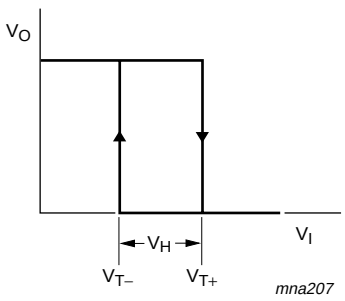
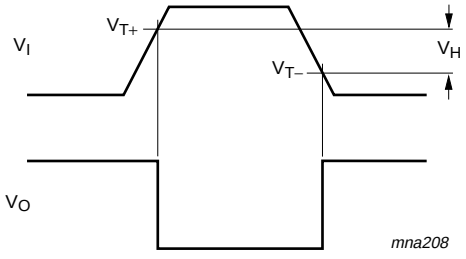


Fig 13. Transfer characteristic.



V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig 14. Definition of V_{T+}, V_{T-} and V_H.

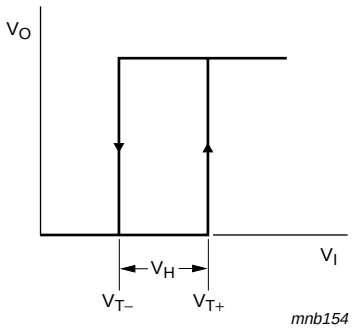
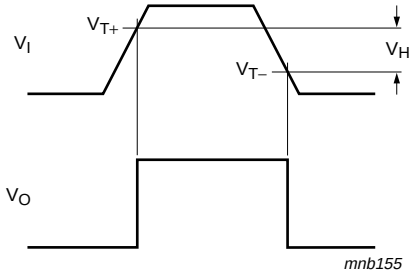


Fig 15. Transfer characteristic.



V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig 16. Definition of V_{T+}, V_{T-} and V_H.

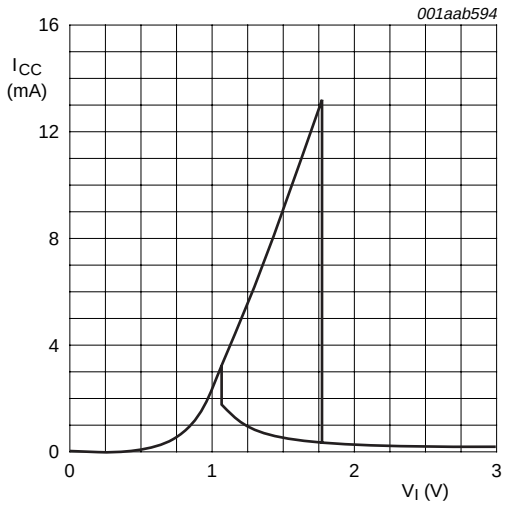
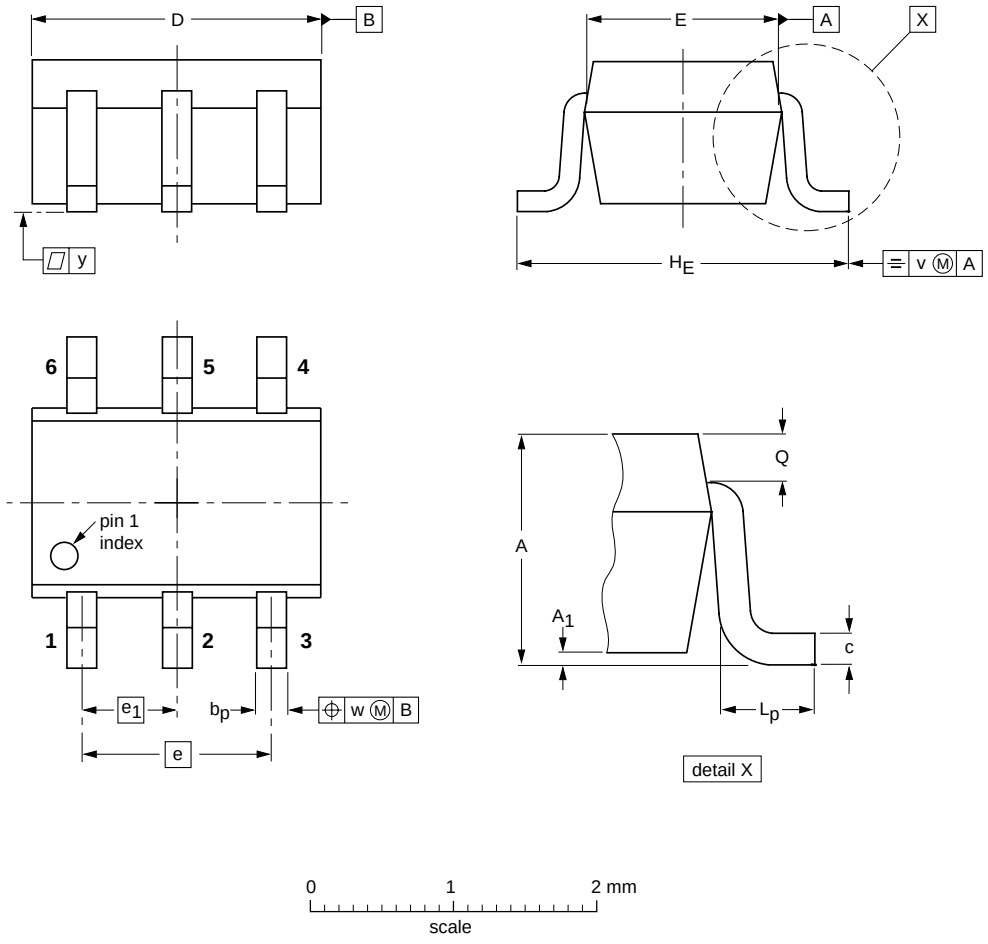


Fig 17. Typical 74LVC1G57 transfer characteristic; V_{CC} = 3.0 V.

16. Package outline

Plastic surface mounted package; 6 leads **SOT363**



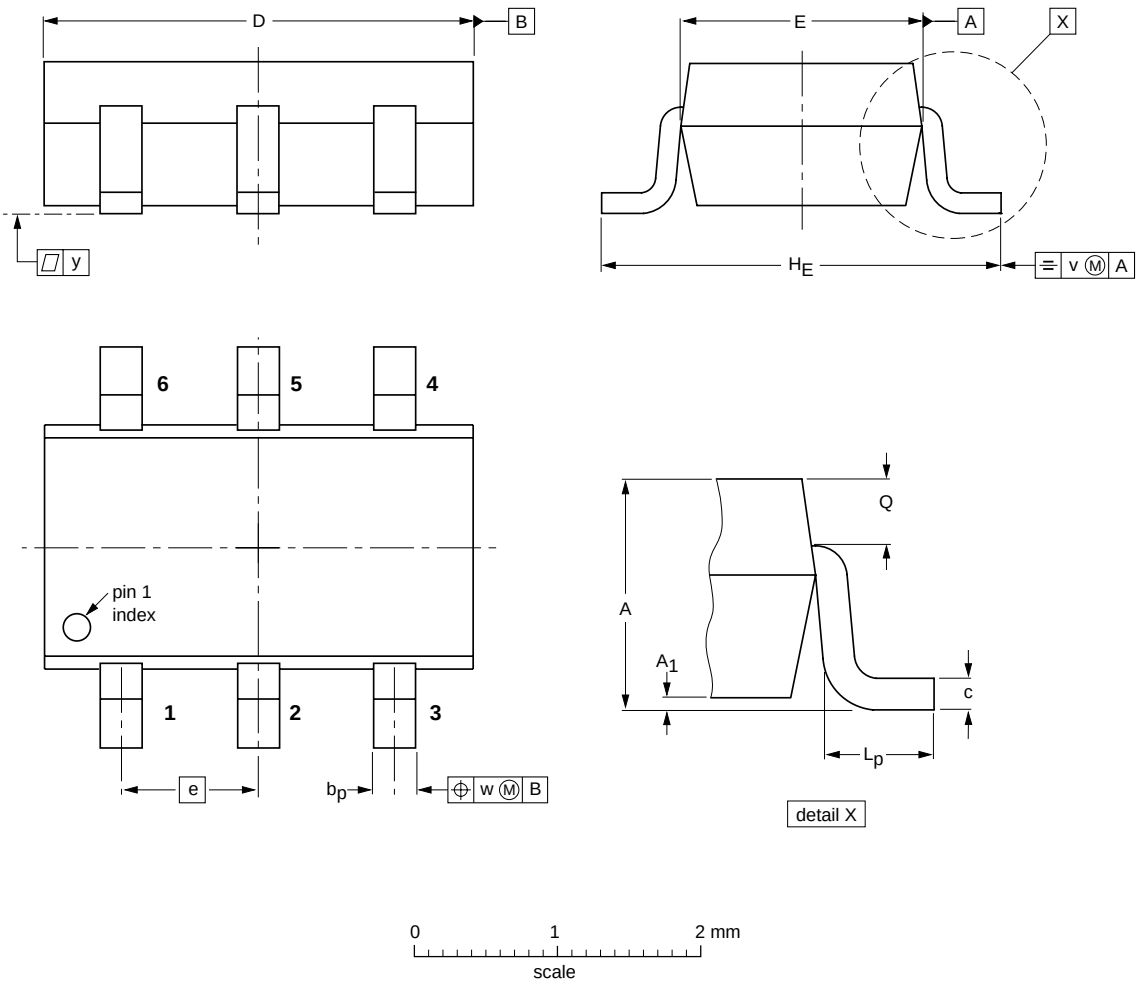
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Fig 18. Package outline SOT363.

Plastic surface mounted package; 6 leads **SOT457**



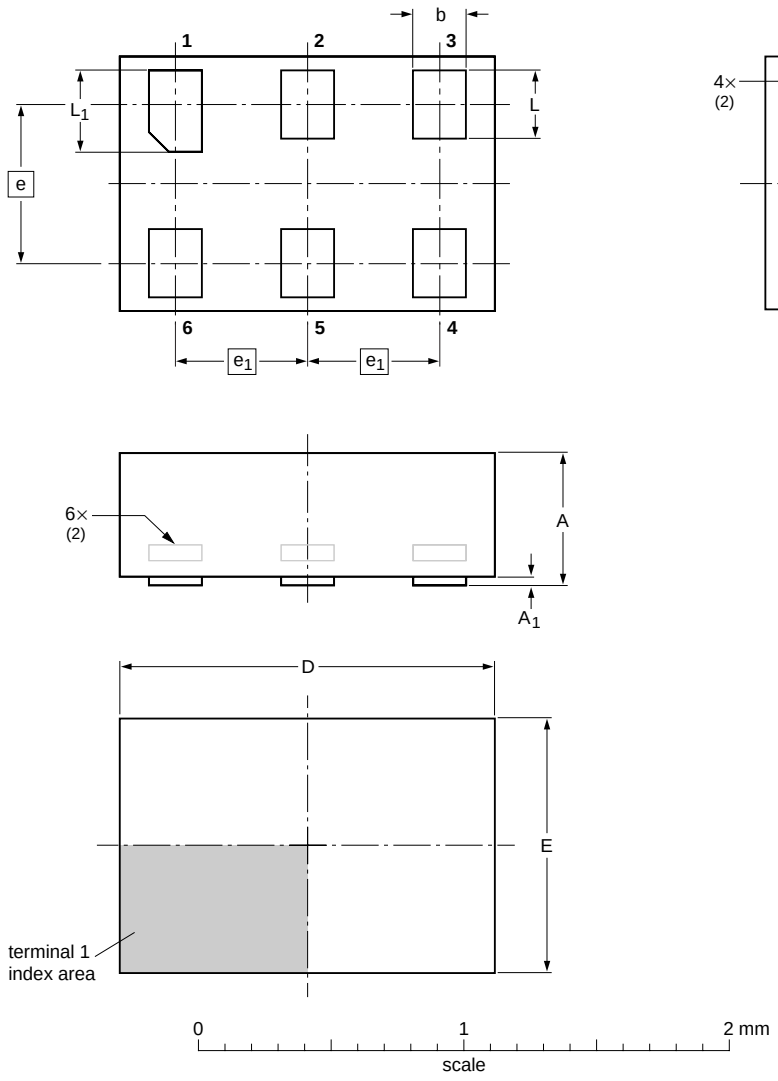
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			~~97-02-28~~ 01-05-04

Fig 19. Package outline SOT457.

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 20. Package outline SOT886 (XSON6).

17. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC1G57_1	20040906	Product data sheet	-	9397 750 13722	-

18. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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22. Contents

Date of release: 6 September 2004
Document number: 9397 750 13722

Published in The Netherlands