DATA SHEET

74LVC1G66
Bilateral switch

Product specification
2001 Oct 30
File under Integrated Circuits, IC24

Philips
Semiconductors

PHILIPS

Bilateral switch 74LVC1G66

FEATURES

- Very low ON resistance:
  - 10 Ω (typical) at V_{CC} = 2.7 V
  - 8 Ω (typical) at V_{CC} = 3.3 V
  - 6 Ω (typical) at V_{CC} = 5 V.
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- High noise immunity
- CMOS low power consumption
- Latch up performance exceeds 250 mA
- SOT353 package
- Direct interface TTL-levels.

DESCRIPTION

The 74LVC1G66 is a high-speed Si-gate CMOS device.

The 74LVC1G66 provides an analog switch. The switch has two input/output pins (Y and Z) and an active HIGH enable input pin (E). When pin E is LOW, the analog switch is turned off.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3 V	2.6	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 5 V	1.9	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3 V	3.4	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 5 V	2.5	ns
C_I	input capacitance		2	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 10 MHz; VCC = 3.3 V; notes 1 and 2	16	pF
C_S	switch capacitance	OFF-state	5	pF
		ON-state	9.5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L + C_S) \times V_{CC}^2 \times f_o$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   C_S = max. switch capacitance in pF;

   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT E	SWITCH
L	OFF
H	ON

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G66GW	–40 to +85 °C	5	SC-88A	plastic	SOT353	VL

PINNING

PIN	SYMBOL	DESCRIPTION
1	Y	independent input/output
2	Z	independent output/input
3	GND	ground (0 V)
4	E	enable input (active HIGH)
5	V_{CC}	supply voltage

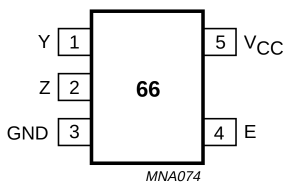


Fig.1 Pin configuration.

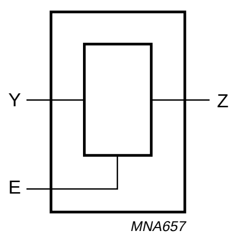


Fig.2 Logic symbol.

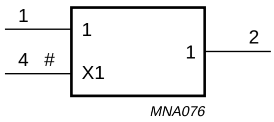


Fig.3 IEC logic symbol.

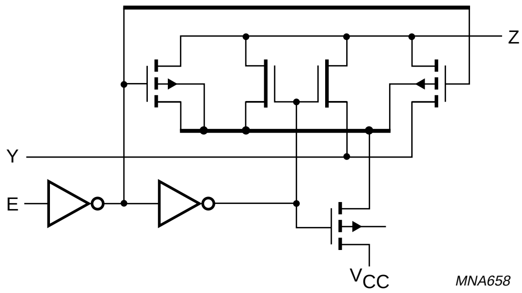


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_S	switch voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r,t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); see note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	–	–50	mA
I_{SK}	switch diode current	$V_S < -0.5$ or $V_S > V_{CC} + 0.5$ V	–	±50	mA
I_S	switch source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V	–	±50	mA
I_{CC}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +85 °C; note 2	–	200	mW

Notes

1. To avoid drawing V_{CC} current out of pin Z, when switch current flows into pin Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin Z, no V_{CC} current will flow out of pin Y. In this case there is no limit for the voltage drop across the switch, but the voltage at pins Y and Z may not exceed V_{CC} or GND.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

DC CHARACTERISTICS

With regard to recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
				–40 to +85			
		OTHER	V_{CC} (V)	MIN.	TYP.[1]	MAX.	
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.30 \times V_{CC}$	V
I_I	input leakage current (control pin)	V_I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I_S	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ – GND; see Fig.6	5.5	–	±0.1	±5	μA
I_S	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ – GND; see Fig.7	5.5	–	±0.1	±5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC}$ – 0.6 V; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	5	500	μA

Note

1. All typical values are at T_{amb} = 25 °C.

Type 74LVC1G66

SYMBOL	PARAMETER	TEST CONDITIONS			T_{amb} (°C)			UNIT
		OTHER	I_S (mA)	V_{CC} (V)	−40 to +85			
					MIN.	TYP.[1]	MAX.	
R_{ON}	ON-resistance (peak)	V_S = GND to V_{CC}; V_I = V_{IH}; see Fig.5	4	1.65 – 1.95	–	35	100	Ω
			8	2.3 – 2.7	–	14	30	Ω
			12	2.7	–	11.5	25	Ω
			24	3.0 – 3.6	–	8.5	20	Ω
			32	4.5 – 5.5	–	6.5	15	Ω
	ON-resistance (rail)	V_S = GND; V_I = V_{IH}; see Fig.5	4	1.65 – 1.95	–	10	30	Ω
			8	2.3 – 2.7	–	8.5	20	Ω
			12	2.7	–	7.5	18	Ω
			24	3.0 – 3.6	–	6.5	15	Ω
			32	4.5 – 5.5	–	6	10	Ω
	ON-resistance (rail)	V_S = V_{CC}; V_I = V_{IH}; see Fig.5	4	1.65 – 1.95	–	12	30	Ω
			8	2.3 – 2.7	–	8.5	20	Ω
			12	2.7	–	7.5	18	Ω
			24	3.0 – 3.6	–	6.5	15	Ω
			32	4.5 – 5.5	–	6	10	Ω
	ON-resistance (flatness)	V_S = GND to V_{CC}; V_I = V_{IH}; see Figs 9 to 12	4	1.8	–	100[2]	–	Ω
			8	2.5	–	17[2]	–	Ω
			12	2.7	–	10[2]	–	Ω
			24	3.3	–	5[2]	–	Ω
			32	5.0	–	3[2]	–	Ω

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. R_{ON} flatness over operating temperature range (–40 to +85 °C).

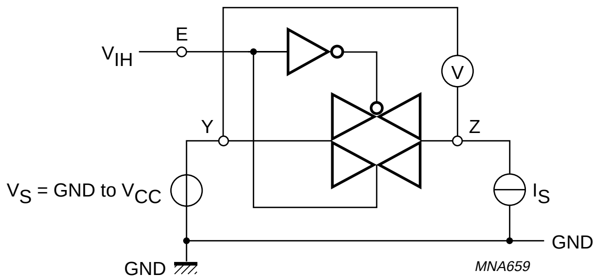


Fig.5 Test circuit for measuring ON-resistance (R_{ON}).

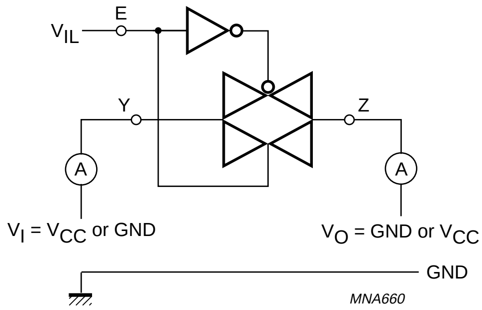


Fig.6 Test circuit for circuit OFF-state current.

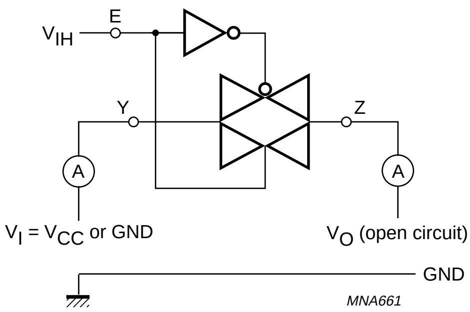


Fig.7 Test circuit for measuring ON-state current.

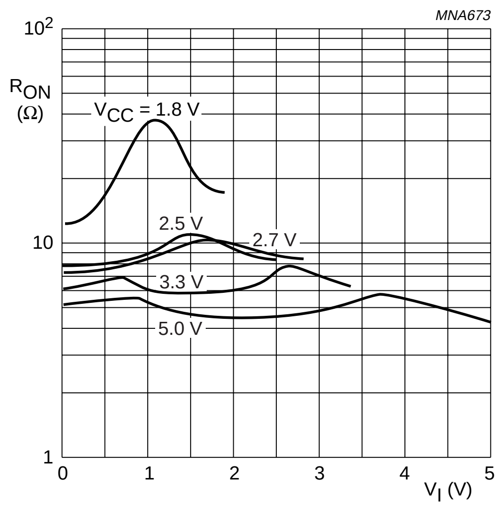


Fig.8 Typical ON-resistance (R_{ON}) as a function of input voltage (V_S) for V_S = GND to V_{CC}.

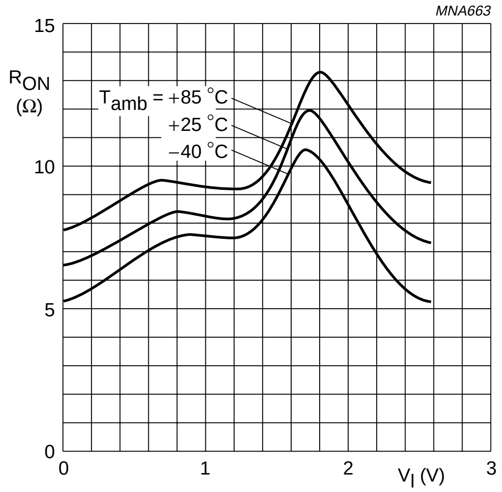


Fig.9 R_{ON} for V_{CC} = 2.5 V.

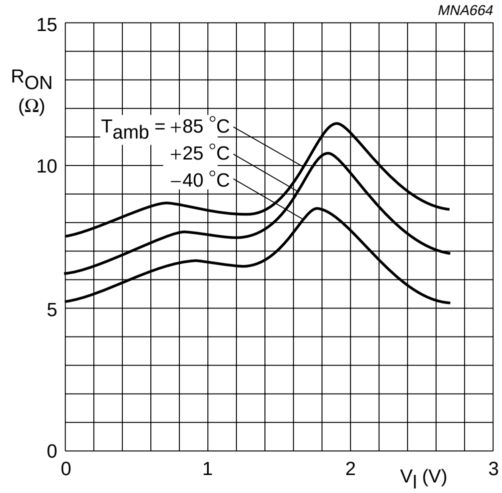


Fig.10 R_{ON} for V_{CC} = 2.7 V.

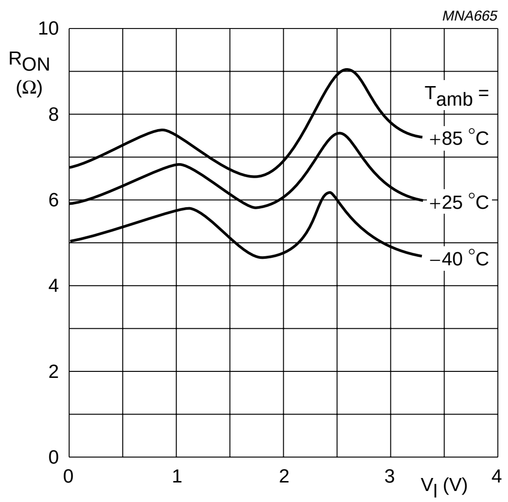


Fig.11 R_{ON} for V_{CC} = 3.3 V.

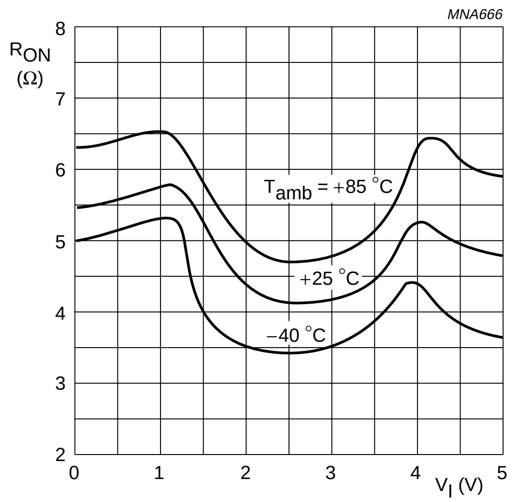


Fig.12 R_{ON} for V_{CC} = 5.0 V.

AC CHARACTERISTICS

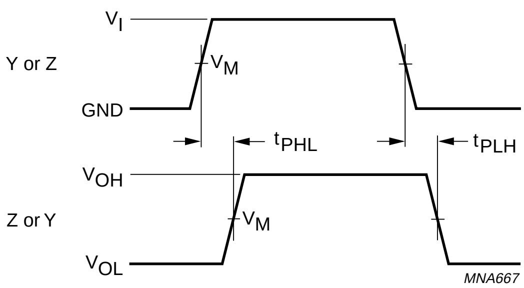
GND = 0 V; $t_r = t_f \leq 2.0$ ns; C_L = 30 pF; R_L = 1 kΩ; V_{CC} = 1.65 to 1.95 V;
GND = 0 V; $t_r = t_f \leq 2.0$ ns; C_L = 30 pF; R_L = 500 Ω; V_{CC} = 2.3 to 2.7 V;
GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 500 Ω; $V_{CC} \geq$ 2.7 V.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		WAVEFORMS	V_{CC} (V)	–40 to +85			
				MIN.	TYP.[1]	MAX.	
t_{PHL}/t_{PLH}	propagation delay inA; inB to outY	see Figs 13 and 15	1.65 to 1.95	–	0.8	2	ns
			2.3 to 2.7	–	0.4	1.2	ns
			2.7	–	0.4	1	ns
			3.0 to 3.6	–	0.3	0.8	ns
			4.5 to 5.5	–	0.2	0.6	ns
t_{PZH}/t_{PZL}	turn-ON time E to V_{OS}	see Figs 14 and 15	1.65 to 1.95	1	5.3	12	ns
			2.3 to 2.7	1	3.0	6.5	ns
			2.7	1	2.6	6	ns
			3.0 to 3.6	1	2.5	5	ns
			4.5 to 5.5	1	1.9	4.2	ns
t_{PHZ}/t_{PLZ}	turn-OFF time E to V_{OS}	see Figs 14 and 15	1.65 to 1.95	1	4.2	10	ns
			2.3 to 2.7	1	2.4	6.9	ns
			2.7	1	3.6	7.5	ns
			3.0 to 3.6	1	3.4	6.5	ns
			4.5 to 5.5	1	2.5	5	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

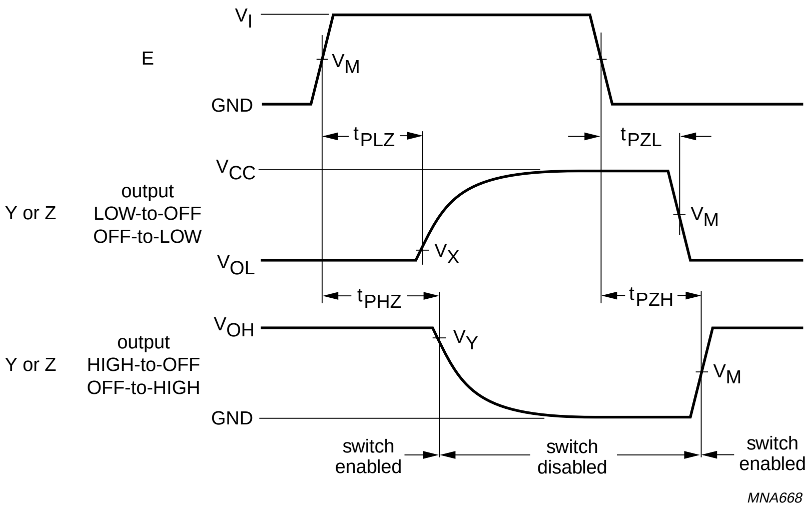
AC WAVEFORMS



V_{CC}	V_M	V_I	INPUT $t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7; V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.13 The input (V_S) to output (V_O) propagation delays.

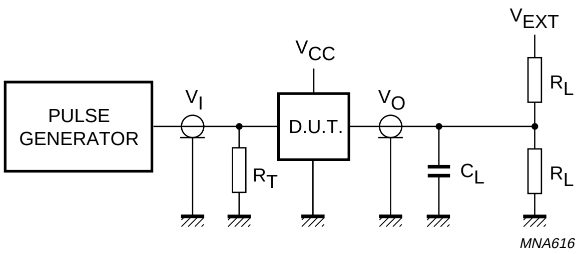


V_{CC}	V_M	V_I	INPUT $t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.14 The turn-on and turn-off times.



				V_{EXT}		
V_{CC}	**V_I**	**C_L**	**R_L**	**t_{PLH}/t_{PHL}**	**t_{PZH}/t_{PHZ}**	**t_{PZL}/t_{PLZ}**
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.15 Load circuitry for switching times.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LVC1G66

Recommended conditions and all typical values are measured at T_{amb} = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	TYPICAL	UNIT
	sine-wave distortion	R_L = 10 kΩ; C_L = 50 pF; f_{in} = 1 kHz; see Fig.17	1.65	0.032	%
			2.3	0.008	%
			3	0.006	%
			4.5	0.001	%
		R_L = 10 kΩ; C_L = 50 pF; f_{in} = 10 kHz; see Fig.17	1.65	0.068	%
			2.3	0.009	%
			3	0.008	%
			4.5	0.006	%
	switch ON signal frequency response	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1 MHz; see Fig.16; note 1	1.65	135	MHz
			2.3	145	MHz
			3	150	MHz
			4.5	155	MHz
		R_L = 50 Ω; C_L = 5 pF; f_{in} = 1 MHz; see Fig.16; note 1	1.65	>500	MHz
			2.3	>500	MHz
			3	>500	MHz
			4.5	>500	MHz
	switch OFF signal feed-through attenuation	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1 MHz; see Fig.18; note 2	1.65	–46	dB
			2.3	–46	dB
			3	–46	dB
			4.5	–46	dB
		R_L = 0 Ω; C_L = 50 pF; f_{in} = 1 MHz; see Fig.18; note 2	1.65	–37	dB
			2.3	–37	dB
			3	–37	dB
			4.5	–37	dB
	crosstalk (control input to signal output)	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1 MHz; t_r = t_f = 2 ns; see Fig.19	1.65	69	mV
			2.3	87	mV
			3	156	mV
			4.5	302	mV
	minimum frequency response (–3 dB)	R_L = 50 Ω; C_L = 10 pF; see Fig.16; note 1	1.65	200	MHz
			2.3	350	MHz
			3	410	MHz
			4.5	440	MHz

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	TYPICAL	UNIT
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_{in} = 10 MHz	2.5	13.7	pF
			3.3	15.2	pF
			5.0	18.3	pF
Q	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f = 1 Mhz; R_L = 1 MΩ; see Fig.20; note 3	1.65 to 5.5	0.05	pC

Notes

1. Adjust f_{in} voltage to obtain 0 dBm level at output. Increase f_{in} frequency until dB meter reads –3 dB.
2. Adjust f_{in} voltage to obtain 0 dBm level at input.
3. Guaranteed by design.

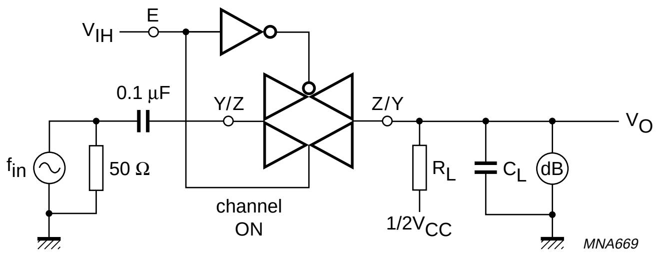
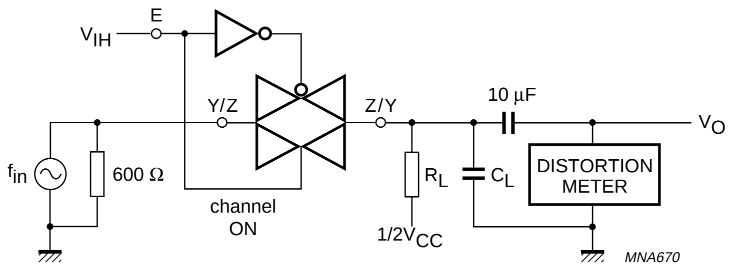


Fig.16 Test circuit for measuring the frequency response when switch is ON.



V_{CC}	V_I
1.65 V	1.4 V_{p-p}
2.3 V	2 V_{p-p}
3 V	2.5 V_{p-p}
4 V	4 V_{p-p}

Fig.17 Test circuit for measuring sine-wave distortion.

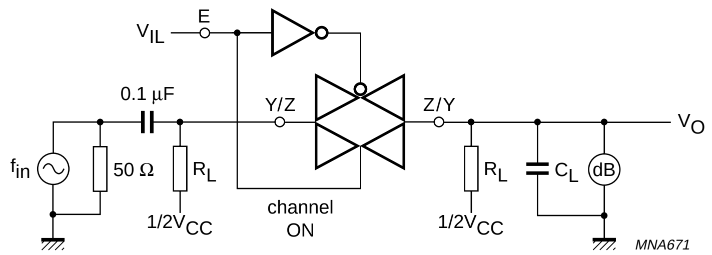


Fig.18 Test circuit for measuring feed-through when switch is OFF.

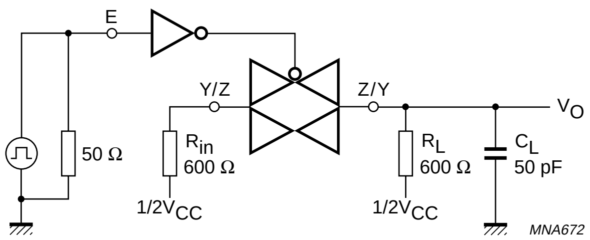
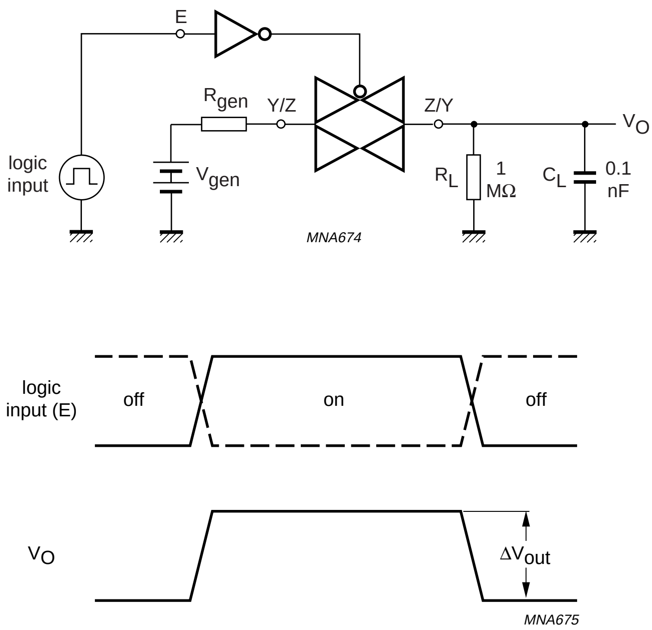


Fig.19 Crosstalk.

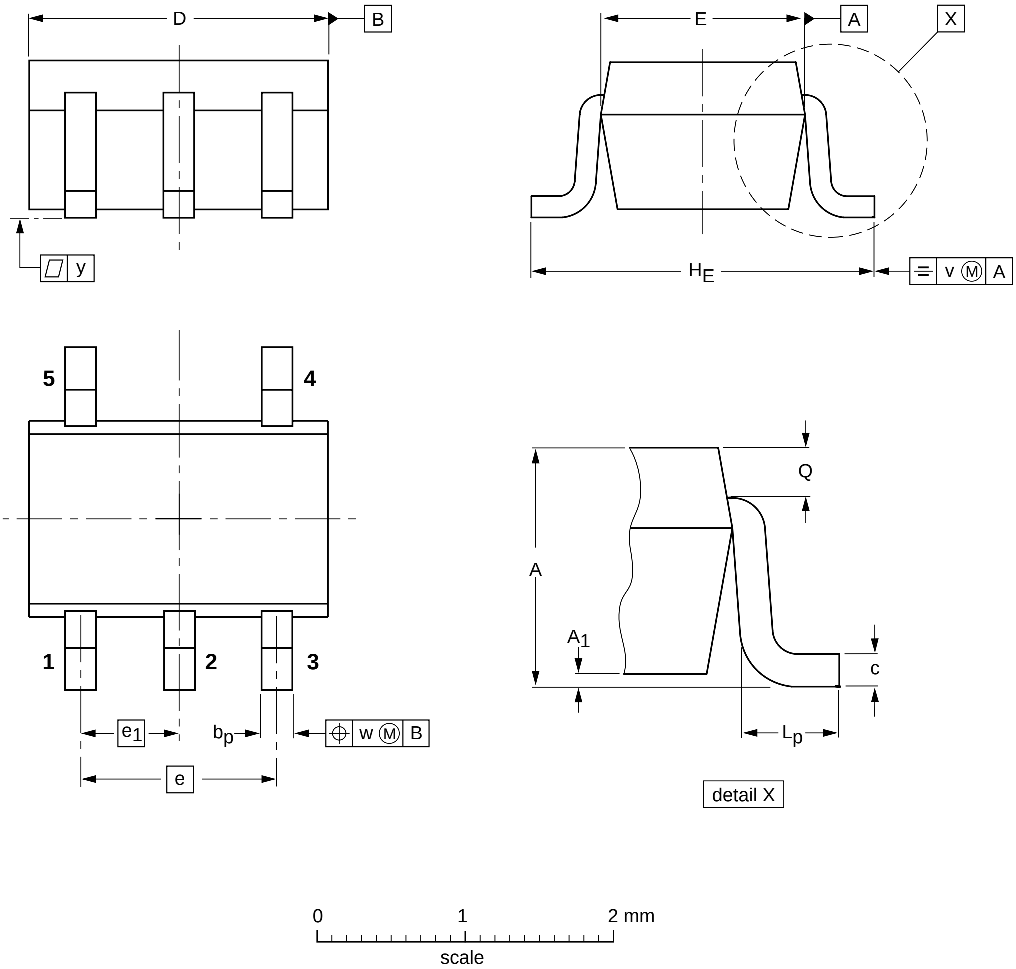


$Q = (\Delta V_{out}) . (C_L)$

Fig.20 Charge injection test.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT353**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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