

74LVC241A

Octal buffer/line driver with 5 V tolerant inputs/outputs;
3-state

Rev. 5 — 16 December 2011

Product data sheet

1. General description

The 74LVC241A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs (pins $\overline{1OE}$ and 2OE). Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5.0 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- High-impedance when $V_{CC} = 0$ V
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC241AD	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC241ADB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC241APW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

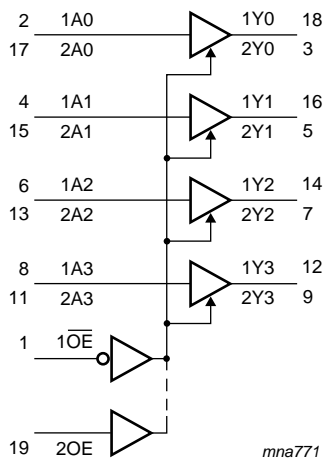


Fig 1. Logic symbol

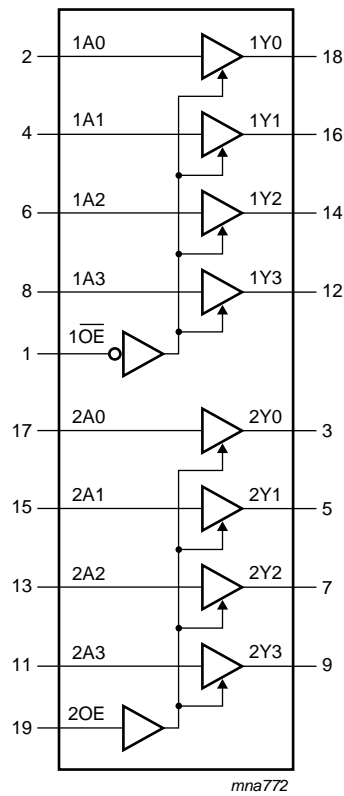


Fig 2. Functional diagram

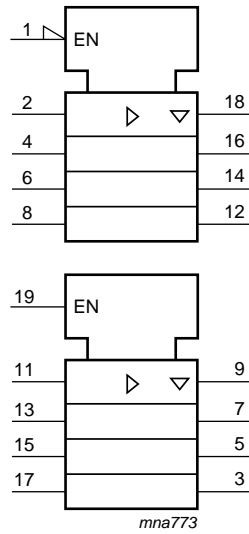


Fig 3. IEC logic symbol

5. Pinning information

5.1 Pinning

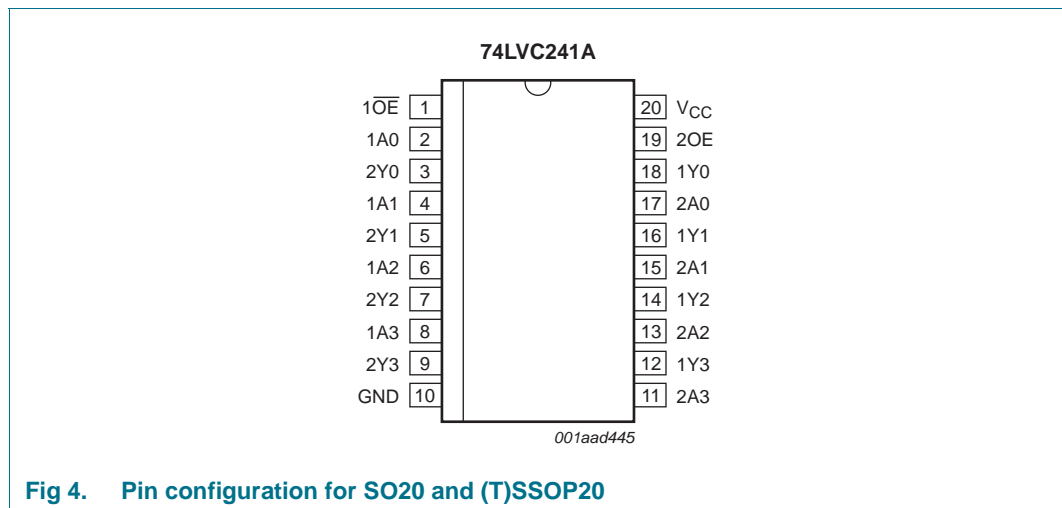


Fig 4. Pin configuration for SO20 and (T)SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$	1	output enable input (active LOW)
2OE	19	output enable input (active HIGH)
1A[0:3]	2, 4, 6, 8	data input
2A[0:3]	17, 15, 13, 11	data input
1Y[0:3]	18, 16, 14, 12	bus output

Table 2. Pin description ...continued

Symbol	Pin	Description
2Y[0:3]	3, 5, 7, 9	bus output
GND	10	ground (0 V)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table^[1]

Input				Output	
1OE	1An	2OE	2An	1Yn	2Yn
L	L	-	-	L	-
L	H	-	-	H	-
H	X	-	-	Z	-
-	-	H	L	-	L
-	-	H	H	-	H
-	-	L	X	-	Z

[1] H = HIGH voltage level; L = LOW voltage level, X = don't care, Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	HIGH-or LOW-state	^[2] -0.5	V _{CC} + 0.5	V
		3-state	^[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above $70\text{ }^{\circ}\text{C}$ the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP20 packages: above $60\text{ }^{\circ}\text{C}$ the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH-or LOW-state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V}$ to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND;	-	±0.1	±5	-	±20	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	1An to 1Yn; 2An to 2Yn; see Figure 5 ^[2]						
		V _{CC} = 1.2 V	-	11	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	5.9	14.1	1.5	16.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.2	7.3	1.0	8.4	ns
		V _{CC} = 2.7 V	1.5	3.2	7.1	1.5	8.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.7	6.1	1.5	7.1	ns
t _{en}	enable time	1OE to 1Yn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	13	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.6	16.2	1.5	18.6	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.7	8.9	1.5	10.3	ns
		V _{CC} = 2.7 V	1.5	3.8	8.1	1.5	9.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.0	7.1	1.5	8.2	ns
		2OE to 2Yn; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	13	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	5.5	13.8	2.5	15.8	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	4.2	7.4	2.1	8.5	ns
		V _{CC} = 2.7 V	1.5	3.7	8.1	1.5	9.4	ns
V _{CC} = 3.0 V to 3.6 V	1.5	3.4	7.1	1.5	8.2	ns		
t _{dis}	disable time	1OE to 1Yn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	8	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	4.3	10.0	2.5	11.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.5	5.6	1.0	6.5	ns
		V _{CC} = 2.7 V	1.5	3.2	7.0	1.5	8.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.0	6.0	1.5	6.9	ns
		2OE to 2Yn; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	8	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	3.5	9.9	1.5	11.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	3.1	5.6	0.5	6.4	ns
		V _{CC} = 2.7 V	1.5	3.4	7.0	1.5	8.1	ns
V _{CC} = 3.0 V to 3.6 V	1.5	2.6	6.0	1.5	6.9	ns		
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V ^[3]	-	-	1.0	-	1.5	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	per buffer; V _i = GND to V _{CC}						
		V _{CC} = 1.65 V to 1.95 V	-	14.4	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	17.9	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	21.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
 t_{en} is the same as t_{PZL} and t_{PZH}.
 t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

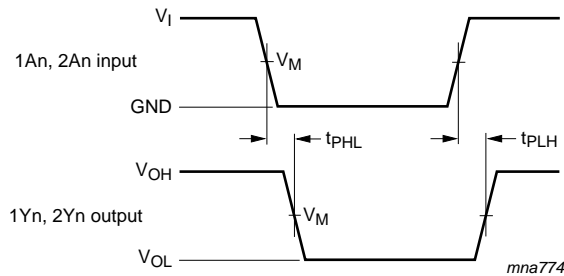
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs

11. AC waveforms

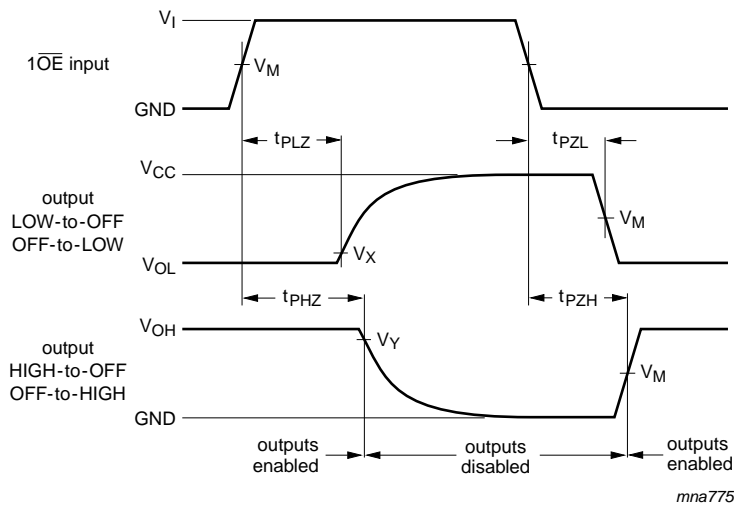


V_M = 1.5 V at V_{CC} ≥ 2.7 V;

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V;

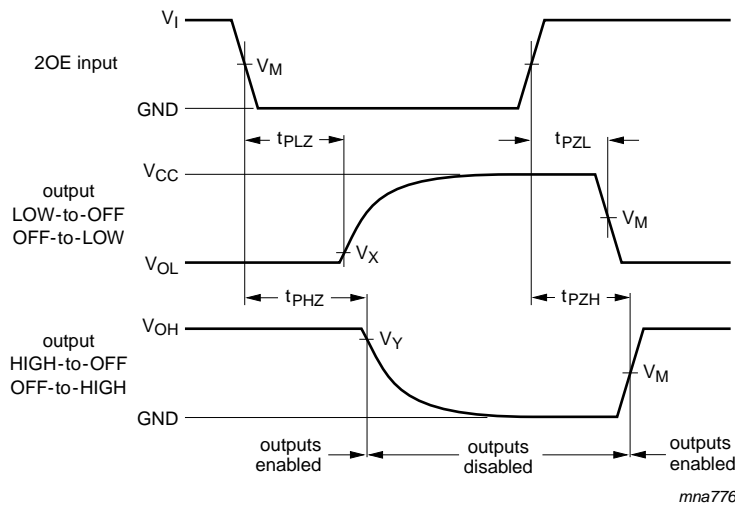
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Input (1An and 2An) to output (1Yn and 2Yn) propagation delays



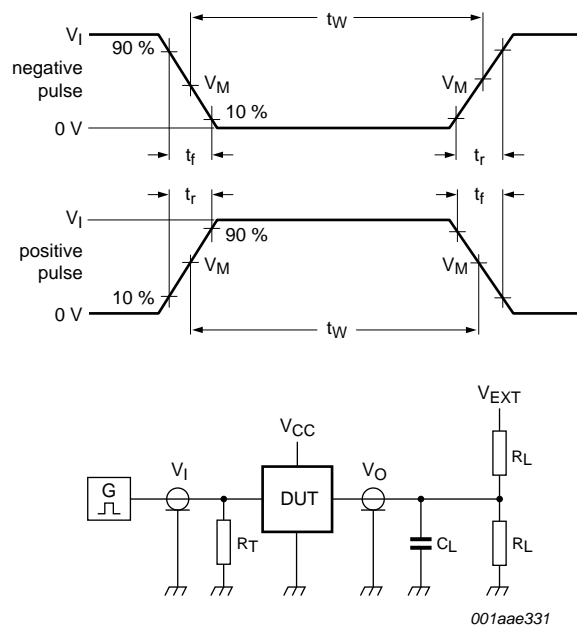
$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$.
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
 $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;
 $V_X = V_{OL} + 0.15 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.
 $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;
 $V_Y = V_{OH} - 0.15 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.

Fig 6. 3-state enable and disable times for input 1OE



$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$. $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
 $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;
 $V_X = V_{OL} + 0.15 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.
 $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;
 $V_Y = V_{OH} - 0.15 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.

Fig 7. 3-state enable and disable times for input 2OE



Test data is given in [Table 8](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

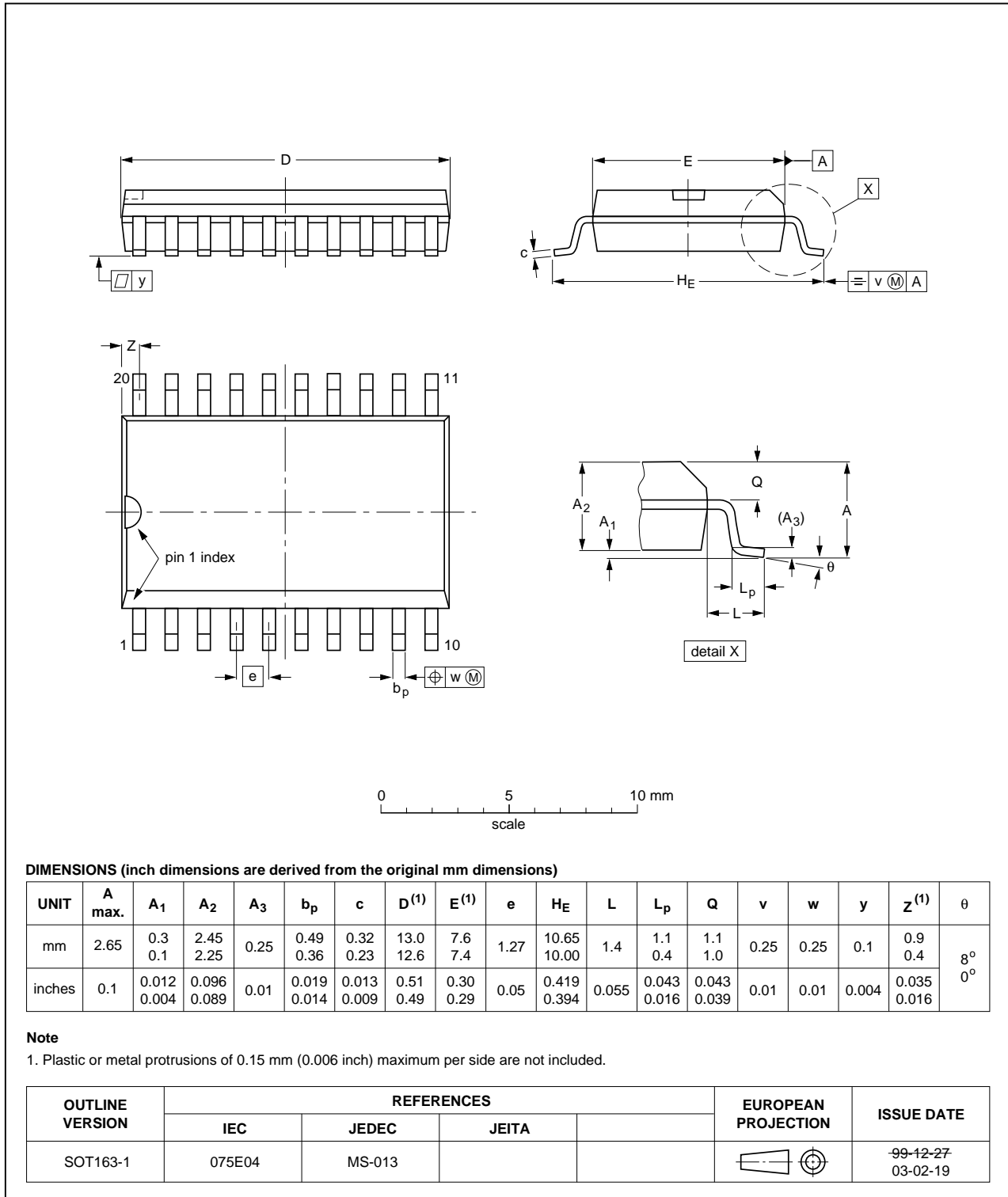


Fig 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

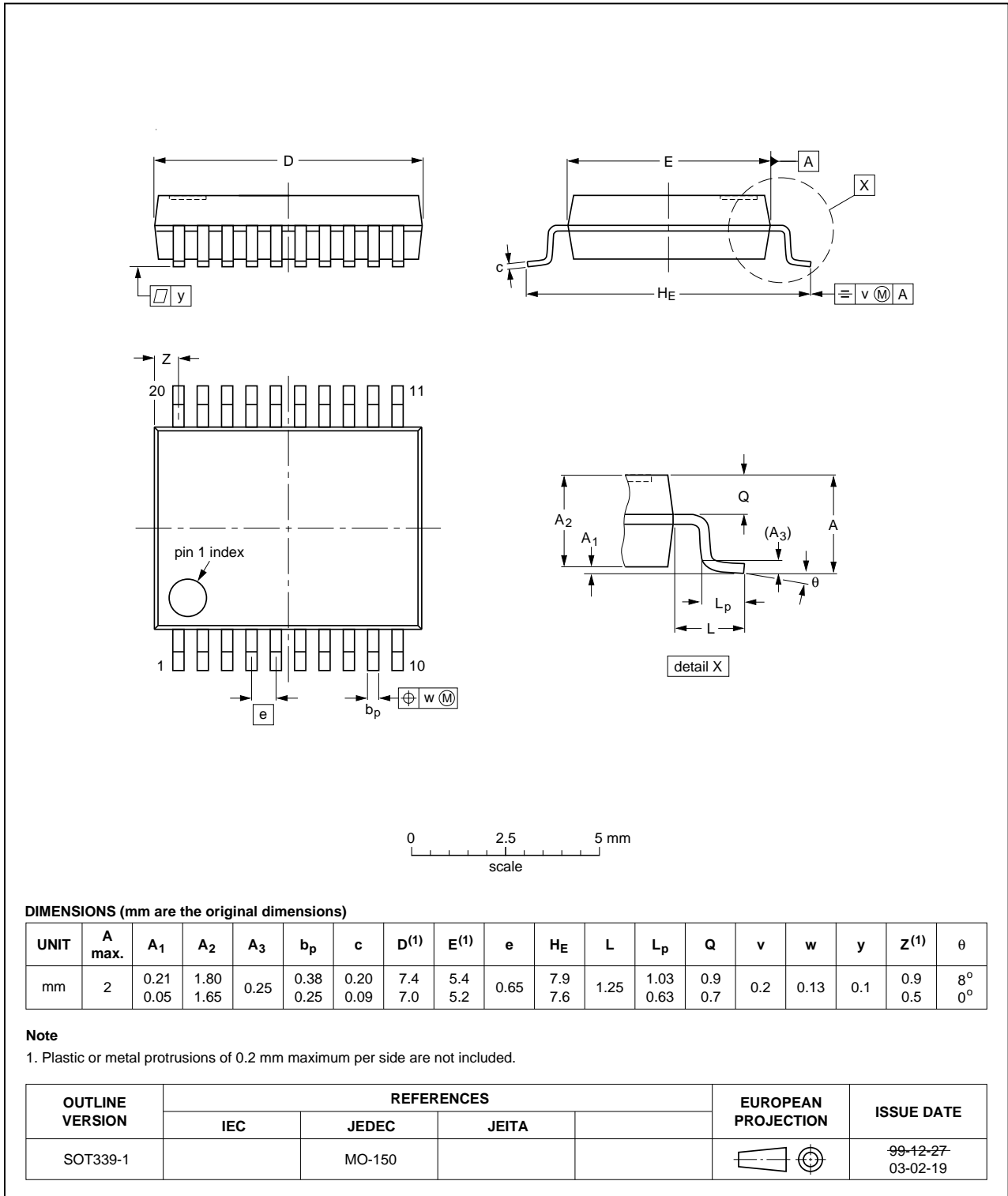


Fig 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

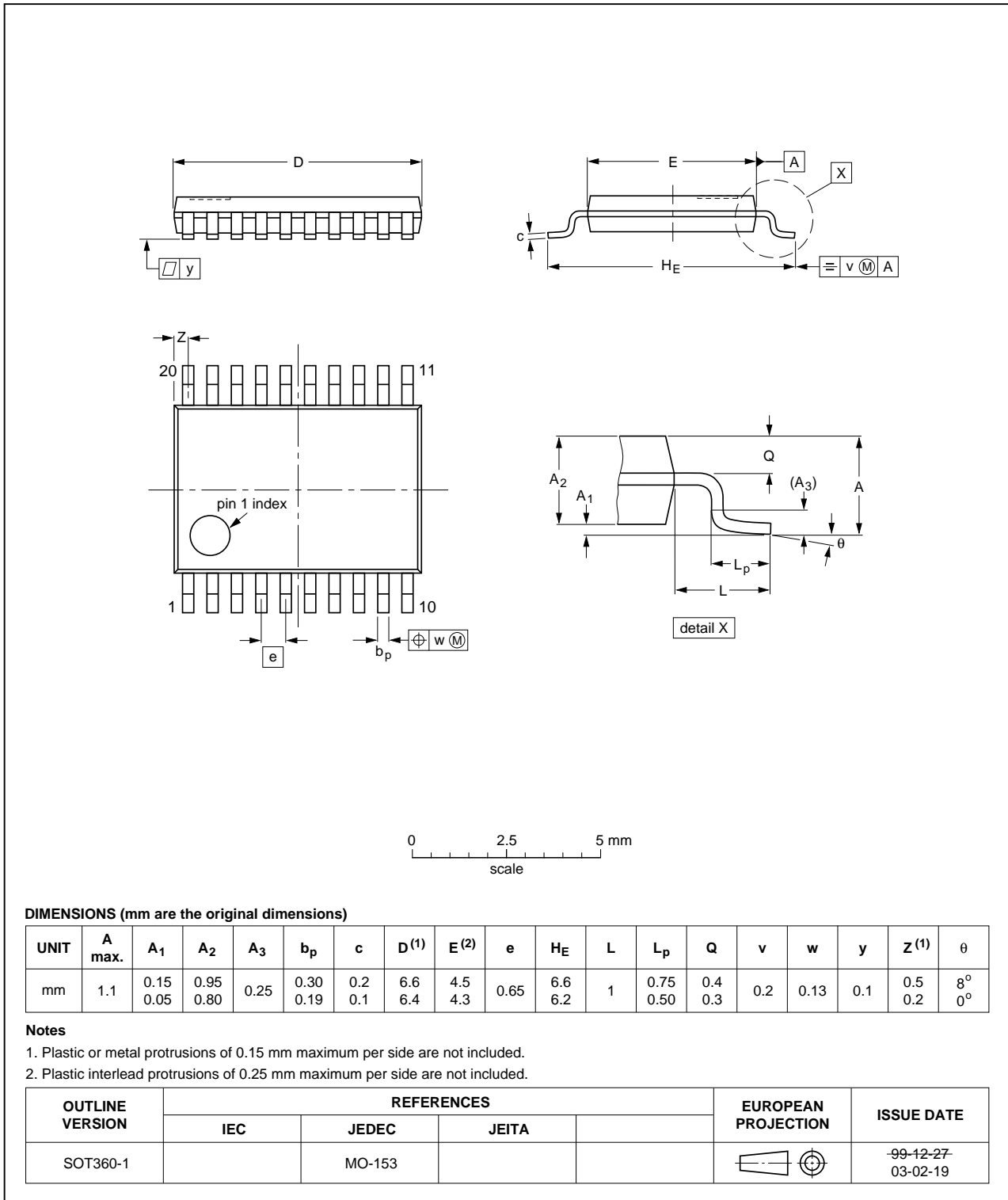


Fig 11. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC241A v.5	20111216	Product data sheet	-	74LVC241A v.4
Modifications:	<ul style="list-style-type: none"> • Table 7: maximum values for lower voltage ranges changed (errata). 			
74LVC241A v.4	20111123	Product data sheet	-	74LVC241A v.3
Modifications:	<ul style="list-style-type: none"> • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. 			
74LVC241A v.3	19980520	Product specification	-	74LVC241A v.2
74LVC241A v.2	19970729	Product specification	-	74LVC241A v.1
74LVC241A v.1	-	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	4
8	Recommended operating conditions	5
9	Static characteristics	6
10	Dynamic characteristics	7
11	AC waveforms	8
12	Package outline	11
13	Abbreviations	14
14	Revision history	14
15	Legal information	15
15.1	Data sheet status	15
15.2	Definitions	15
15.3	Disclaimers	15
15.4	Trademarks	16
16	Contact information	16
17	Contents	17

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