



OCTAL BUFFER/LINE DRIVER WITH 3 STATE OUTPUTS

Description

The 74LVC244A provides two 4-bit line drivers with separate outputenable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

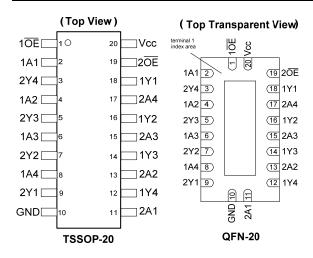
The device is designed for operation with a power supply range of 1.65V to 3.6V.

The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using l_{OFF} . The l_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

Features

- Supply Voltage Range from 1.65V to 3.6V
- Sinks or Sources 24ma at V_{CC} = 3V
- CMOS Low Power Consumption
- I_{OFF} Supports Partial Power Down Operation
- Inputs or Outputs Accept up to 5.5V
- Inputs can be Driven by 3.3V or 5V Allowing for Mixed Voltage Applications
- Schmitt Trigger Action at All Inputs
- Typical V_{OLP} (Quiet Output Ground Bounce) Less than 0.8V with V_{CC} = 3.3V and T_A = +25°C
- Typical V_{OHV} (Quiet Output Dynamic VOH) Greater than 2.0V with V_{CC} = 3.3V and T_A = +25°C
- ESD Protection Tested per JESD 22
 - Exceeds 200-V Machine Model (A115)
 - Exceeds 2000-V Human Body Model (A114)
 - Exceeds 1000-V Charged Device Model (C101)
- Latch-Up Exceeds 250mA per JESD 78, Class I
- All devices are:
 - Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)
 - Halogen and Antimony Free. "Green" Device (Note 3)

Pin Assignments



Applications

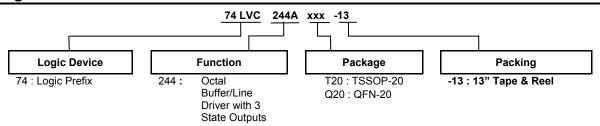
- General Purpose Logic
- Bus Driving
- Power Down Signal Isolation
- Wide array of products such as:
 - PCs, Notebooks, Netbooks, Ultrabooks
 - Networking Computer Peripherals, Hard Drives, CD/DVD ROM
 - TV, DVD, DVR, Set Top Box

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
- 3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



Ordering Information



Part Number	Package	Package	Package	13" Таре	13" Tape and Reel		
Part Number	Code	(Note 4 & 5)	Size	Quantity	Part Number Suffix		
74LVC244AT20-13	T20	TSSOP-20	6.4mm X 6.5mm X 1.2mm 0.65 mm lead pitch	2500/Tape & Reel	-13		
74LVC244AQ20-13	Q20	V-QFN4525-20	2.5mm X 4.5mm X 0.95mm 0.50 mm lead pitch	2500/Tape & Reel	-13		

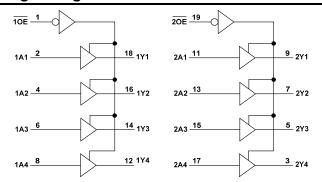
Notes:

- 4. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
- 5. V-QFN4525-20 is a JEDEC recognized naming convention that specifies the package thickness category as V and the number 4525 describes the package as 4.5mm X 2.5mm.

Pin Descriptions

Pin Number	Pin Name	Description
1	10E	Output Enable 1
2	1A1	Data Input
3	2Y4	Data Output
4	1A2	Data Input
5	2Y3	Data Output
6	1A3	Data Input
7	2Y2	Data Output
8	1A4	Data Input
9	2Y1	Data Output
10	GND	Ground
11	2A1	Data Input
12	1Y4	Data Output
13	2A2	Data Input
14	1Y3	Data Output
15	2A3	Data Input
16	1Y2	Data Output
17	2A4	Data Input
18	1Y1	Data Output
19	2OE	Output Enable 2
20	V _{cc}	Supply Voltage

Logic Diagram



Function Table

(E	(Each 4-Bit Buffer)						
INPU	OUTPUT						
ŌE	Α	Y					
L	Н	Н					
L	L	L					
Н	Х	Z					



Absolute Maximum Ratings (Notes 6 & 7)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
Vcc	Supply Voltage Range	-0.5 to +7.0	V
VI	Input Voltage Range	-0.5 to +7.0	V
I _{IK}	Input Clamp Current V _I < 0V	-20	mA
lok	Output Clamp Current V _O < 0V	-50	mA
Io	Continuous Output Current -0.5V < V _O V _{CC} +0.5V	±50	mA
Icc	Continuous Current Through V _{CC}	100	mA
I _{GND}	Continuous Current Through GND	-100	mA
TJ	Operating Junction Temperature	-40 to +150	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _{TOT}	Total Power Dissipation	500	mW

Notes:

- 6. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
- 7. Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.

Recommended Operating Conditions (Note 8)

Symbol	Parameter	Conditions	Min	Max	Unit
1/	Cupply Voltage	Operating	1.65	3.6	V
V_{CC}	Supply Voltage	Data Retention Only	1.5	_	V
VI	Input Voltage	_	0	5.5	V
Vo	Output Voltage	_	0	V _{CC}	V
		V _{CC} = 1.65V	_	-4	
	High Lovel Output Current	V _{CC} = 2.3V	_	-8	A
Іон	High-Level Output Current	V _{CC} = 2.7V	_	-12	mA mA
		V _{CC} = 3.0V	_	-24	
		V _{CC} = 1.65V	_	4	
	Land and Ortant Orman	V _{CC} = 2.3V	_	8	
l _{OL}	Low-Level Output Current	V _{CC} = 2.7V	_	12	mA mA
		V _{CC} = 3.0V	_	24	İ
Δt/ΔV	Input Transition Rise or Fall Rate		_	10	ns/V
T _A	Operating Free-Air Temperature		-40	+125	°C

Note

8. Unused inputs should be held at V_{CC} or ground.



Electrical Characteristics

Comple al	Danamatan	Test Conditions	V	T _A = -40°C	to +85°C	T _A = -40°	to +125°C	11
Symbol	Parameter	lest Conditions	V _{CC}	Min	Max	Min	Max	Unit
			1.65V to 1.95V	V _{CC} X 0.65	_	V _{CC} X 0.65	_	
V_{IH}	High-Level Input Voltage		2.3V to 2.7V	1.7	_	1.7	_	V
	Voltage		3.0V to 3.6V	2	_	2	_	
	Lave Lavellin and		1.65V to 1.95V	_	V _{CC} X 0.35	_	V _{CC} X 0.35	
V_{IL}	Low-Level input Voltage		2.3V to 2.7V	_	0.7	_	0.7	V
	voltago		3.0V to 3.6V	_	0.8	_	0.8	
		I _{OH} = -50μA	1.65V to 3.6V	V _{CC} -0.2	_	V _{CC} -0.3	_	
		I _{OH} = -4mA	1.65V	1.2	_	1.05	_	
\/	High-Level	I _{OH} = -8mA	2.3V	1.7	_	1.65	_	
V_{OH}	Output Voltage	10. 4	2.7V	2.2	_	2.05	_	
		I _{OH} = -12mA	3.0V	2.4	_	2.48	_	V
		I _{OH} = -24mA	3.0V	2.3	_	2.0	_	
		I _{OL} = 100μA	1.65V to 3.6V	_	0.2	_	0.3	
		I _{OL} = 4mA	1.65V	_	0.45	_	0.65	
V_{OL}	Low-Level Output Voltage	I _{OL} = 8mA	2.3V	_	0.60	_	0.80	V
	voltage	I _{OL} = 12mA	2.7V	_	0.40	_	0.60	
		I _{OL} = 24mA	3.0V	_	0.55	_	0.80	
I _{OFF}	Power Down Leakage Current	V_1 or $V_0 = 0$ or 5.5V	0V	_	±10	_	20	μΑ
l _l	Input Current Control Pins	V _I =GND or 5.5V	0 to 3.6V	_	±5	_	± 20	μΑ
I _{OZ}	Z-state Current including Input Current I/O Pins	V _I =GND or 5.5V V _O = 0 to 5.5V	3.6V	_	±5	_	± 20	μА
Icc	Supply Current	$V_I = GND \text{ or } V_{CC}, I_O = 0$	3.6V	_	10	_	40	μΑ
Δlcc	Additional Supply Current	One input at V_{CC} -0.6V, Io = 0A	2.7V to 3.6V	_	500	_	5000	μΑ
C _i	Input Capacitance	Control Pins V _I = GND or	0V to 3.6V	4.0 ty	pical	4.0 ty	pical	pF
	Сараспапсе	I/O Pins Vcc		5.5 ty	pical	5.5 ty	pical	•



Switching Characteristics

Symbol	Parameter	Test Conditions	Vcc	-	Γ _A = +25°(3		-40° to 5°C		-40° to :5°C	Unit			
		Conditions		Min	Тур	Max	Min	Max	Min	Max	7			
			1.5V	1	7	16.9	1	18.9	1	20.4				
	Propagation		1.8V ± 0.15V	1	6.0	11.4	1	11.3	1	12.4				
t _{PD}	Delay A _N to Y _N	Figure 1	2.5V ± 0.2V	1	3.9	7.4	1	8.0	1	10.0	ns			
			2.7V	1	4.2	7.7	1	8.5	1	8.8				
			$3.3V \pm 0.3$	1.5	3.8	7.3	1.5	7.7	1.5	7.9				
	Enable Time OE to Y _N Figure 1		1.5V	1	12.4	18.3	1	19.8	1	25.4				
				Enable Time		1.8V ± 0.15V	1	6.4	12.1	1	12.6	1	14.1	
t _{EN}				Figure 1	2.5V ± 0.2V	1	4.6	9.1	1	9.6	1	11.7	ns	
			2.7V	1	5	8.4	1	8.6	1	10.3				
			$3.3V \pm 0.3$	1.5	4.5	7.4	1.5	7.6	1.5	9.4				
			1.5V	1	7.2	15.6	1	16.1	1	17.6				
	Disable Time		1.8V ± 0.15V	1	5.8	11.6	1	12.1	1	13.6				
t _{DIS}		Figure 1	2.5V ± 0.2V	1	3.7	7.3	1	7.8	1	9.9	ns			
			2.7V	1	3.8	6.6	1	6.8	1	8.6				
			3.3V ± 0.3	1.5	3.8	6.3	1.5	6.5	1.5	8				
t _{sk(0)}	Output Skew Time		3.3V ± 0.3	_	_	1.0	_	_	_	1.5	ns			

Operating Characteristics

 $T_A = +25^{\circ}C$

Symbol	Parameter	Test Conditions	V _{CC}	Тур	Unit
	Dawer dissination	F= 10 MHz	1.8V± 0.15V	9.9	
C_pd	Power dissipation	Outputs Enabled	2.5V± 0.2V	10.2	pF
	capacitance per gate		3.3V± 0.3V	10.6	1

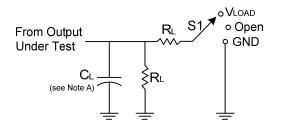
Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Тур	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	TSSOP-20	(Note 9)	_	74	_	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	TSSOP-20	(Note 9)	_	15	_	°C/W
θ_{JA}	Thermal Resistance Junction-to-Ambient	V-QFN4525-20	(Note 9)	_	67	_	°C/W
θ _{JC}	Thermal Resistance Junction-to-Case	V-QFN4525-20	(Note 9)	_	20	_	°C/W

Note: 9. Test conditions for TSSOP-20 and V-QFN4525-20: Devices mounted on 4 layer FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout per JESD 51-7.

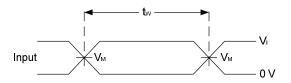


Parameter Measurement Information

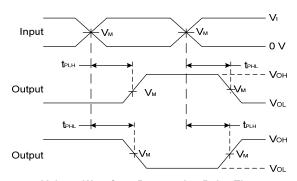


TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{LOAD}
t _{PHZ} /t _{PZH}	GND

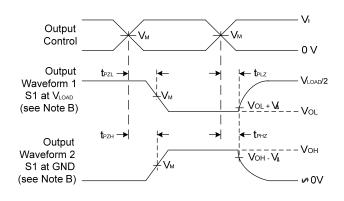
.,	Inputs		, , , , , , , , , , , , , , , , , , ,			_		
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R_L	$\mathbf{V}\Delta$	
1.8V ± 0.15V	V_{CC}	≤2ns	V _{CC} /2	2 x V _{CC}	30pF	1ΚΩ	0.15V	
2.5V ± 0.2V	Vcc	≤2ns	V _{CC} /2	2 x V _{CC}	30pF	500Ω	0.15V	
2.7V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V	
3.3V ± 0.3V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V	



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs



Voltage Waveform Enable and Disable Times Low and High Level Enabling

Notes: A. Includes test lead and test apparatus capacitance.

B. All pulses are supplied at pulse repetition rate \leq 10 MHz.

C. Inputs are measured separately one transition per measurement.

D. t_{PLZ} and t_{PHZ} are the same as $t_{\text{dis.}}$

E. t_{PZL} and t_{PZH} are the same as t_{EN0}

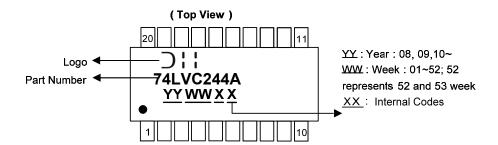
F. t_{PLH} and t_{PHL} are the same as t_{PD.}

Figure 1 Load Circuit and Voltage Waveforms



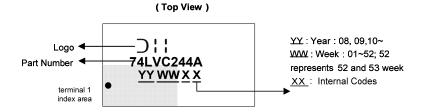
Marking Information

(1) TSSOP20



Part Number	Package
74LVC244AT20	TSSOP-20

(2) QFN-20 (V-QFN4525-20)



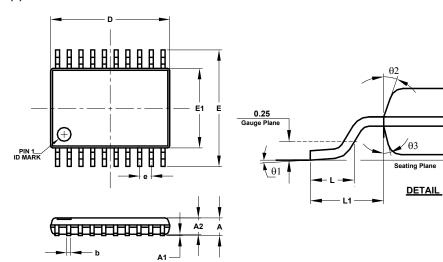
Part Number	Package
74LVC244AQ20	V-QFN4525-20



Package Outline Dimensions (All Dimensions in mm)

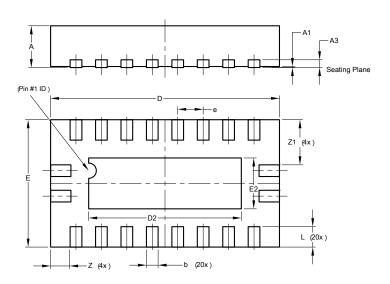
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

(1) TSSOP-20



TSSOP-20				
Dim	Min	Max	Тур	
Α	-	1.20	-	
A 1	0.05	0.15	-	
A2	0.80	1.05	-	
b	0.19	0.30	-	
C	0.09	0.20		
D	6.40	6.60	6.50	
Е	6.20	6.60	6.40	
E1	4.30	4.50	4.40	
е	0.65 BSC			
٦	0.45	0.75	0.60	
L1	1.0 REF			
θ1	0°	8°	-	
θ2	10°	14°	12°	
θ3	10°	14°	12°	
All Dimensions in mm				

(2) QFN-20 (V-QFN4525-20)



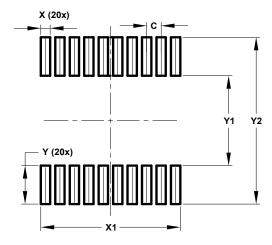
V-QFN4525-20				
Dim	Min	Max	Тур	
Α	0.75	0.85	0.80	
A1	0.00	0.05	0.02	
А3	-	-	0.15	
b	0.18	0.30	0.23	
D	4.45	4.55	4.50	
D2	2.85	3.15	3.00	
E	2.45	2.55	2.50	
E2	0.85	1.15	1.00	
е	0.50BSC			
L	0.30	0.50	0.40	
Z	-	-	0.385	
Z 1	-	-	0.885	
All Dimensions in mm				



Suggested Pad Layout

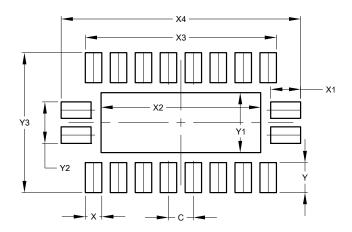
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) TSSOP-20



Dimensions	Value (in mm)
С	0.650
Х	0.420
X1	6.270
Υ	1.789
Y1	4.160
Y2	7.720

(2) QFN-20 (V-QFN4525-20)



Dimensions	Value (in mm)
С	0.500
X	0.330
X1	0.600
X2	3.200
Х3	3.830
X4	4.800
Υ	0.600
Y1	1.200
Y2	0.830
Y3	2.800



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