



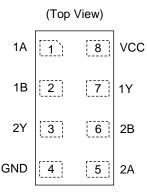
#### **DUAL 2-INPUT NAND GATE**

### **Description**

The 74LVC2G00 is a dual, two input NAND gate. Both gates have push-pull outputs designed for operation over a power supply range of 1.65V to 5.5V. The device is fully specified for partial power down applications using loff. The loff circuitry disables the output, preventing damaging current backflow when the device is powered down. Each gate performs the positive Boolean function:

$$Y = \overline{A \bullet B}$$
 or  $Y = \overline{A} + \overline{B}$ 

### **Pin Assignments**



X2-DFN2010-8 X2-DFN1410-8 X2-DFN1210-8

### **Features**

- Wide Supply Voltage Range from 1.65 to 5.5V
- ± 24mA Output Drive at 3.3V
- CMOS Low Power Consumption
- I<sub>OFF</sub> Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- Schmitt Trigger Action at all inputs makes the circuit tolerant for slower input rise and fall times. The hysteresis is typically 100mV at V<sub>CC</sub> = 3.0V.
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114)
  - Exceeds 1000-V Charged Device Model (C101)
- Latch-Up Exceeds 100mA per JESD 78, Class I
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

### **Applications**

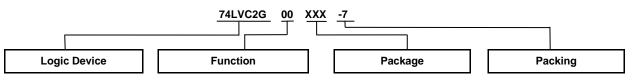
- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide Array of Products Such as:
  - PCs, Networking, Notebooks, Netbooks, PDAs
  - Tablet Computers, E-readers
  - Computer Peripherals, Hard Drives, CD/DVD ROMs
  - TVs, DVDs, DVRs, Set Top Boxes
  - Cell Phones, Personal Navigation / GPS
  - MP3 Players, Cameras, Video Recorders

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



# **Ordering Information** (Note 4)



74 : Logic Prefix LVC : 1.65V to 5.5V Logic Family 2-Input NAND Gate

00:

HD4 : X2-DFN2010-8 HK3 : X2-DFN1410-8 RA3 : X2-DFN1210-8 -7:7" Tape & Reel

2G : Dual Gate

	Package Package Package		7" Tape and Reel (Note 6)		
Device	Code	(Note 5)	Size	Quantity	Part Number Suffix
74LVC2G00HD4-7	HD4	X2-DFN2010-8	1.95mm x 1.0mm x 0.4mm 0.5 mm lead pitch	5,000/Tape & Reel	-7
74LVC2G00HK3-7	HK3	X2-DFN1410-8	1.35mm x 1.0mm x 0.35mm 0.4 mm lead pitch	5,000/Tape & Reel	-7
74LVC2G00RA3-7	RA3	X2-DFN1210-8	1.2mm x 1.0mm x 0.35mm 0.3 mm lead pitch	5,000/Tape & Reel	-7

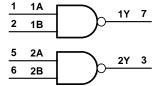
Notes: 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

- 5. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.
- 6. The taping orientation is located on our website at http://www.diodes.com/datasheets/ap02007.pdf.

# **Pin Descriptions**

Pin Name	Pin No.	Description
1A	1	Data Input
1B	2	Data Input
2Y	3	Data Output
GND	4	Ground
2A	5	Data Input
2B	6	Data Input
1Y	7	Data Output
Vcc	8	Supply Voltage

# **Logic Diagram**



# **Function Table**

Inp	Output	
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L



# Absolute Maximum Ratings (Notes 7 & 8)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
Vcc	Supply Voltage	-0.5 to +6.5	V
VI	Input Voltage	-0.5 to +6.5	V
Vo	Output Voltage -Active Mode	-0.5 to V <sub>CC</sub> +0.5	V
VO	Output Voltage Power Down Mode	-0.5 to +6.5	V
I <sub>IK</sub>	Input Clamp Current V <sub>I</sub> <0	-50	mA
lok	Output Clamp Current (Vo < 0 OR Vo > Vcc )	±50	mA
lo	Continuous Output Current (Vo = 0 to V <sub>CC</sub> )	±50	mA
Icc	Continuous Current Through V <sub>CC</sub>	100	mA
I <sub>GND</sub>	Continuous Current Through GND	-100	mA
TJ	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C

Notes:

# **Recommended Operating Conditions** (Note 9)

Symbol	Parameter		Min	Max	Unit
.,	On and the second	Operating	1.65	5.5	.,
V <sub>CC</sub>	Operating Voltage	Data Retention Only	1.5	_	V
VI	Input Voltage		0	5.5	V
	Output Voltage Active Mode		0	V <sub>CC</sub>	V
Vo	Output Voltage Power-Down Mode		0	5.5	]
	OH High-Level Output Current	V <sub>CC</sub> = 1.65V	_	-4	
		V <sub>CC</sub> = 2.3V	_	-8	
		V <sub>CC</sub> = 2.7V	_	-12	mA
I <sub>OH</sub>	Tright-Level Output Current	V 2.0V	_	-16	
		$V_{CC} = 3.0V$	_	-24	
		V <sub>CC</sub> = 4.5V	_	-32	
		V <sub>CC</sub> = 1.65V	_	4	
		V <sub>CC</sub> = 2.3V	_	8	]
I.e.	Low Lovel Output Current	V <sub>CC</sub> = 2.7V	_	12	mA
loL	Low-Level Output Current	V 2.0V	_	16	IIIA
		$V_{CC} = 3.0V$	_	24	
		V <sub>CC</sub> = 4.5V	_	32	
Δt/ΔV	Innut Transition Disc or Fall Data	V <sub>CC</sub> = 1.65V to 2.7V	_	20	20/1
ΔυΔν	Input Transition Rise or Fall Rate	V <sub>CC</sub> = 2.7V to 5.5V	_	10	ns/V
T <sub>A</sub>	Operating Fr	ee-Air Temperature	-40	+125	°C

Note: 9. Unused inputs should be held at  $V_{\text{CC}}$  or Ground.

<sup>7.</sup> Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device

operation should be within recommend values.

8. Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.



# **Electrical Characteristics** (All typical values are at T<sub>A</sub> = +25°C)

0	D	T1 0	Test Conditions		-40°C to +85°C			+125°C	
Symbol	Parameter	Test Conditions	V <sub>CC</sub>	Min	Тур.	Max	Min	Max	Uni
			$V_{CC} = 1.65V \text{ to } 1.95V$	0.65 x V <sub>CC</sub>		_	0.65 x V <sub>CC</sub>	_	
	High-Level		V <sub>CC</sub> = 2.3V to 2.7V	1.7	_	_	1.7	_	l
$V_{IH}$	Input Voltage	_	V <sub>CC</sub> = 2.7V to 3.6V	2.0	_	_	2.0	_	V
			V <sub>CC</sub> = 4.5V to 5.5V	0.7 x V <sub>CC</sub>	_	_	0.7 x V <sub>CC</sub>	_	
			$V_{CC} = 1.65V \text{ to } 1.95V$	_	-	0.35 x V <sub>CC</sub>	_	0.35 x V <sub>CC</sub>	
.,	Low-Level		V <sub>CC</sub> = 2.3V to 2.7V	_	_	0.7	_	0.7	١.,
$V_{IL}$	Input Voltage	_	V <sub>CC</sub> = 2.7V to 3.6V	_	_	0.8	_	0.8	V
			V <sub>CC</sub> = 4.5V to 5.5V	_	_	0.3 x V <sub>CC</sub>	_	0.3 x V <sub>CC</sub>	
		I <sub>OH</sub> = -100μA	1.65V to 5.5V	V <sub>CC</sub> – 0.1	Vcc	_	V <sub>CC</sub> – 0.1	_	
		I <sub>OH</sub> = -4mA	1.65V	1.2	1.53	_	0.95	_	
	High-Level	I <sub>OH</sub> = -8mA	2.3V	1.9	2.13	_	1.7	_	
VoH	Output	I <sub>OH</sub> = -12mA	2.7	2.2	2.5	_	1.9	_	٧
	Voltage	I <sub>OH</sub> = -16mA	2) /	2.4	2.7	_	2.2	_	
		I <sub>OH</sub> = -24mA	3V	2.3	2.6	_	2.0	_	
		$I_{OH} = -32mA$	4.5V	3.8	4.1	_	3.4	_	
		I <sub>OL</sub> = 100μA	1.65V to 5.5V	_	0	0.1	_	0.1	
		$I_{OL} = 4mA$	1.65V	_	0.08	0.45	_	0.7	
	Low-Level	$I_{OL} = 8mA$	2.3V	_	0.14	0.3	_	0.45	1
$V_{OL}$	Output	$I_{OL} = 12mA$	2.7V	_	0.19	0.4	1	0.6	V
	Voltage	$I_{OL} = 16mA$	0)/	_	0.25	0.4	1	0.6	
		$I_{OL} = 24mA$	3V	_	0.37	0.55	_	0.8	
		$I_{OL} = 32mA$	4.5V	_	0.43	0.55	_	0.8	
II	Input Current	V <sub>I</sub> = 5.5V or GND	0V to 5.5V	_	± 0.1	±5	_	± 20	μΑ
I <sub>OFF</sub>	Power Down Leakage Current	$V_1$ or $V_0 = 5.5V$	0V	_	± 0.1	±10	_	±20	μA
I <sub>CC</sub>	Supply Current	$V_I = 5.5V$ or GND $I_O=0A$	1.65V to 5.5V	_	0.1	10	_	40	μA
ΔI <sub>CC</sub>	Additional Supply Current	One input at $V_{CC} - 0.6V$ Other inputs at $V_{CC}$ or GND	2.3V to 5.5V	_	5	500	_	5,000	μА
Cı	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V	_	2.5	_	_	_	pF



# **Operating Characteristics**

	Parameter	Test Conditions	V <sub>CC</sub> = 1.8V Typ.	V <sub>CC</sub> = 2.5V Typ.	V <sub>CC</sub> = 3.3V Typ.	V <sub>CC</sub> = 5V Typ.	Unit
C <sub>pd</sub>	Power Dissipation Capacitance	f = 10MHz	19	19	20	22	pF

# Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Тур.	Max	Unit
	θ <sub>JA</sub> Thermal Resistance Junction-to-Ambient	X2-DFN2010-8		-	313	-	
$\theta_{JA}$		X2-DFN1410-8	(Note 10)	_	321	_	°C/W
		X2-DFN1210-8		_	395	_	
	- 15 1	X2-DFN2010-8	(Note 10)	_	145	_	
$\theta_{JC}$	Thermal Resistance Junction-	X2-DFN1410-8		_	166	_	°C/W
	to-Case	X2-DFN1210-8		-	236	_	

Note: 10. Test condition for each package type: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

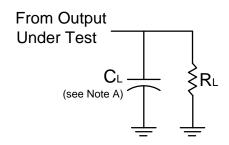
# **Switching Characteristics**

Typical Values at  $T_A = +25$ °C and nominal voltages 1.8V, 2.5V, 2.7V, 3.3V, and 5.0V. See Figure 1.

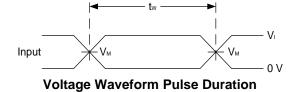
D 1	From To		V	T <sub>A</sub>	= -40°C to +85	5°C	T <sub>A</sub> = -40°C	to +125°C	1124	
Parameter	Input	Output	Vcc	Min	Тур	Max	Min	Max	Unit	
				1.8V ± 0.15V	1.2	3.5	8.6	1.2	10.8	
			$2.5V \pm 0.2V$	0.7	2.3	4.8	0.7	6.0		
t <sub>pd</sub>	A or B Y	Y	2.7V	0.7	3.0	5.6	0.7	7.0	ns	
			$3.3V \pm 0.3V$	0.7	2.2	4.3	0.7	5.4		
			5.0V ± 0.5V	0.5	1.8	3.3	0.5	4.2		

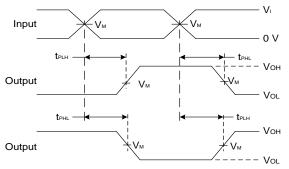


### **Parameter Measurement Information**



V	/cc Inputs V <sub>M</sub>		C <sub>L</sub>	R <sub>L</sub>		
V <sub>cc</sub>	Vı	t <sub>r</sub> /t <sub>f</sub>	<b>™</b>	O <sub>L</sub>	KL.	
1.8V ± 0.15V	V <sub>cc</sub>	≤2ns	V <sub>CC</sub> /2	30pF	1kΩ	
2.5V ± 0.2V	Vcc	≤2ns	V <sub>CC</sub> /2	30pF	500Ω	
2.7V	2.7V	≤2.5ns	1.5V	50pF	500Ω	
3.3V ± 0.3V	2.7V	≤2.5ns	1.5V	50pF	500Ω	
5.0V ± 0.5V	V <sub>CC</sub>	≤2.5ns	V <sub>CC</sub> /2	50pF	500Ω	





**Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs** 

Figure 1. Load Circuit and Voltage Waveforms

Notes:

A. Includes test lead and test apparatus capacitance.B. All pulses are supplied at pulse repetition rate ≤ 10MHz.

C. Inputs are measured separately one transition per measurement.

D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .



# **Marking Information**

(Top View)

<u>XX</u> 

XX: Identification Code
Y: Year: 0~9
W: Week: A~Z: 1~26 week;
a~z: 27~52 week; z represents
52 and 53 week

X: Internal Code

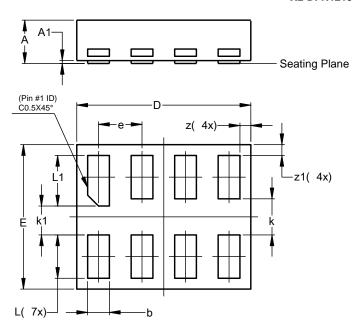
Part Number	Package	Identification Code
74LVC2G00HD4-7	X2-DFN2010-8	4T
74LVC2G00HK3-7	X2-DFN1410-8	4U
74LVC2G00RA3-7	X2-DFN1210-8	4V



# X2-DFN1210-8 Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### X2-DFN1210-8

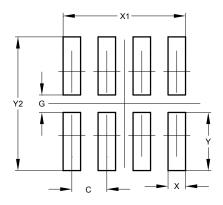


	X2-DFN1210-8								
Dim	Min	Max	Тур						
Α	-	0.35	0.30						
A1	0	0.03	0.02						
b	0.10	0.20	0.15						
D	1.15	1.25	1.20						
Е	0.95	1.05	1.00						
е	-	-	0.30						
k	-	-	0.25						
k1	-	-	0.20						
L	0.25	0.35	0.30						
L1	0.30	0.40	0.35						
Z	0.050	0.100	0.075						
z1	0.050	0.100	0.075						
All I	Dimens	ions in	mm						

### **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X2-DFN1210-8



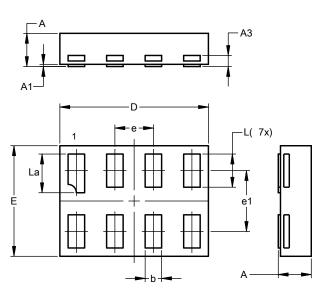
Dimensions	Value (in mm)
С	0.300
G	0.150
Х	0.150
X1	1.050
Y	0.500
Y1	1.150



# X2-DFN1410-8 Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### X2-DFN1410-8

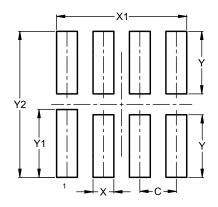


X2-DFN1410-8				
Dim	Min	Max	Тур	
Α	0.30	0.35	0.33	
A1	0.00	0.03	0.02	
А3			0.10	
b	0.12	0.20	0.15	
D	1.30	1.40	1.35	
Е	0.95	1.05	1.00	
е			0.35	
e1			0.55	
L	0.27	0.35	0.30	
L1	0.32	0.40	0.35	
All Dimensions in mm				

# **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X2-DFN1410-8



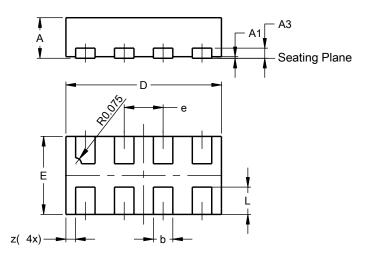
Dimensions	Value (in mm)
С	0.350
Х	0.200
X1	1.250
Υ	0.600
Y1	0.650
Y2	1.400



# X2-DFN2010-8 Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### X2-DFN2010-8

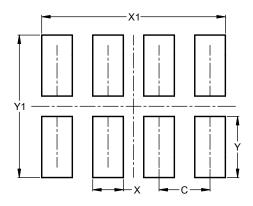


X2-DFN2010-8				
Dim	Min	Max	Тур	
Α		0.40		
A1	0.00	0.05	0.02	
A3			0.13	
b	0.20	0.30	0.25	
D	1.950	2.05	2.00	
Е	0.95	1.05	1.00	
е			0.50	
Ĺ	0.30	0.40	0.35	
Z			0.125	
All Dimensions in mm				

# Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X2-DFN2010-8



Dimensions	Value (in mm)
С	0.500
X	0.300
X1	1.800
Y	0.600
Y1	1.400



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