

DATA SHEET

74LVC841A

10-bit transparent latch with 5-volt
tolerant inputs/outputs (3-State)

Product specification
IC24 Data Handbook

1998 Jun 17

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1 A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC841A is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-State operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment. The 74LVC841A is a 10-bit transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all internal latches. The 74LVC841A consists of ten transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the ten latches are available at the outputs.

When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n ; LE to Q_n	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	4.5 5.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	$V_I = \text{GND to } V_{CC}^1$	22	pF

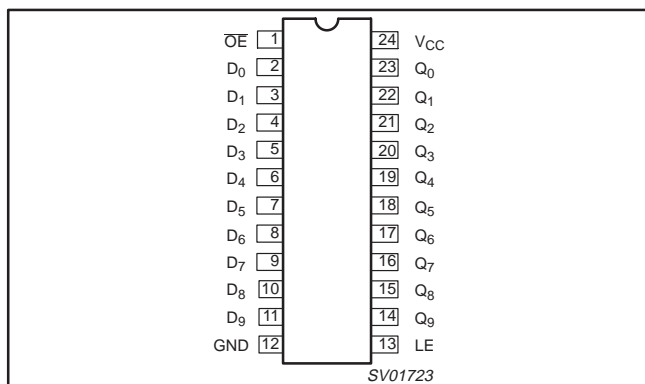
NOTE:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	-40°C to +125°C	74LVC841A D	74LVC841A D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +125°C	74LVC841A DB	74LVC841A DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +125°C	74LVC841A PW	7LVC841APW DH	SOT355-1

PIN CONFIGURATION



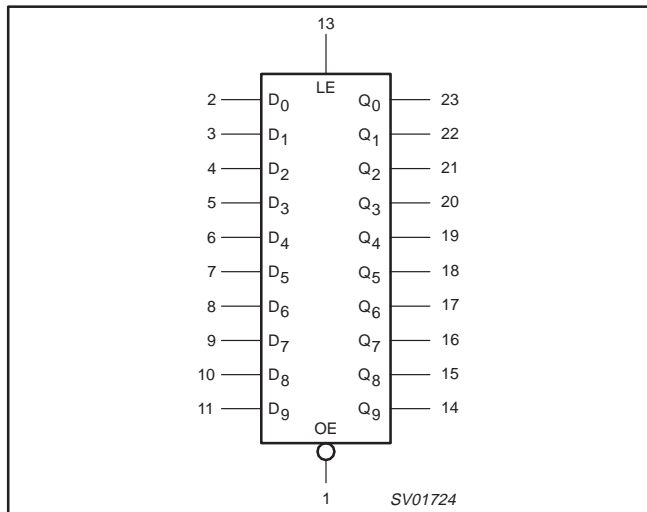
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	Output enable input (active Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D_0 to D_9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q_0 to Q_9	3-state latch outputs
12	GND	Ground (0 V)
13	LE	Latch enable input (active HIGH)
24	V_{CC}	Positive supply voltage

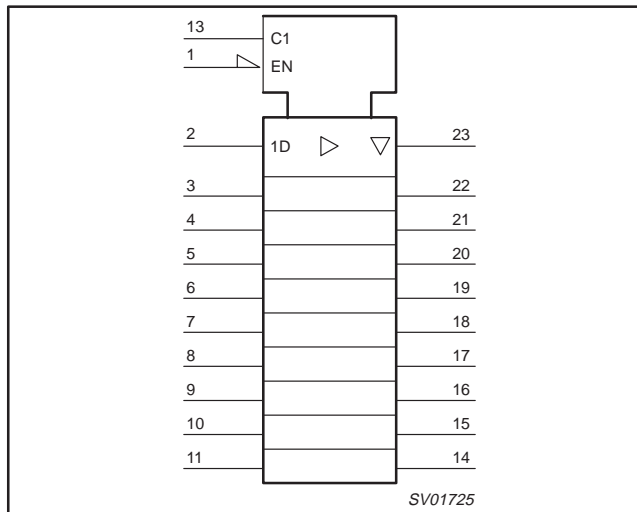
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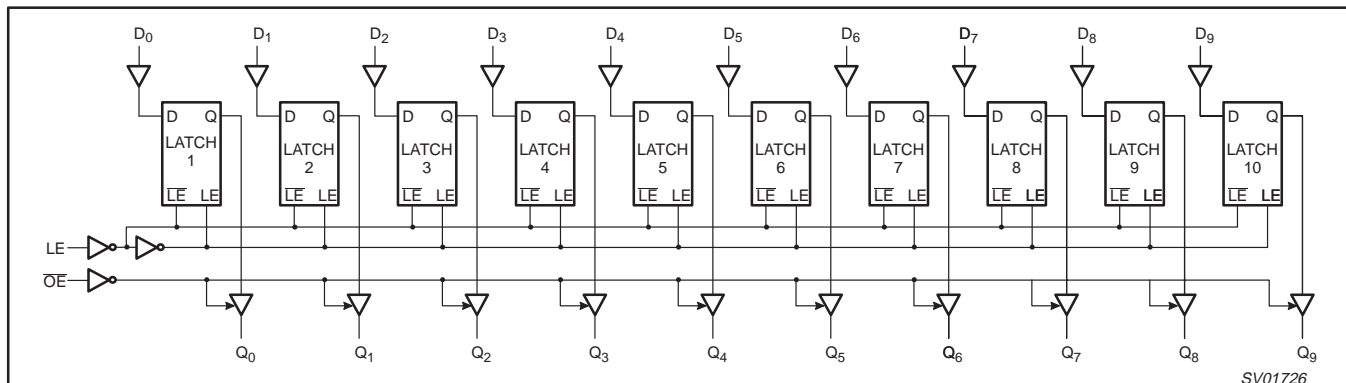
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE for register A_n or B_n

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	\overline{OE}	LE	D _n		Q ₀ TO Q ₉
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
latch register and disable outputs	H H	X X	l h	L H	Z Z
Hold	L	L	X	NC	NC

NOTES:

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
- X = don't care
- Z = high impedance OFF-state
- NC = no change

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V _I	DC input voltage range		0	5.5	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.2 to 2.7V V _{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +6.5	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage	Note 2	-0.5 to +5.5	V
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0	± 50	mA
V _O	DC output voltage	Note 2	-0.5 to V _{CC} +0.5	V
I _O	DC output source or sink current	V _O = 0 to V _{CC}	± 50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		± 100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package			
	- plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 1.0			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		±0.1	±5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	±5	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTE:

1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = -40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V		
			MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} /t _{PLH}	Propagation delay D _n to Q _n	Figures 1, 5	1.5	4.5	6.7	1.5	7.5	ns
t _{PHL} /t _{PLH}	Propagation delay LE to Q _n	Figures 2, 5	1.5	4.9	7.6	1.5	8.6	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	Figures 3, 5	1.5	5.4	7.9	1.5	8.9	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	Figures 3, 5	1.5	3.8	5.9	1.5	6.9	ns
t _w	LE pulse width, HIGH	Figure 4	2.0	0.7	–	2.0		ns
t _{su}	Set-up time D _n to LE	Figure 4	2.0	0.5	–	2.0		ns
t _h	Hold time D _n to LE	Figure 4	1.0	-0.5	–	1.0		ns

NOTE:

1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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AC WAVEFORMS

$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_M = 0.5\text{ V} \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 $V_M = 1.5\text{ V}$ at $V_{CC} = 3.0\text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 $V_Y = V_{OH} - 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$

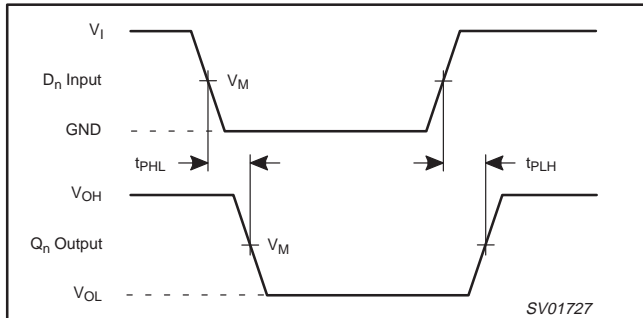


Figure 1. Input (D_n) to output (Q_n) propagation delays.

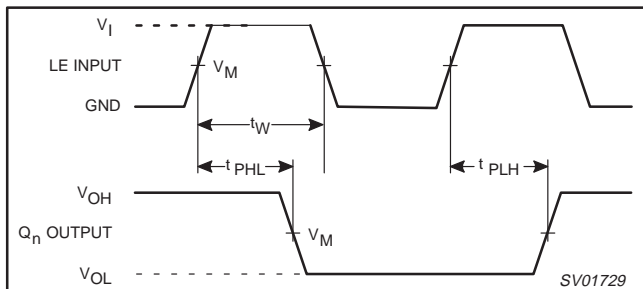


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

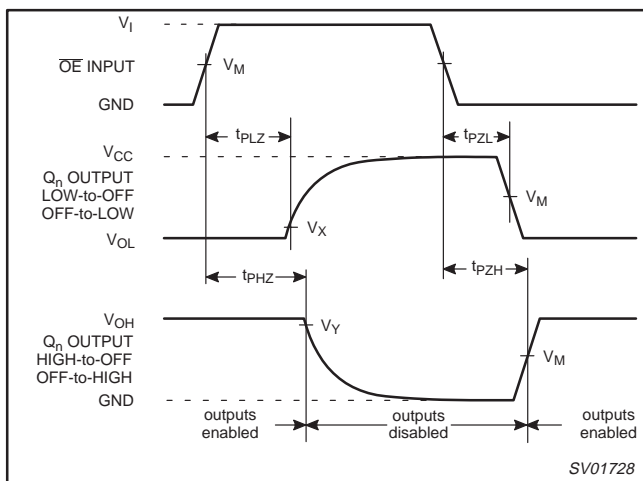


Figure 3. 3-State enable and disable times.

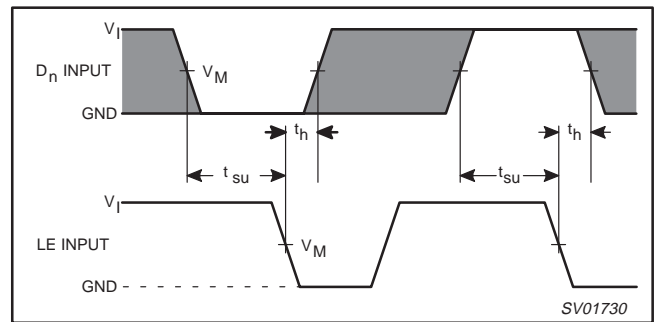


Figure 4. Data set-up and hold times for the D_n input to LE input.

Note to Figure 4: The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT

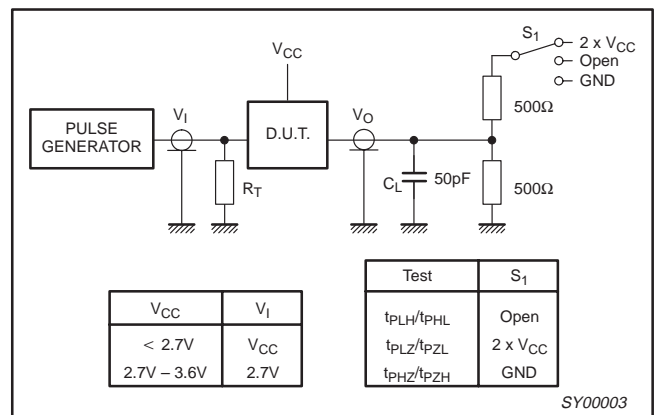


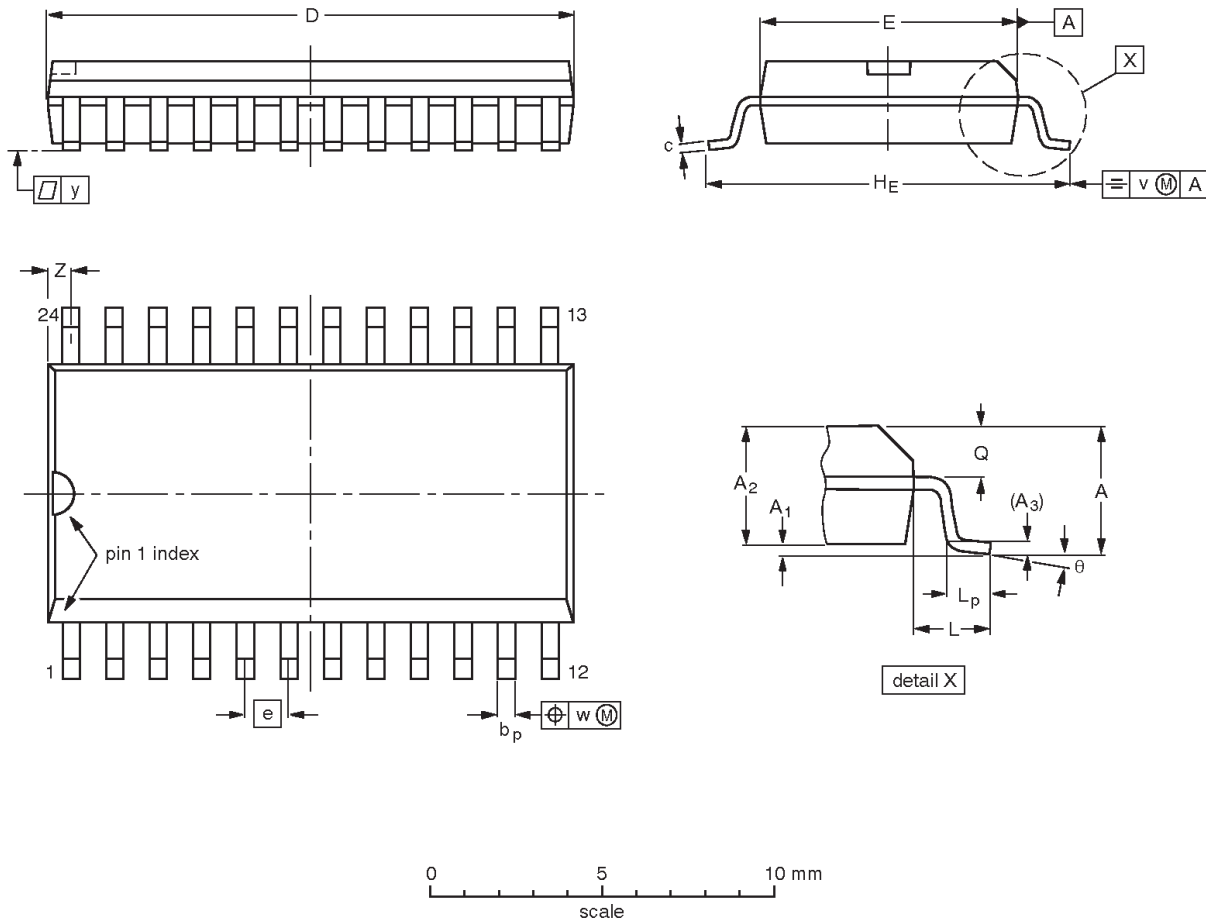
Figure 5. Load circuitry for switching times.

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

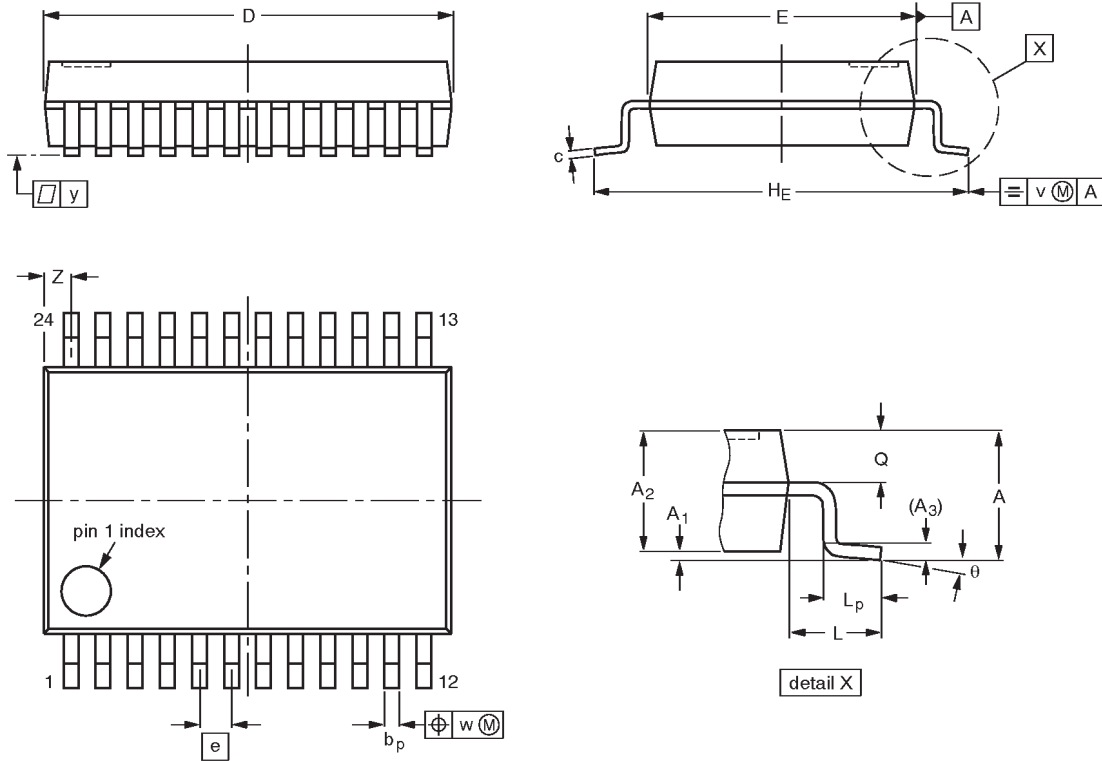
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

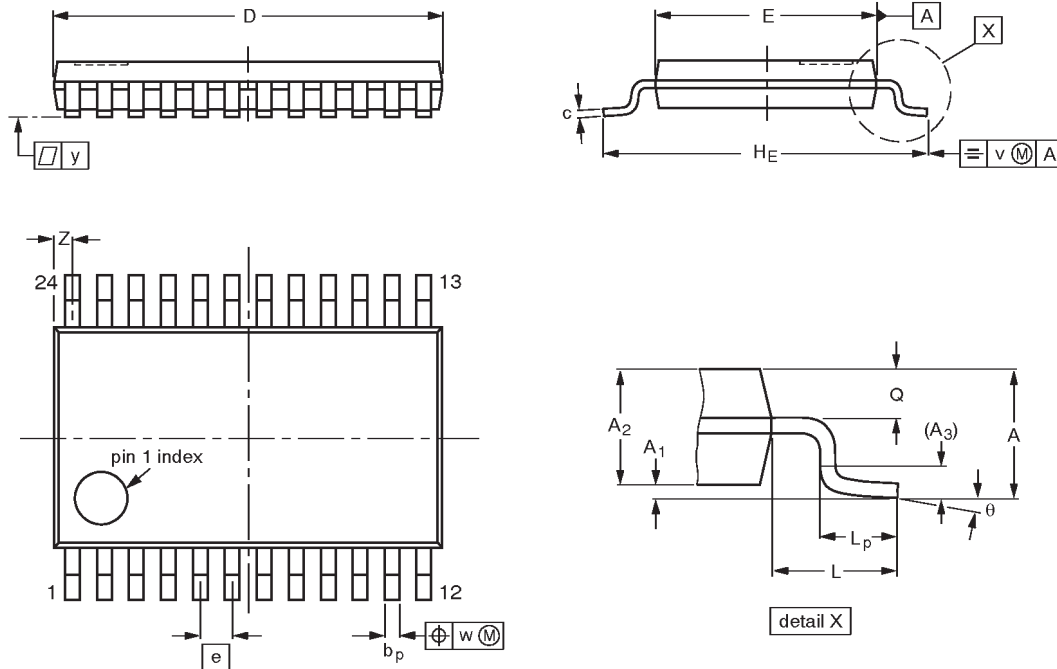
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				-93-06-16 95-02-04

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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