# 74LVT02

## 3.3 V Quad 2-input NOR gate

Rev. 3 — 7 April 2017 Product data sheet

## 1 General description

The 74LVT02 is a high-performance BiCMOS product designed for $V_{CC}$ operation at 3.3 V.

The 74LVT02 is a quad 2-input NOR gate.

## 2 Features and benefits

- Wide supply voltage range from 2.7 V to 3.6 V
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Latch-up protection
  - JESD78 Class II exceeds 500 mA
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

## 3 Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVT02D | -40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVT02DB | -40 °C to +85 °C | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74LVT02PW | -40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

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# 4 Functional diagram

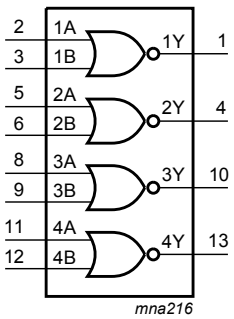



Figure 1. Logic symbol

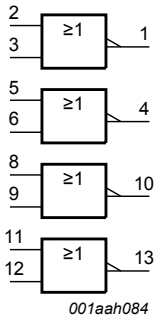



Figure 2. IEC logic symbol

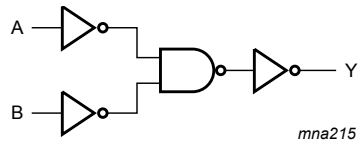



Figure 3. Logic diagram (one gate)

# 5 Pinning information

## 5.1 Pinning

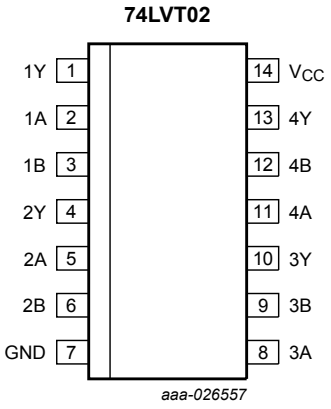



Figure 4. Pin configuration for SOT108-1 (SO14)

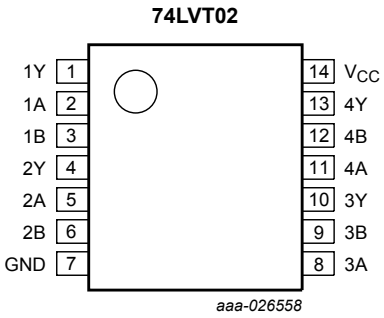



Figure 5. Pin configuration for SOT337-1 and SOT402-1 (SSOP14 and TSSOP14)

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| 1Y to 4Y | 1, 4, 10, 13 | data output |
| 1A to 4A | 2, 5, 8, 11 | data input |
| 1B to 4B | 3, 6, 9,12 | data input |
| GND | 7 | ground (0 V) |
| $V_{CC}$ | 14 | supply voltage |

# 6 Functional description

**Table 3. Function table [1]**

| Input | | Output |
|---|---|---|
| nA | nB | nY |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

[1] H = HIGH voltage level; L = LOW voltage level

# 7 Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +4.6 | V |
| $V_I$ | input voltage | | [1] | -0.5 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state | [1] | -0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | -50 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | -50 | - | mA |
| $I_O$ | output current | output in LOW-state | | - | 64 | mA |
| | | output in HIGH-state | | -32 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $T_j$ | junction temperature | | [2] | - | 150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 to +85 °C | [3] | - | 500 | mW |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

# 8 Recommended operating conditions

**Table 5. Operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.7 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $I_{OH}$ | HIGH-level output current | | -20 | - | - | mA |
| $I_{OL}$ | LOW-level output current | | - | - | 32 | mA |
| $T_{amb}$ | ambient temperature | in free-air | -40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

# 9 Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{amb}$ = -40 °C to +85 °C | | | | | | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 2.7 V; $I_{IK}$ = -18 mA | -1.2 | | - | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = 2.7 V to 3.6 V; $I_{OH}$ = -100 µA | $V_{CC}$ - 0.2 | | - | V |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = -6 mA | 2.4 | - | - | V |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = -20 mA | 2.0 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 2.7 V; $I_{OL}$ = 100 µA | - | | 0.2 | V |
| | | $V_{CC}$ = 2.7 V; $I_{OL}$ = 24 mA | - | | 0.5 | V |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 32 mA | - | | 0.5 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 0 V or 3.6 V; $V_I$ = 5.5 V | - | - | 10 | µA |
| | | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | | - | ±1 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | | | ±100 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | |
| | | output HIGH | - | - | 0.02 | mA |
| | | output LOW | - | 1 | 2 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3.0 V to 3.6 V; one input at $V_{CC}$ - 0.6 V and other inputs at $V_{CC}$ or GND [2] | - | | 0.2 | µA |
| $C_I$ | input capacitance | $V_I$ = 0 V or 3.0 V | - | 3 | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 3.3 V.

[2] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

# 10 Dynamic characteristics

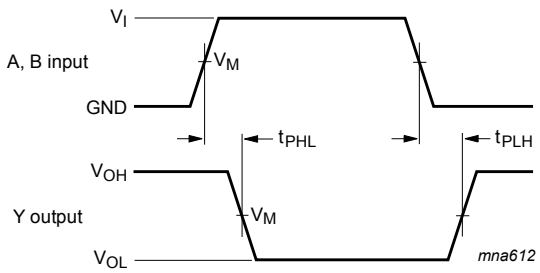
**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{amb}$ = -40 °C to +85 °C | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | nA or nB to nY; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 5.2 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1 | 2.8 | 4.4 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | nA or nB to nY; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 3.4 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1 | 2.6 | 3.6 | ns |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 3.3 V.

## 10.1 Waveforms and test circuit



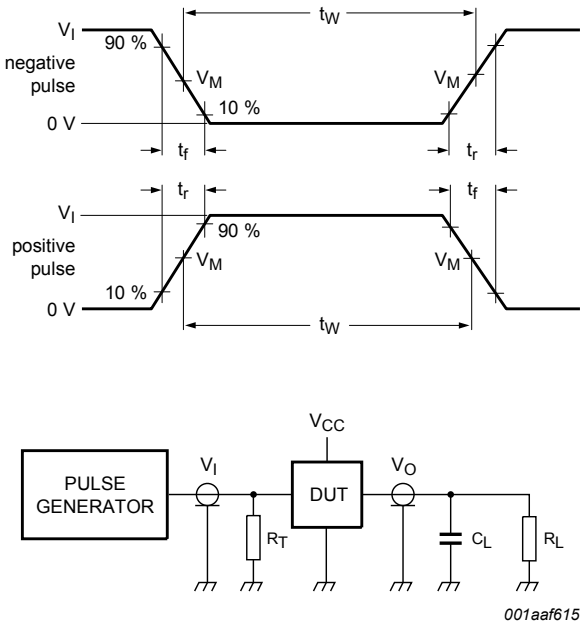

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Figure 6. Input to output propagation delays**

**Table 8. Measurement points**

| Input | | Output |
|---|---|---|
| $V_M$ | $V_I$ | $V_M$ |
| 1.5 V | 2.7 V | 1.5 V |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = load capacitance including jig and probe capacitance.

$R_L$ = load resistance.

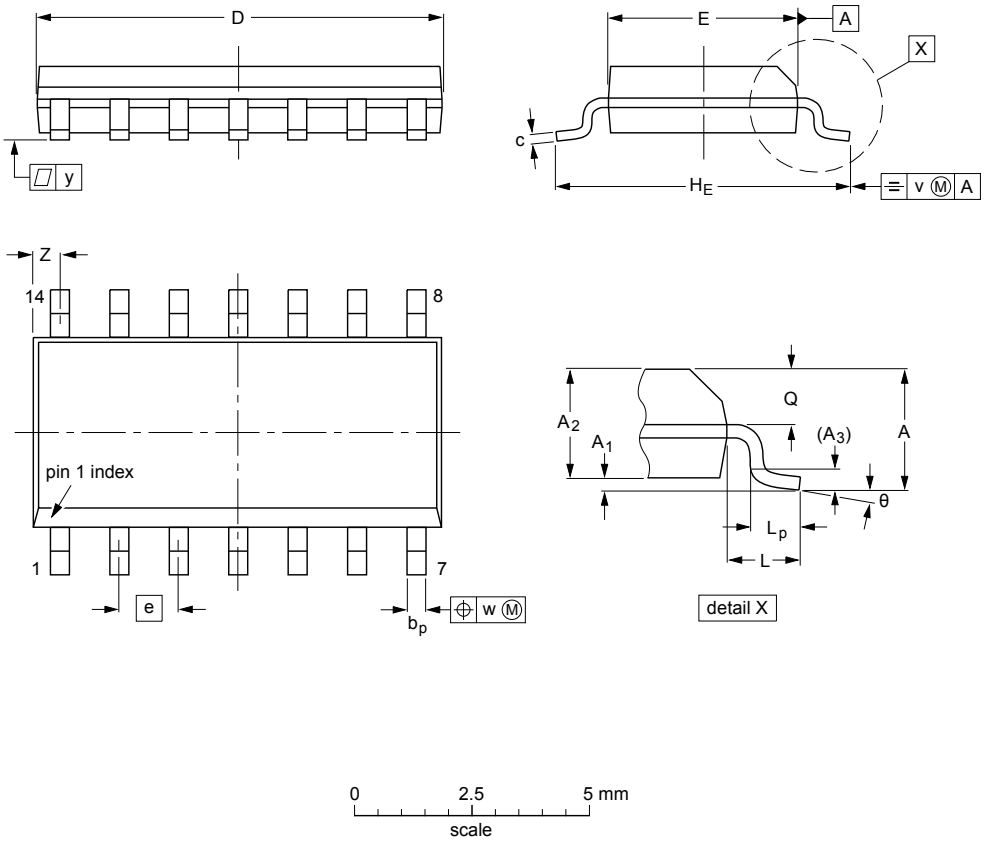
**Figure 7. Test circuit for measuring switching times**

**Table 9. Test data**

| Input | | | | Load | | Test |
|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | $t_{PLH}$, $t_{PHL}$ |

# 11 Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

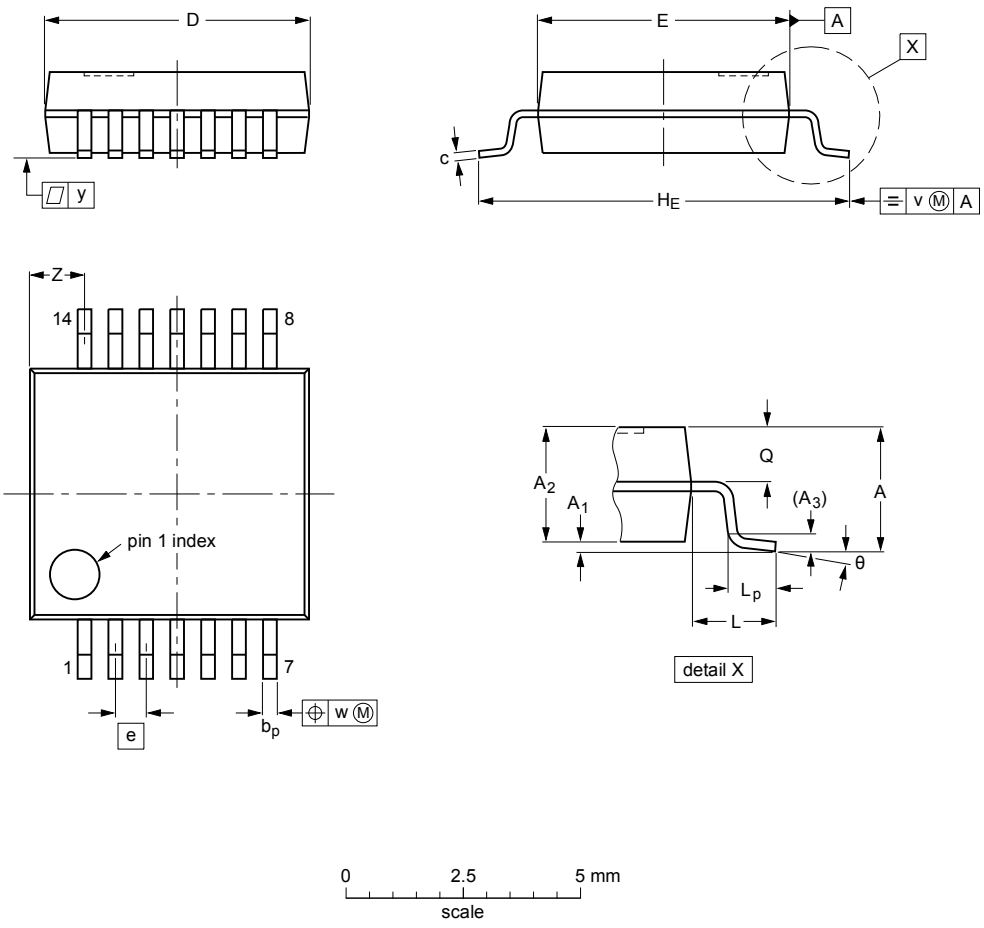
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Figure 8. Package outline SOT108-1 (SO14)**

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm** **SOT337-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.4<br>0.9 | $8^o$<br>$0^o$ |

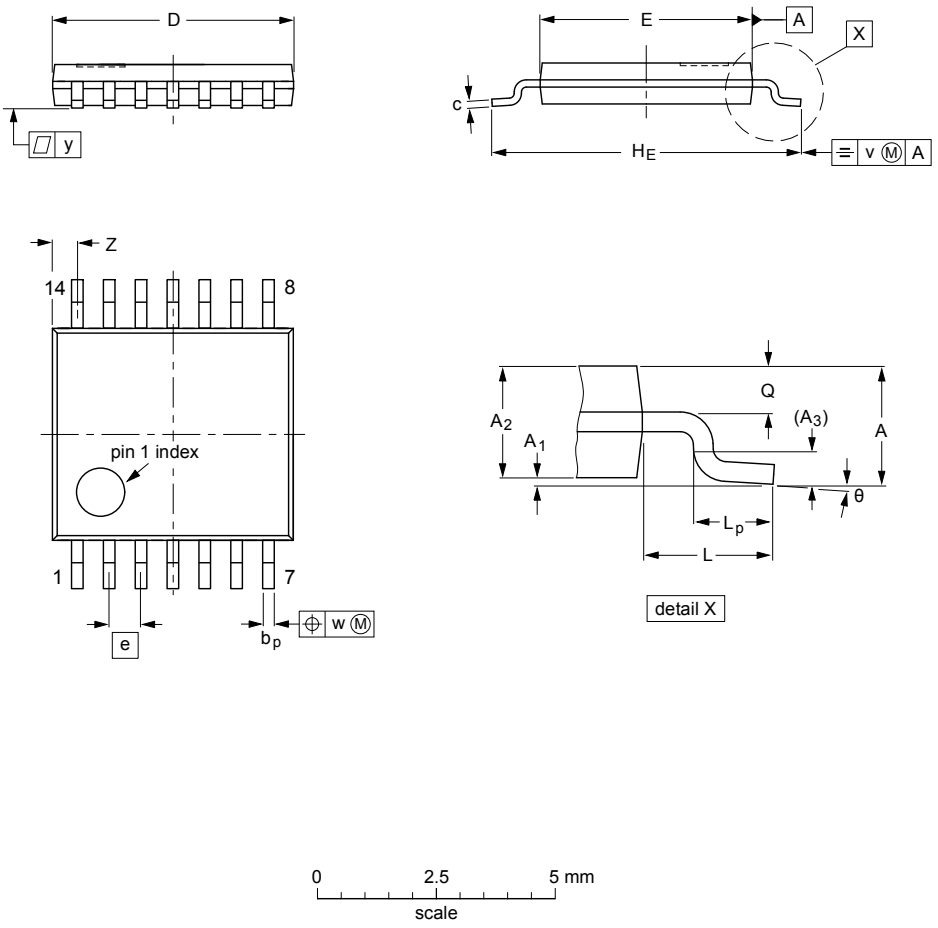
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT337-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Figure 9. Package outline SOT337-1 (SSOP14)**

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Figure 10. Package outline SOT402-1 (TSSOP14)**

## 12 Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 13 Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVT02 v.3 | 20170324 | Product data sheet | - | 74LVT02 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LVT02 v.2 | 19960815 | Product specification | - | 74LVT02 v.1 |

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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