# 74LVT125; 74LVTH125

## 3.3 V quad buffer; 3-state

Rev. 7 — 31 May 2016 Product data sheet

## 1. General description

The 74LVT125; 74LVTH125 is a high-performance BiCMOS product designed for $V_{CC}$ operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT125; 74LVTH125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$ and $4\overline{OE}$), each controlling one of the 3-state outputs.

## 2. Features and benefits

- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and −32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVT125D | –40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVTH125D | | | | |
| 74LVT125DB | –40 °C to +85 °C | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74LVTH125DB | | | | |
| 74LVT125PW | –40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74LVTH125PW | | | | |
| 74LVT125BQ | –40 °C to +85 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74LVTH125BQ | | | | |

## 4. Functional diagram

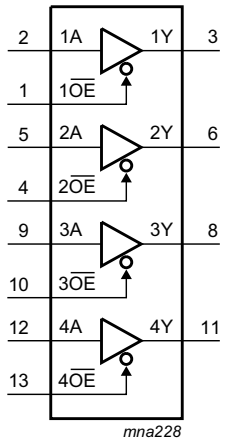



**Fig 1. Logic symbol**

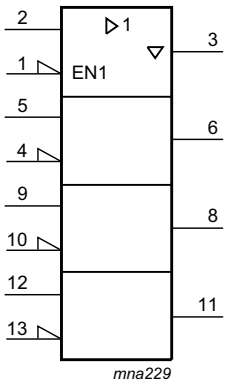



**Fig 2. IEC logic symbol**

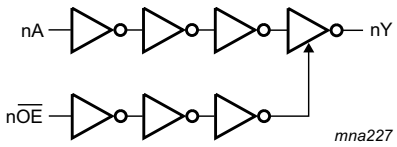



**Fig 3. Logic diagram (one buffer)**

# 5. Pinning information

## 5.1 Pinning

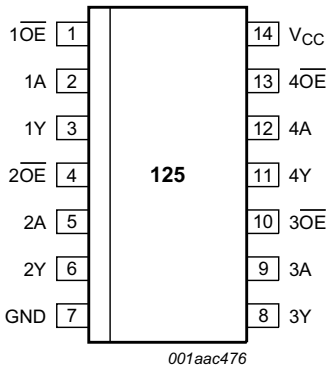
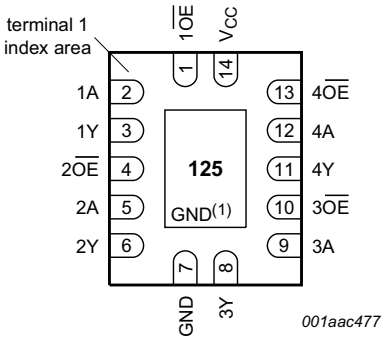



Fig 4. Pin configuration SO14, SSOP14 and TSSOP14




Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| $1\overline{OE}$ | 1 | 1 output enable input (active LOW) |
| 1A | 2 | 1 data input |
| 1Y | 3 | 1 data output |
| $2\overline{OE}$ | 4 | 2 output enable input (active LOW) |
| 2A | 5 | 2 data input |
| 2Y | 6 | 2 data output |
| GND | 7 | ground (0 V) |
| 3Y | 8 | 3 data output |
| 3A | 9 | 3 data input |
| $3\overline{OE}$ | 10 | 3 output enable input (active LOW) |
| 4Y | 11 | 4 data output |
| 4A | 12 | 4 data input |
| $4\overline{OE}$ | 13 | 4 output enable input (active LOW) |
| $V_{CC}$ | 14 | supply voltage |

# 6. Functional description

## 6.1 Function table

**Table 3. Function table[1]**

| Control | Input | Output |
|---|---|---|
| $\overline{nOE}$ | nA | nY |
| L | L | L |
| L | H | H |
| H | X | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.5 | +4.6 | V |
| $V_I$ | input voltage | [1] | –0.5 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state [1] | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | - | –50 | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | - | –50 | mA |
| $I_O$ | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | - | –64 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | [2] | - | 150 | °C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.7 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.8 | V |
| $I_{OH}$ | HIGH-level output current | | - | - | –32 | mA |
| $I_{OL}$ | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle ≤ 50 %; f ≥ 1 kHz | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | 0 | - | 10 | ns/V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +85 | °C |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = –40 °C to +85 °C** [1] | | | | | | |
| $V_{IK}$ | input clamping voltage | $I_{IK}$ = –18 mA; $V_{CC}$ = 2.7 V | - | –0.9 | –1.2 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –100 μA; $V_{CC}$ = 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | $V_{CC}$ – 0.1 | - | V |
| | | $I_{OH}$ = –8 mA; $V_{CC}$ = 2.7 V | 2.4 | 2.5 | - | V |
| | | $I_{OH}$ = –32 mA; $V_{CC}$ = 3.0 V | 2.0 | 2.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 2.7 V | | | | |
| | | $I_{OL}$ = 100 μA | - | 0.1 | 0.2 | V |
| | | $I_{OL}$ = 24 mA | - | 0.3 | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | | | | |
| | | $I_{OL}$ = 16 mA | - | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 32 mA | - | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 64 mA | - | 0.4 | 0.55 | V |
| $I_I$ | input leakage current | all input pins | | | | |
| | | $V_{CC}$ = 0 V or 3.6 V; $V_I$ = 5.5 V | - | 1 | 10 | μA |
| | | control pins | | | | |
| | | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | - | ±0.1 | ±1 | μA |
| | | data pins [2] | | | | |
| | | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ | - | 0.1 | 1 | μA |
| | | $V_{CC}$ = 3.6 V; $V_I$ = 0 V | - | –1 | –5 | μA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | - | 1 | ±100 | μA |
| $I_{BHL}$ | bus hold LOW current | $V_{CC}$ = 3 V; $V_I$ = 0.8 V [3] | 75 | 150 | - | μA |
| $I_{BHH}$ | bus hold HIGH current | $V_{CC}$ = 3 V; $V_I$ = 2.0 V | - | –150 | –75 | μA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_{CC}$ = 3.6 V; $V_I$ = 0 V to 3.6 V | 500 | - | - | μA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_{CC}$ = 3.6 V; $V_I$ = 0 V to 3.6 V | - | - | –500 | μA |
| $I_{LO}$ | output leakage current | output in HIGH-state when $V_O$ > $V_{CC}$; $V_O$ = 5.5 V; $V_{CC}$ = 3.0 V | - | 60 | 125 | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC}$ ≤ 1.2 V; $V_O$ = 0.5 V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; $\overline{nOE}$ = don't care [4] | - | ±1 | ±100 | μA |
| $I_{OZ}$ | OFF-state output current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | output HIGH: $V_O$ = 3.0 V | - | 1 | 5 | μA |
| | | output LOW: $V_O$ = 0.5 V | - | –1 | –5 | μA |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | |
| | | outputs HIGH | - | 0.13 | 0.19 | mA |
| | | outputs LOW | - | 2 | 7 | mA |
| | | outputs disabled [5] | - | 0.13 | 0.19 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3 V to 3.6 V; one input at $V_{CC}$ − 0.6 V and other inputs at $V_{CC}$ or GND [6] | - | 0.1 | 0.2 | mA |
| $C_I$ | input capacitance | $V_I$ = 0 V or 3.0 V | - | 4 | - | pF |
| $C_O$ | output capacitance | outputs disabled; $V_O$ = 0 V or 3.0 V | - | 8 | - | pF |

[1] Typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

[2] Unused pins at $V_{CC}$ or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any $V_{CC}$ between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC}$ = 1.2 V to $V_{CC}$ = 3.0 V to 3.6 V a transition time of 100 µs is permitted. This parameter is valid for $T_{amb}$ = 25 °C only.

[5] $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = –40 °C to +85 °C [1]** | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | nAn to nY; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 4.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.7 | 4.0 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | nAn to nY; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 4.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.9 | 3.9 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $n\overline{OE}$ to nY; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 6.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.4 | 4.7 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | $n\overline{OE}$ to nY; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 6.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.1 | 3.4 | 4.7 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $n\overline{OE}$ to nY; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 5.7 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.8 | 3.7 | 5.1 | ns |

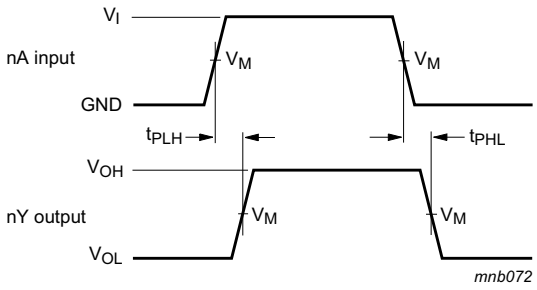
**Table 7. Dynamic characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLZ}$ | LOW to OFF-state propagation delay | $n\overline{OE}$ to nY; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 4.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.3 | 2.6 | 4.5 | ns |

[1] Typical values are at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

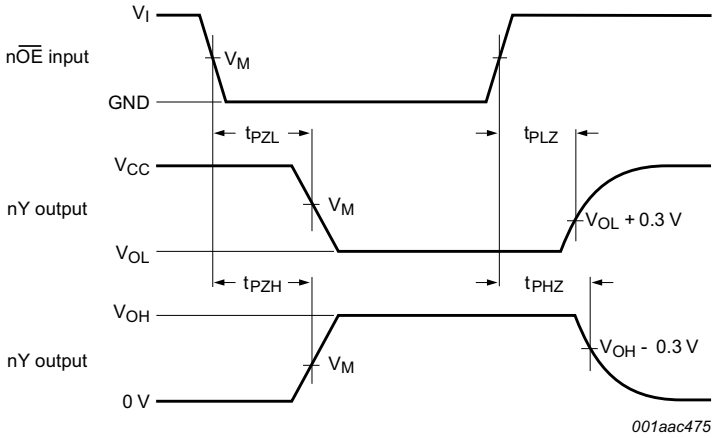
## 11. Waveforms




$V_M$ = 1.5 V.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

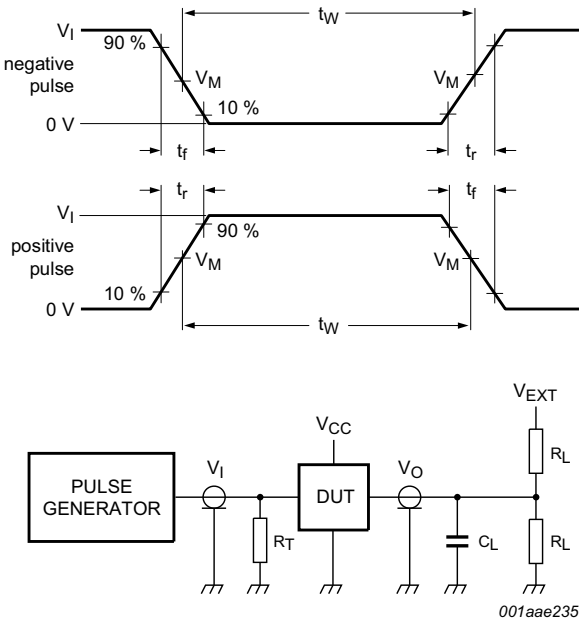
**Fig 6. Propagation delay input (nA) to output (nY)**




$V_M$ = 1.5 V.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times of 3-state outputs**




Test data is given in Table 8.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = Test voltage for switching times.

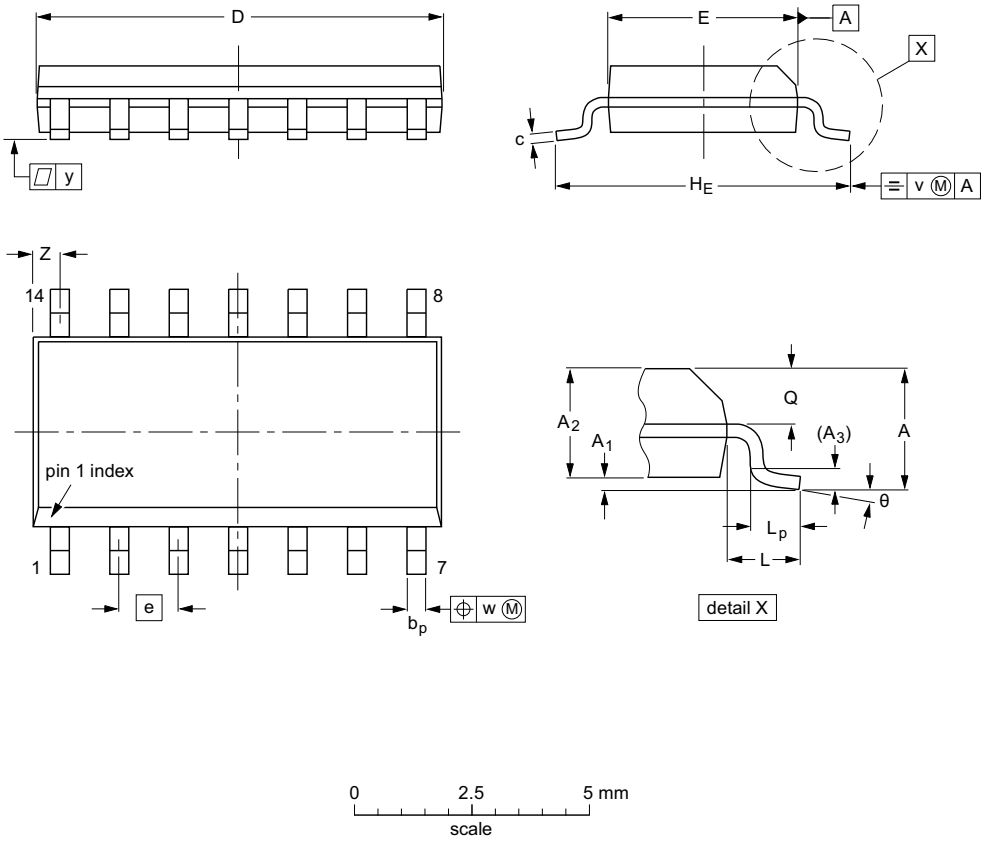
**Fig 8. Test circuit for measuring switching times**

**Table 8. Test data**

| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

## 12. Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

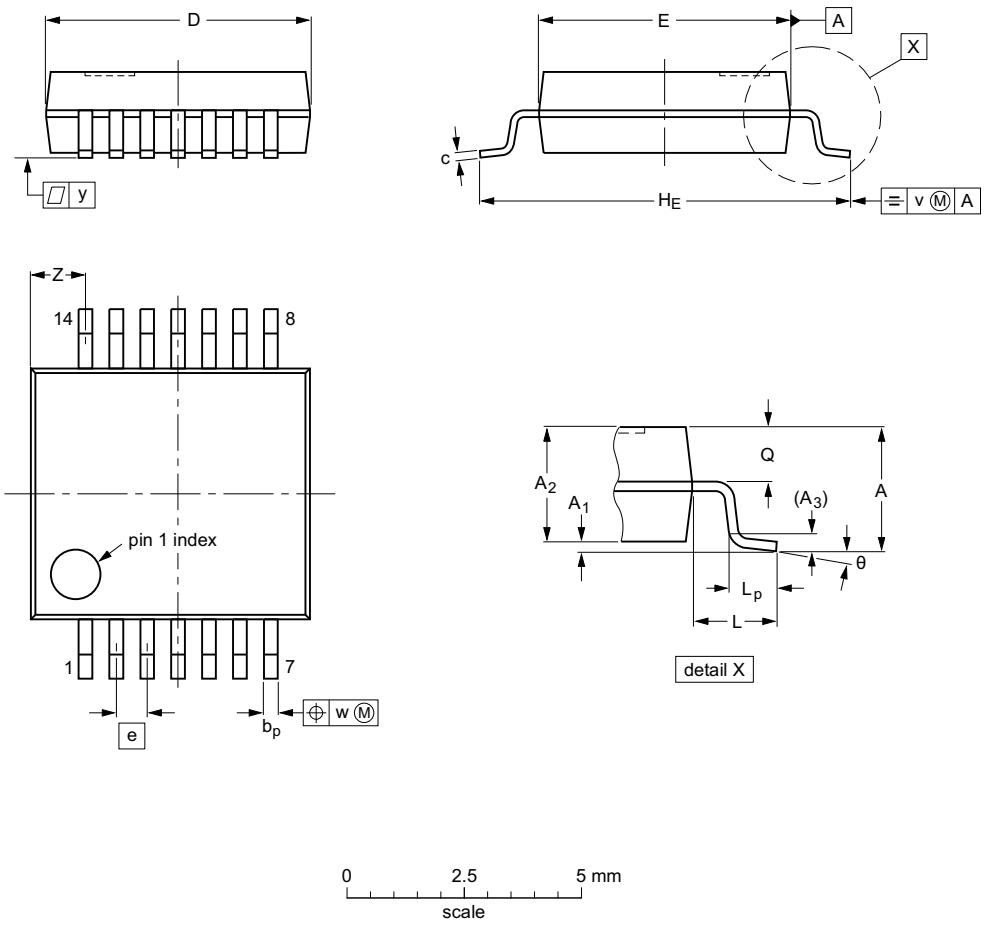
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT108-1 (SO14)**

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm** **SOT337-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.4<br>0.9 | $8^o$<br>$0^o$ |

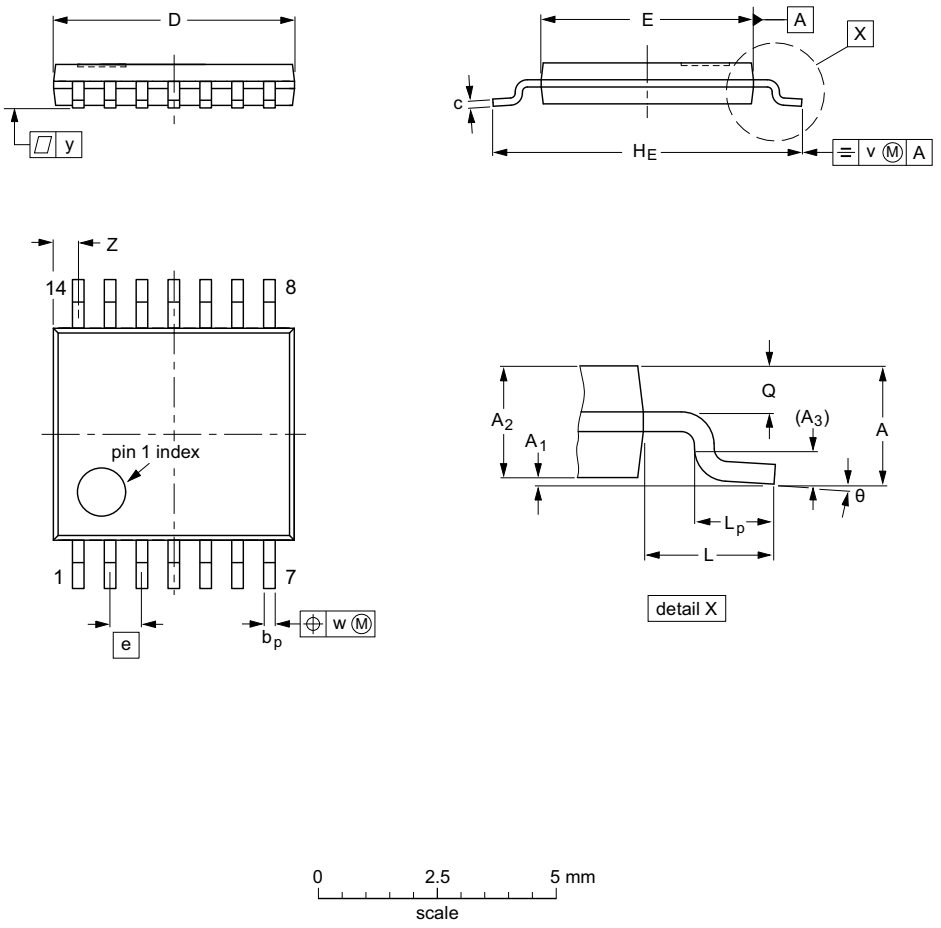
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT337-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT337-1 (SSOP14)**

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | 8°<br>0° |

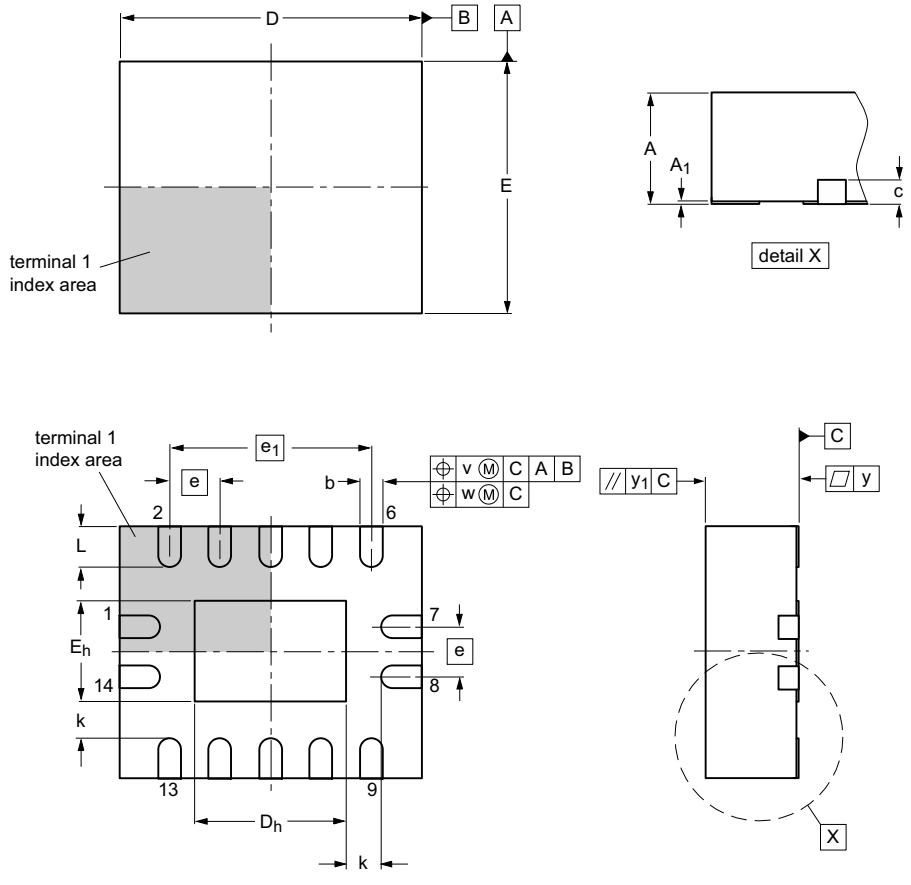
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 11. Package outline SOT402-1 (TSSOP14)**

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm** **SOT762-1**




Dimensions (mm are the original dimensions)

| Unit | | $A^{(1)}$ | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | k | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1 | 0.05 | 0.30 | | 3.1 | 1.65 | 2.6 | 1.15 | | | | 0.5 | | | | |
| mm | nom | | 0.02 | 0.25 | 0.2 | 3.0 | 1.50 | 2.5 | 1.00 | 0.5 | 2 | | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | | 0.00 | 0.18 | | 2.9 | 1.35 | 2.4 | 0.85 | | | 0.2 | 0.3 | | | | |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot762-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT762-1 | | MO-241 | | | | ~~15-04-10~~ 15-05-05 |

**Fig 12. Package outline SOT762-1 (DHVQFN14)**

## 13. Abbreviations

**Table 9. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVT_LVTH125 v.7 | 20160531 | Product data sheet | - | 74LVT125 v.6 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LVT_LVTH125 v.6 | 20060306 | Product data sheet | - | 74LVT125 v.5 |
| Modifications: | • Section 3: Added type numbers 74LVTH125D, 74LVTH125DB, 74LVTH125PW and 74LVTH125BQ. | | | |
| 74LVT125 v.5 | 20050210 | Product data sheet | - | 74LVT125 v.4 |
| 74LVT125 v.4 | 20050207 | Product data sheet | - | 74LVT125 v.3 |
| 74LVT125 v.3 | 20040624 | Product data sheet | - | 74LVT125 v.2 |
| 74LVT125 v.2 | 19980219 | Product specification | - | 74LVT125 v.1 |
| 74LVT125 v.1 | - | - | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 17. Contents





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