

74LVT240

3.3 V Octal inverting buffer/line driver; 3-state

Rev. 3 — 10 April 2017

Product data sheet

1 General description

The 74LVT240 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an octal inverting buffer that is ideal for driving bus lines. The device features two output enable pins ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

2 Features and benefits

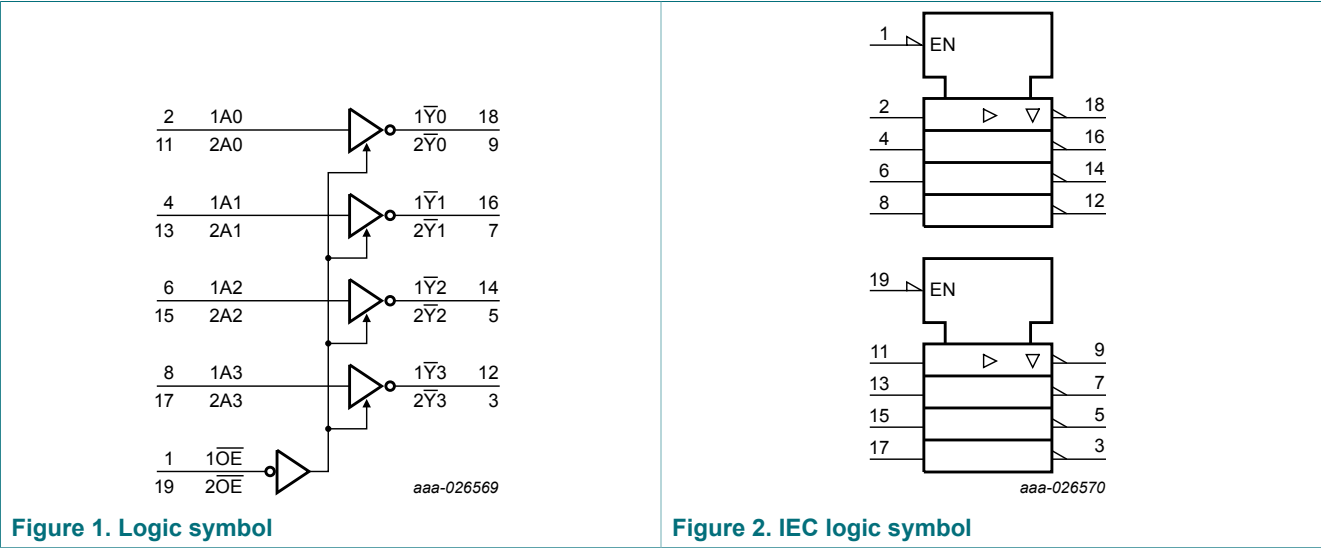
- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
 - JESD78 Class II exceeds 500 mA
- ESD protection:
 - MIL STD 883 method 3015: exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3 Ordering information

Table 1. Ordering information

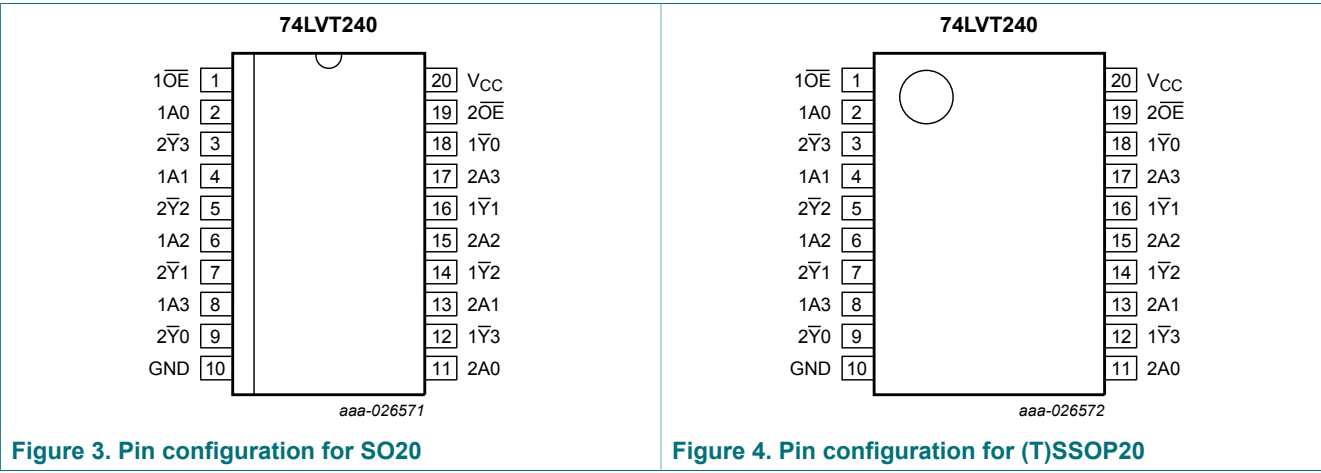
Type number	Package			
	Temperature range	Name	Description	Version
74LVT240D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT240DB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT240PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4 Functional diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
V _{CC}	20	supply voltage

6 Functional description

Table 3. Function table ^[1]

Inputs		Outputs
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_J	junction temperature	[2]	-	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to $+85$ °C [3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
I_{OH}	HIGH-level output current		-32	-	mA
I_{OL}	LOW-level output current		-	32	mA
		current duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	64	mA
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IK}	input clamping voltage	$V_{CC} = 2.7\text{ V}; I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}; I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7\text{ V}; I_{OH} = -8\text{ mA}$	2.4	2.5	-	V
		$V_{CC} = 3.0\text{ V}; I_{OH} = -32\text{ mA}$	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7\text{ V}; I_{OL} = 100\text{ }\mu\text{A}$		0.1	0.2	V
		$V_{CC} = 2.7\text{ V}; I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}; I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$V_{CC} = 3.0\text{ V}; I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}; I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
I_I	input leakage current	all input pins				
		$V_{CC} = 0\text{ V or }3.6\text{ V}; V_I = 5.5\text{ V}$	-	1	10	μA
		control pins				
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}$	-	± 0.1	± 1	μA
		data pins ^[2]				
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}$	-	0.1	1	μA
		$V_{CC} = 3.6\text{ V}; V_I = 0\text{ V}$	-5	-1	-	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}; V_I\text{ or }V_O = 0\text{ V to }4.5\text{ V}$	-	1	± 100	μA
I_{BHL}	bus hold LOW current	$V_{CC} = 3.0\text{ V}; V_I = 0.8\text{ V}$	75	150	-	μA
I_{BHH}	bus hold HIGH current	$V_{CC} = 3.0\text{ V}; V_I = 2.0\text{ V}$	-	-150	-75	μA
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 3.6\text{ V}; V_I = 0\text{ V to }3.6\text{ V}$ ^[3]	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 3.6\text{ V}; V_I = 0\text{ V to }3.6\text{ V}$ ^[3]	-	-	-500	μA
I_{CEX}	output high leakage current	$n\bar{Y}n$ output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}; V_{CC} = 3.0\text{ V}$	-	60	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}; V_O = 0.5\text{ V to }V_{CC}$; $V_I = \text{GND or }V_{CC}$; $n\bar{OE} = \text{don't care}$ ^[4]	-	± 1	± 100	μA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6\text{ V}; V_O = 3.0\text{ V}$	-	1	5	μA
		$V_{CC} = 3.6\text{ V}; V_O = 0.5\text{ V}$	-5	-1	-	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}$				
		outputs HIGH	-	0.12	0.19	mA
		outputs LOW	-	3	12	mA

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
		outputs disabled ^[5]	-	0.12	0.19	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; one input = $V_{CC} - 0.6\text{ V}$; other inputs at V_{CC} or GND ^[6]	-	0.1	0.2	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or 3.0 V	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or 3.0 V	-	8	-	pF

[1] All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms . From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of 100 ms is permitted. This parameter is valid for $T_{amb} = +25\text{ }^{\circ}\text{C}$ only.

[5] I_{CC} with the outputs disabled is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10 Dynamic characteristics

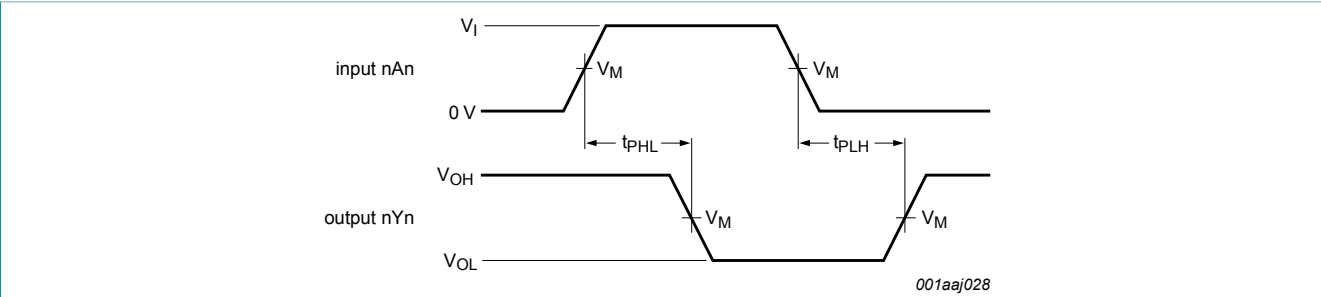
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$						
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Figure 5				
		$V_{CC} = 2.7\text{ V}$	-	-	5.2	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.5	4.3	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Figure 5				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.5	4.3	ns
t_{PZH}	OFF-state to HIGH propagation delay	nOE to nYn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.7	5.2	ns
t_{PZL}	OFF-state to LOW propagation delay	nOE to nYn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	6.7	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.1	5.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	nOE to nYn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2.0	3.4	5.6	ns
t_{PLZ}	LOW to OFF-state propagation delay	nOE to nYn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	5.6	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.6	3.2	5.1	ns

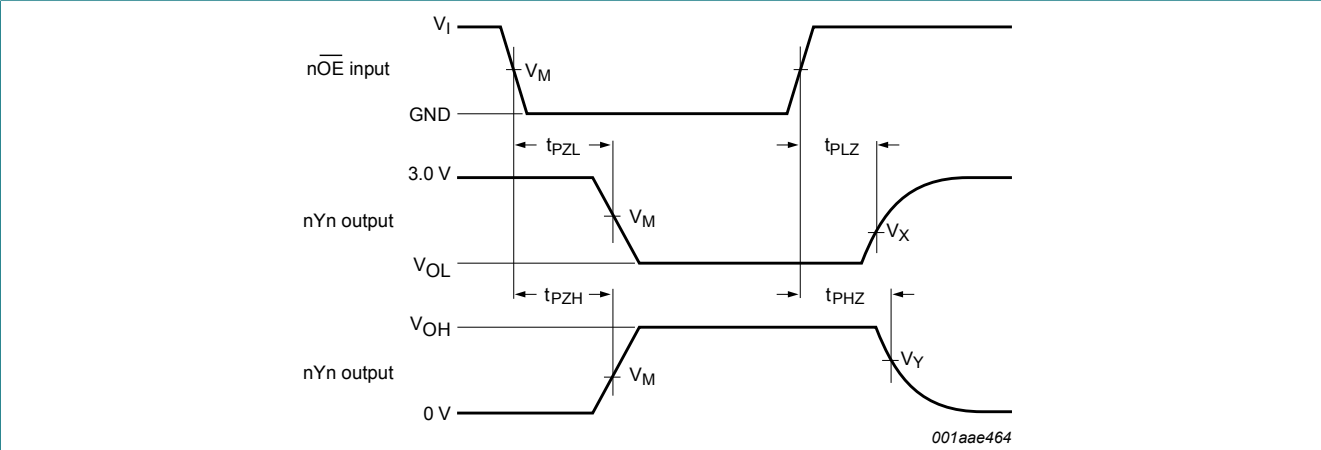
[1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.3\text{ V}$.

10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Input (nAn) to output (nYn) propagation delays

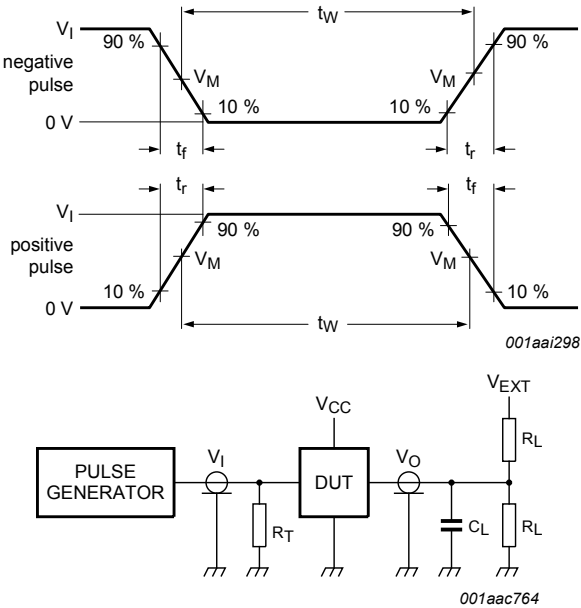


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. 3-state enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = Load capacitance including jig and probe capacitance.
 R_L = Load resistance.

Figure 7. Test circuit for measuring switching times

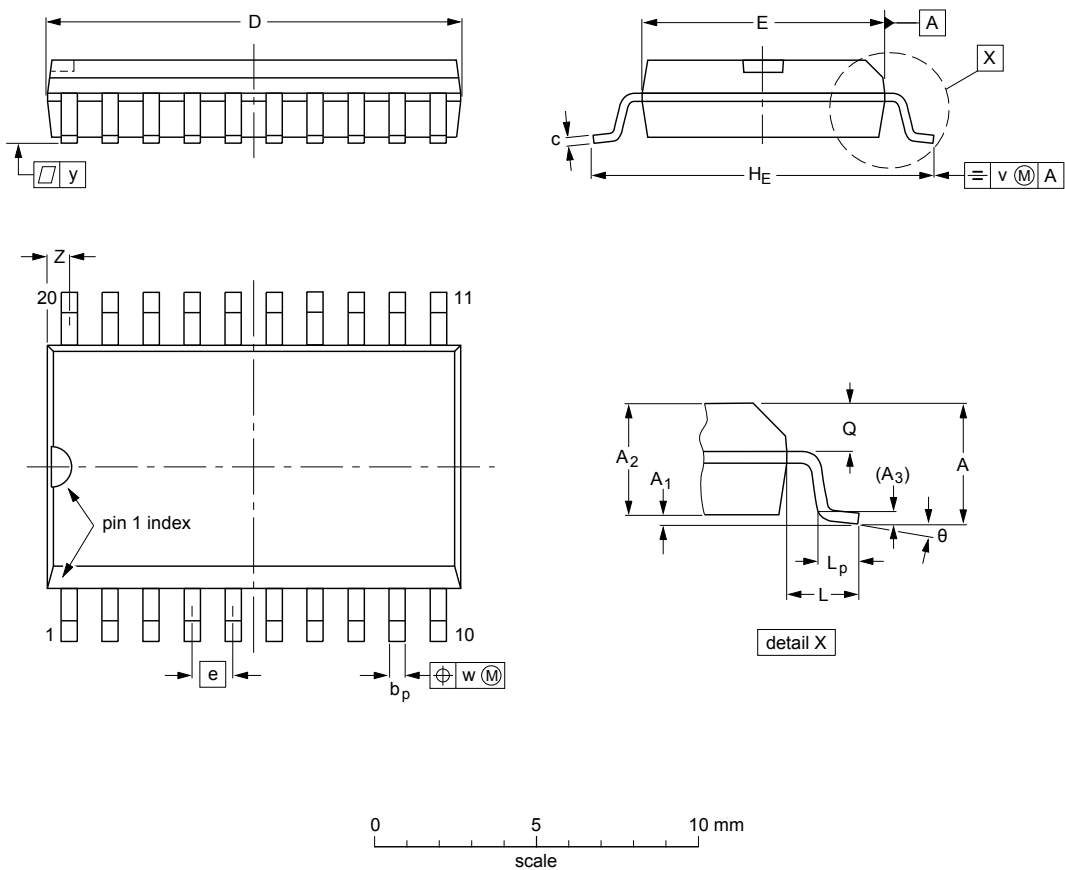
Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

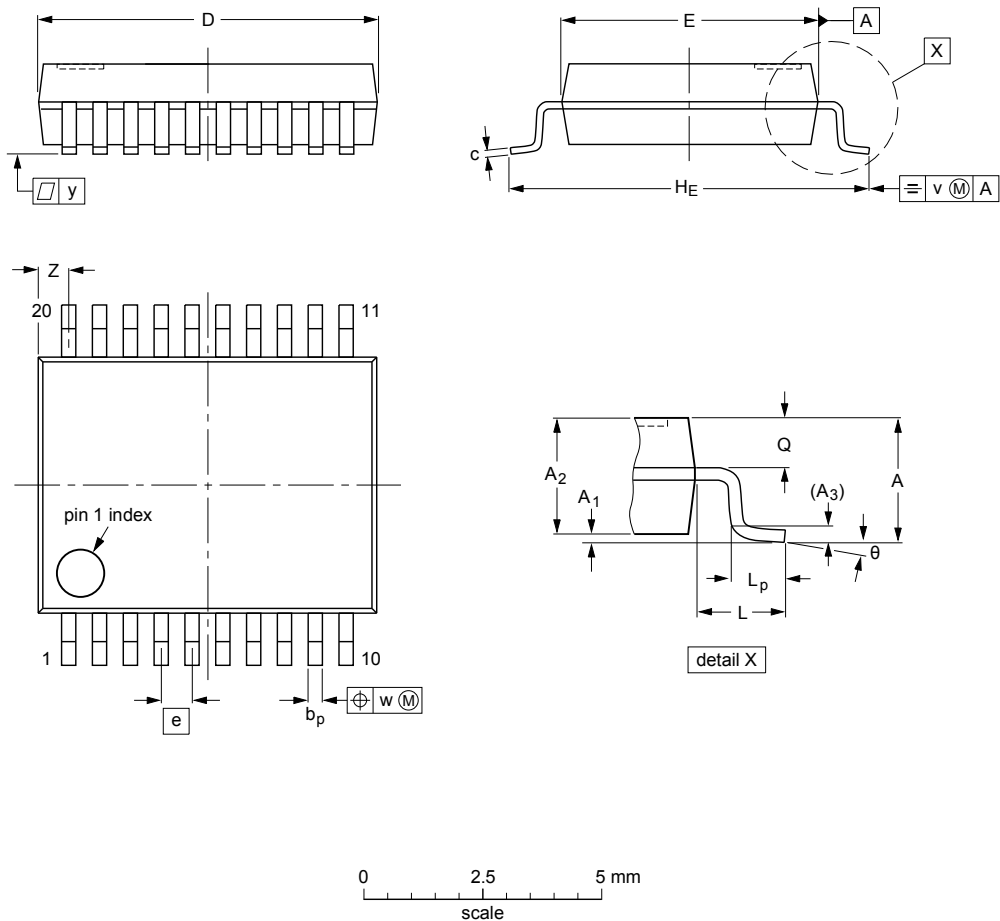
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Figure 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

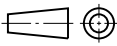
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27- 03-02-19

Figure 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

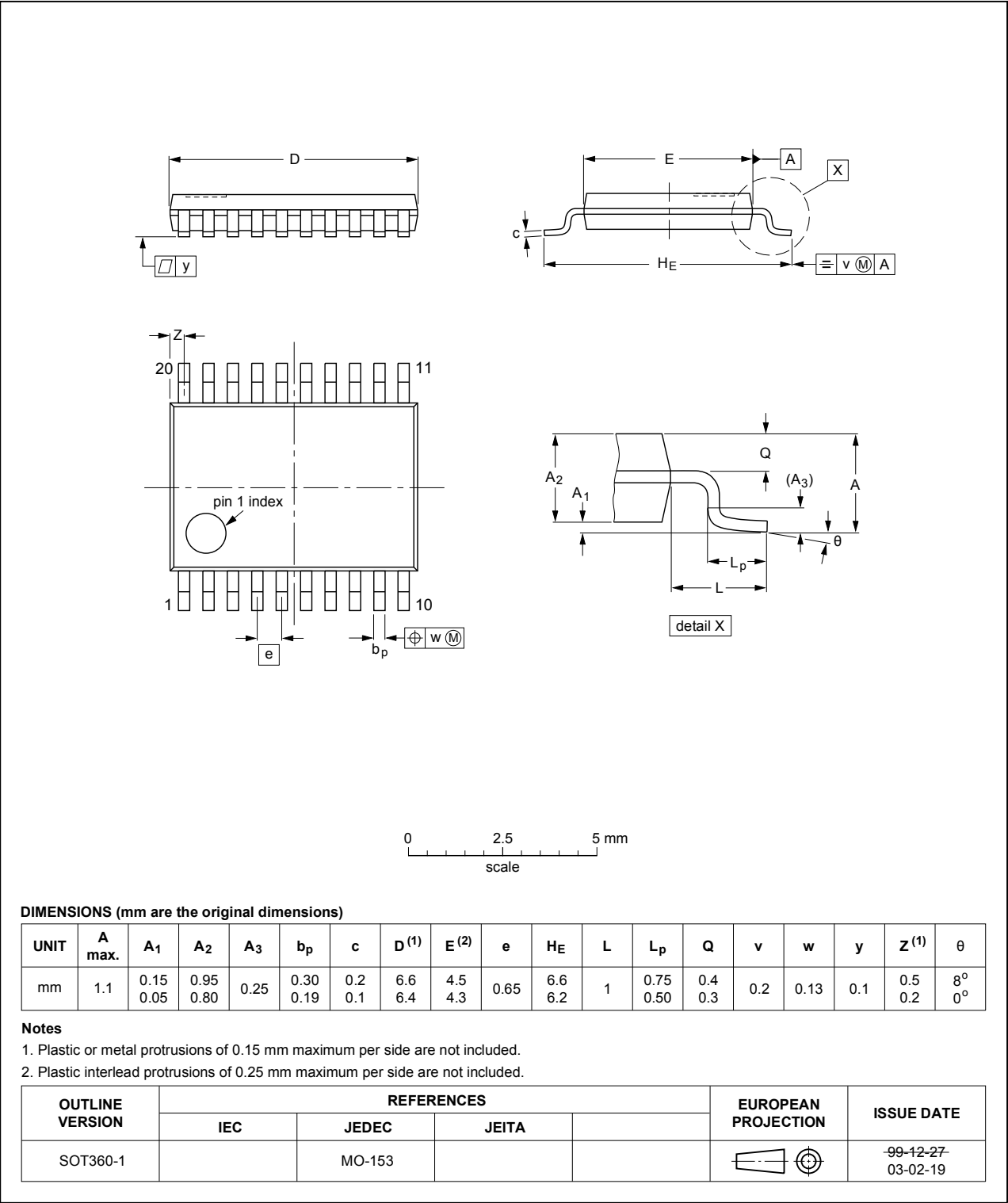


Figure 10. Package outline SOT360-1 (TSSOP20)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT240 v.3	20170410	Product data sheet	-	74LVT240 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74LVT240 v.2	19980219	Product specification	-	74LVT240 v.1
74LVT240 v.1	19940516	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

14.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia. In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical

systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

3.3 V Octal inverting buffer/line driver; 3-state

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer

design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	2
5.1	Pinning	2
5.2	Pin description	3
6	Functional description	3
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	6
10.1	Waveforms and test circuit	7
11	Package outline	9
12	Abbreviations	12
13	Revision history	12
14	Legal information	13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© Nexperia B.V. 2017.

All rights reserved.

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 10 April 2017
Document identifier: 74LVT240