74LVT2952

3.3 V Octal registered transceiver; 3-State

Rev. 4 — 11 September 2013 Product data sheet

1. General description

The 74LVT2952 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses.

Data applied to the inputs is entered and stored on the rising edge of the clock (CPxx) if the clock enable ($\overline{CE}$xx) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable ($\overline{OE}$xx)) is LOW. Data flow from An inputs to Bn outputs is the same as for Bn inputs to An outputs.

2. Features and benefits

- 8-bit registered transceiver
- Independent registers for A and B buses
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT2952D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVT2952DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVT2952PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Functional diagram

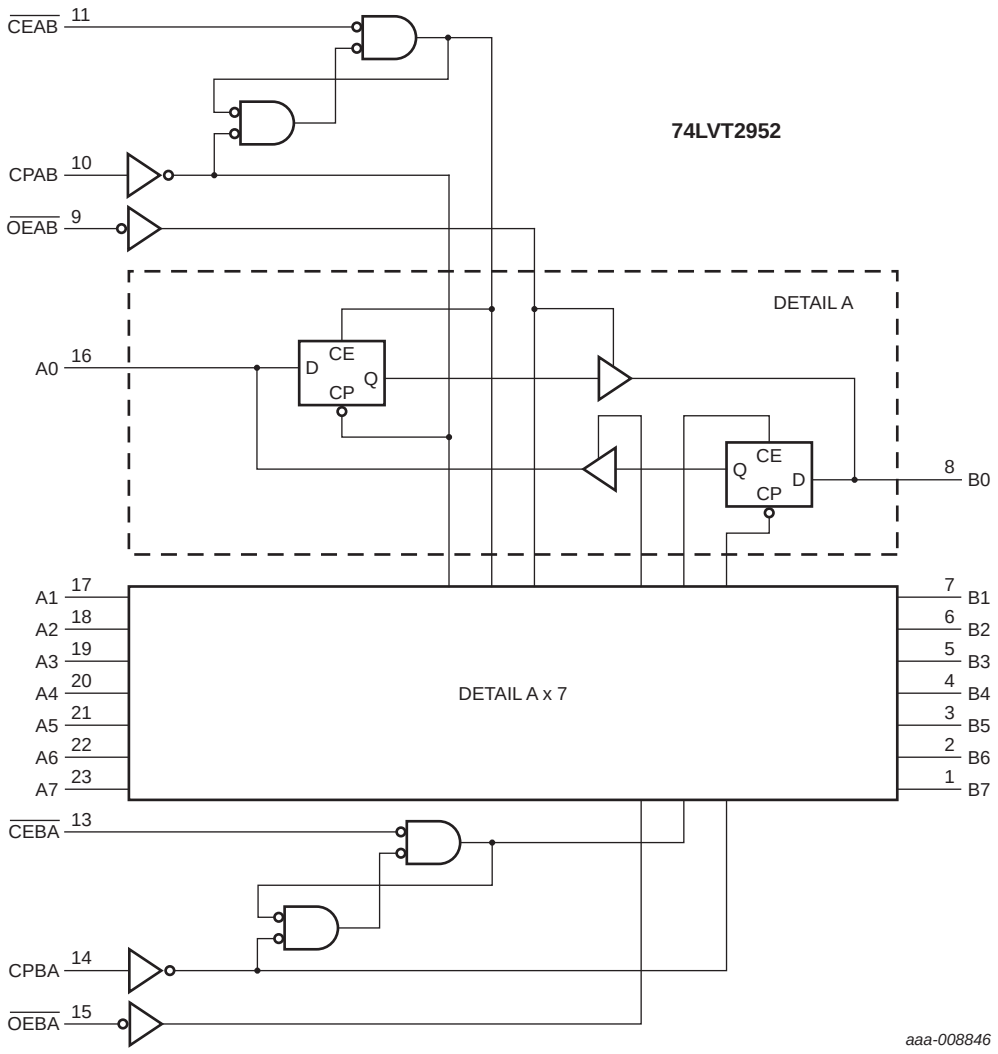


Fig 1. Logic diagram

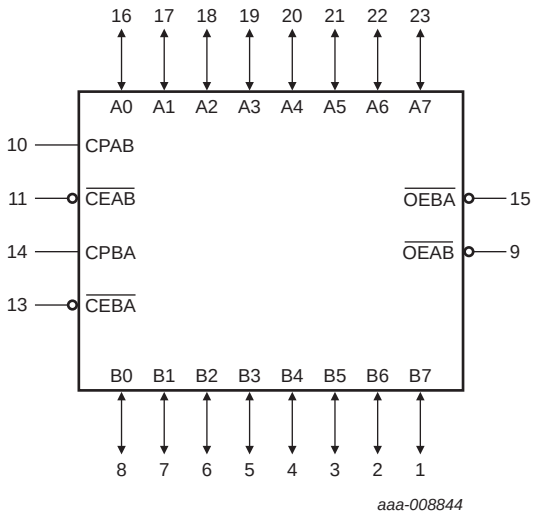


Fig 2. Logic symbol

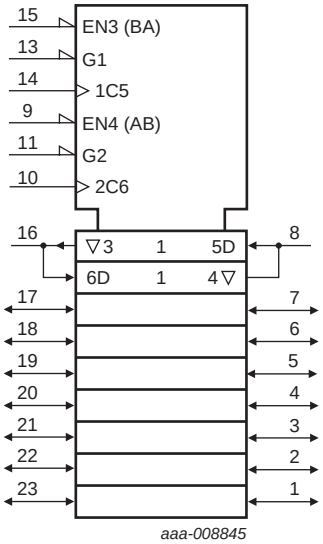


Fig 3. IEC logic symbol

5. Pinning information

5.1 Pinning

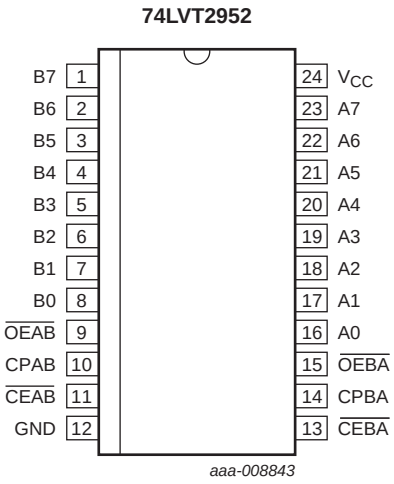


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
B7 to B0	1, 2, 3, 4, 5, 6, 7, 8	data input/output (B side)
$\overline{OEAB}$, $\overline{OEBA}$	9, 15	output enable input (active LOW)
CPAB, CPBA	10, 14	clock input
$\overline{CEAB}$, $\overline{CEBA}$	11, 13	clock enable input
GND	12	ground (0 V)
A0 to A7	16, 17, 18, 19, 20, 21, 22, 23	data input/output (A side)
V_{CC}	24	supply voltage

6. Functional description

Table 3. Function selection[1]

Inputs			Internal	Operating mode
An, Bn	CPxx[2]	$\overline{CExx}$[2]		
X	X	H	nc	hold data
L	↑	L	L	load data
H	↑	L	H	load data

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition;
nc = no change.

[2] xx = AB or BA.

Table 4. Function selection[1]

Inputs	Internal Q	An, Bn outputs	Operating mode
$\overline{OExx}$[2]			
H	X	Z	outputs disabled
L	L	L	outputs enabled
L	H	H	outputs enabled

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high impedance OFF-state.

[2] xx = AB or BA.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1][2]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[3]	–0.5	7.0	V
V_O	output voltage	output in OFF or HIGH state	[3]	–0.5	+7	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW state		-	128	mA
		output in HIGH state		–64	-	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[4]	-	500	mW

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[4] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
I_{OH}	HIGH-level output current		-	–32	mA
I_{OL}	LOW-level output current		-	32	mA
		current duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	64	mA
T_{amb}	ambient temperature	in free air	–40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	output enabled	-	10	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		–1.2	–0.9	-	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC} – 0.1	-	V
		V_{CC} = 2.7 V; I_{OH} = –8 mA		2.4	2.5	-	
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA		-	0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA		-	0.25	0.4	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 64 mA		-	0.4	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC}	[2]	-	0.13	0.55	V
I_I	input leakage current	control pins					
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	1	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	±0.1	±1	µA
		I/O data pins	[3]				
		V_{CC} = 3.6 V; V_I = 5.5 V		-	1	20	µA
		V_{CC} = 3.6 V; V_I = V_{CC}		-	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V		–5	–1	-	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	1	±100	µA
I_{LO}	output leakage current	V_O = 5.5 V; V_{CC} = 3.6 V; output HIGH		-	60	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq$ 1.2 V V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OExx}$ = don't care	[4]	-	1	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3.0 V; V_I = 0.8 V		75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3.0 V; V_I = 2.0 V		-	–150	–75	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 0 V to 3.0 V; V_I = 3.6 V	[5]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 0 V to 3.0 V; V_I = 3.6 V	[5]	-	-	–500	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A					
		outputs HIGH		-	0.13	0.19	mA
		outputs LOW		-	3	12	mA
		outputs disabled		-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input = V_{CC} – 0.6 V; other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_I	input capacitance	control inputs; outputs disabled; V_I = 0 V or 3.0 V		-	4	-	pF

Table 7. Static characteristics *…continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$C_{I/O}$	input/output capacitance	at I/O data pins, outputs disabled; $V_{I/O}$ = 0 V or 3.0 V	-	8	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 ms is permitted. This parameter is valid for T_{amb} = +25 °C only.

[5] This parameter is the bus hold overdrive current required to force the input to the opposite logic state.

[6] This parameter is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Figure 8.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{PLH}	LOW to HIGH propagation delay	CPBA to An or CPAB to Bn; see Figure 5				
		V_{CC} = 2.7 V	-	-	7.1	ns
		V_{CC} = 3.3 V ± 0.3 V	1.3	3.1	6.1	ns
t_{PHL}	HIGH to LOW propagation delay	CPBA to An or CPAB to Bn; see Figure 5				
		V_{CC} = 2.7 V	-	-	6.9	ns
		V_{CC} = 3.3 V ± 0.3 V	1.8	3.8	6.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OEBA}$ to An; $\overline{OEAB}$ to Bn; see Figure 7				
		V_{CC} = 2.7 V	-	-	6.7	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.4	5.6	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OEBA}$ to An; $\overline{OEAB}$ to Bn; see Figure 7				
		V_{CC} = 2.7 V	-	-	8.0	ns
		V_{CC} = 3.3 V ± 0.3 V	1.2	3.6	6.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OEBA}$ to An; $\overline{OEAB}$ to Bn; see Figure 7				
		V_{CC} = 2.7 V	-	-	6.9	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.7	6.3	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OEBA}$ to An; $\overline{OEAB}$ to Bn; see Figure 7				
		V_{CC} = 2.7 V	-	-	5.3	ns
		V_{CC} = 3.3 V ± 0.3 V	1.6	3.4	5.1	ns
$t_{su(H)}$	set-up time HIGH	An to CPAB or Bn to CPBA; see Figure 7				
		V_{CC} = 2.7 V	2.8	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	2.5	1.0	-	ns
		$\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA; see Figure 7				
		V_{CC} = 2.7 V	0.8	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	0.9	0.3	-	ns

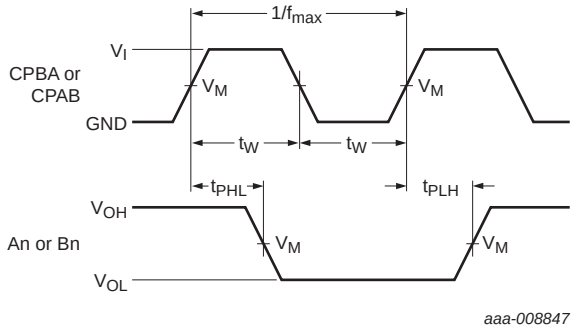
Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit, see Figure 8.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$t_{su(L)}$	set-up time LOW	An to CPAB or Bn to CPBA; see Figure 7				
		V_{CC} = 2.7 V	3.0	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	2.5	1.0	-	ns
		$\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA; see Figure 7				
		V_{CC} = 2.7 V	2.7	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	2.4	–0.3	-	ns
$t_{h(H)}$	hold time HIGH	An to CPAB or Bn to CPBA; see Figure 7				
		V_{CC} = 2.7 V	0.7	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	1.5	–0.5	-	ns
		$\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA; see Figure 7				
		V_{CC} = 2.7 V	0.7	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	2.5	0.3	-	ns
$t_{h(L)}$	hold time LOW	An to CPAB or Bn to CPBA; see Figure 7				
		V_{CC} = 2.7 V	2.6	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	1.5	–0.5	-	ns
		$\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA; see Figure 7				
		V_{CC} = 2.7 V	2.6	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	2.5	0	-	ns
t_W	pulse width	CPAB or CPBA; HIGH or LOW; see Figure 5				
		V_{CC} = 2.7 V	3.3	-	-	ns
		V_{CC} = 3.3 V ± 0.3 V	3.3	1.0	-	ns
f_{max}	maximum frequency	CPBA, CPAB; V_{CC} = 3.3 V ± 0.3 V; see Figure 5	150	200	-	MHz

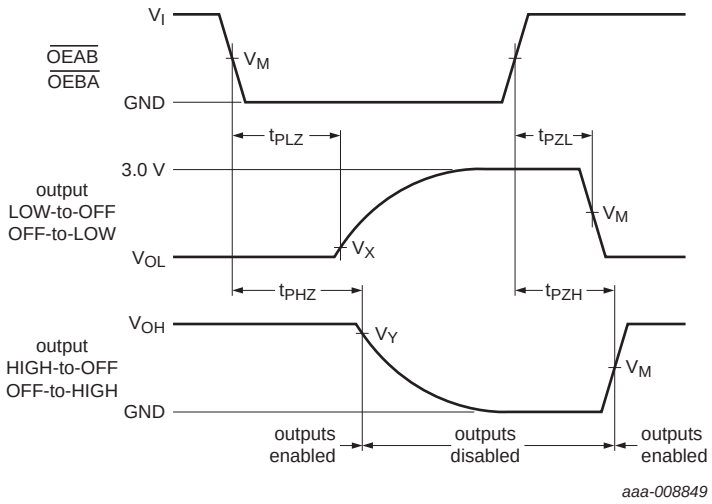
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

11. Waveforms



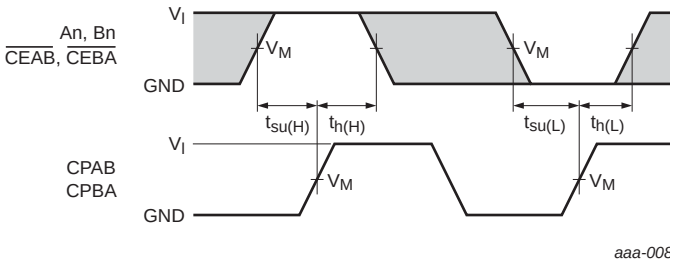
See Table 9 for measurement points

Fig 5. Clock input to output propagation delay, clock pulse width and maximum frequency



See Table 9 for measurement points

Fig 6. 3-state output enable and disable times



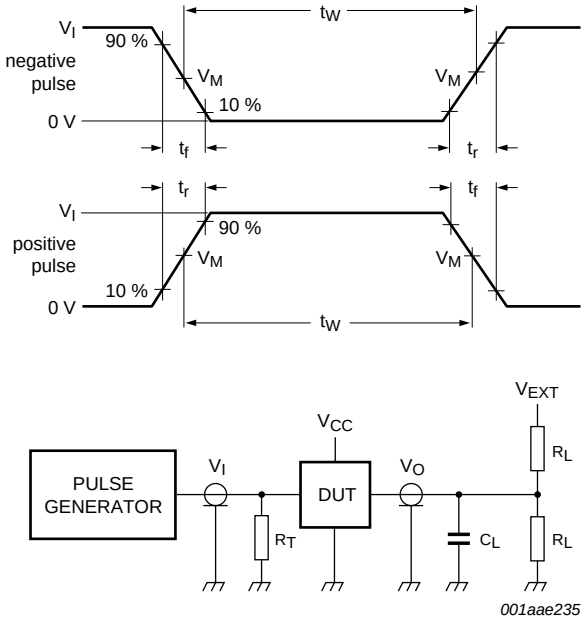
See Table 9 for measurement points

The shaded areas indicate when the input is permitted to change for predictable output performance

Fig 7. Data setup and hold times

Table 9. Measurement points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
2.7 V to 3.6 V	GND to 2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

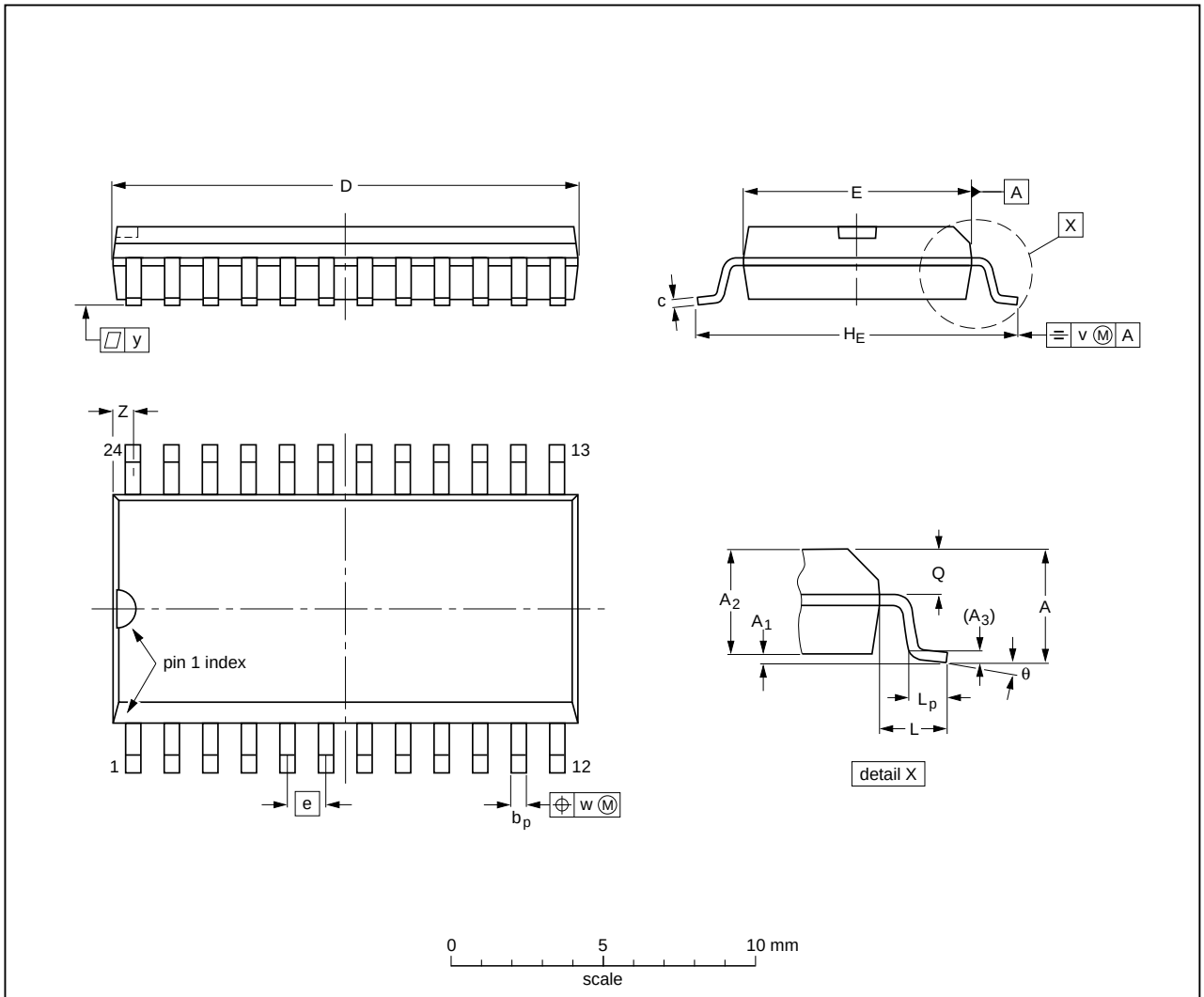
Fig 8. Test circuit for switching times

Table 10. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

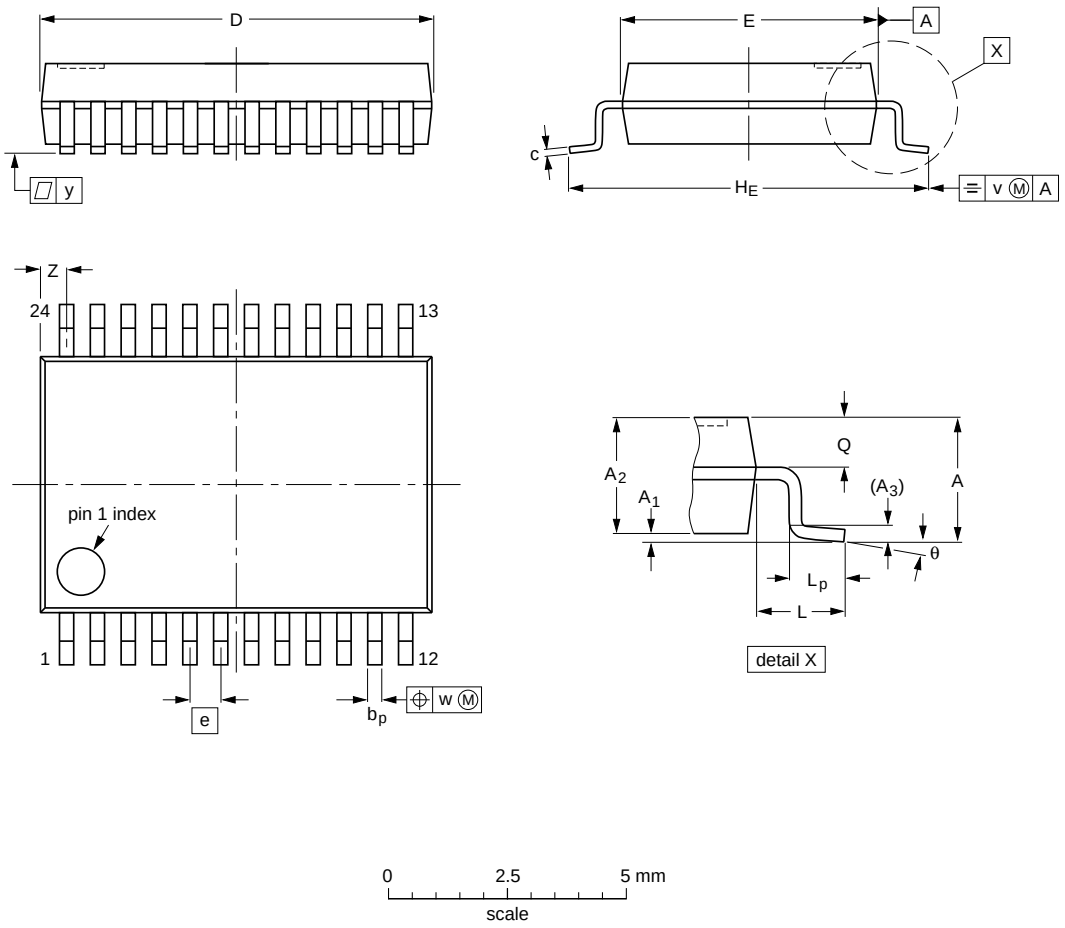
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

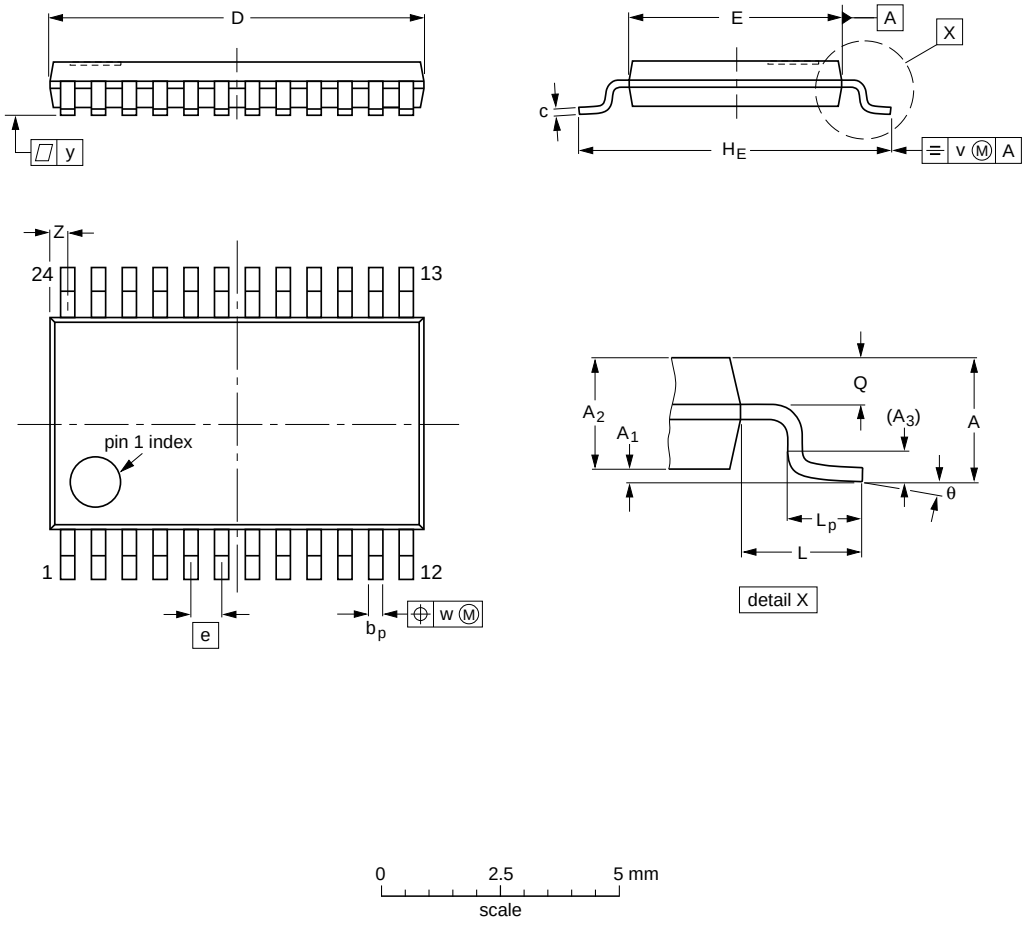
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT2952 v.4	20130911	Product data sheet	-	74LVT2952 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74LVT2952 v.3	20040907	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

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