FAIRCHILD

SEMICONDUCTOR ™

August 2001
Revised August 2001

74LVT32373 • 74LVTH32373
Low Voltage 32-Bit Transparent Latch
with 3-STATE Outputs (Preliminary)

General Description

The LVT32373 and LVTH32373 contain thirty-two non-inverting latches with 3-STATE outputs and are intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The LVTH32373 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT32373 and LVTH32373 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

■ Input and output interface capability to systems at 5V V_{CC}

■ Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH32373), also available without bushold feature (74LVT32373)

■ Live insertion/extraction permitted

■ Power Up/Down high impedance provides glitch-free bus loading

■ Outputs source/sink −32 mA/+64 mA

■ ESD performance:
  Human-body model > 2000V
  Machine model > 200V
  Charged-device model > 1000V

■ Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

| Order Number	Package Number	Package Description
74LVT32373GX (Note 1)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LVTH32373GX (Note 1)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

Note 1: BGA package available in Tape and Reel only.

Logic Symbol
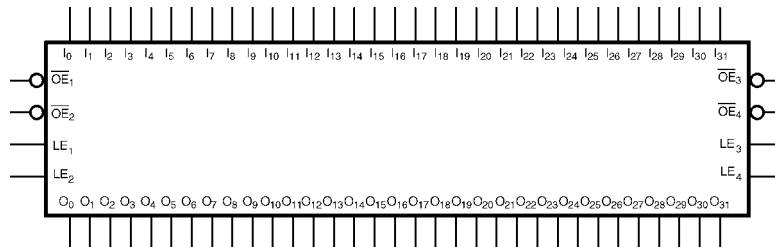
74LVT32373 • 74LVTH32373

Connection Diagram
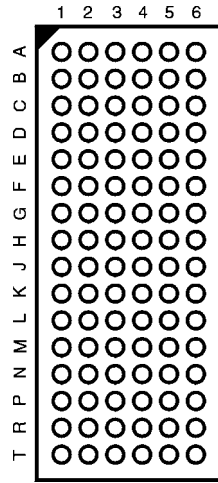
(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0–I_{31}	Inputs
O_0–O_{31}	3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	$\overline{OE}_1$	LE_1	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC1}	V_{CC1}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC1}	V_{CC1}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	$\overline{OE}_2$	LE_2	I_{15}	I_{14}
J	O_{17}	O_{16}	$\overline{OE}_3$	LE_3	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC2}	V_{CC2}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC2}	V_{CC2}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	$\overline{OE}_4$	LE_4	I_{31}	I_{30}

Truth Table

Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
CP_3	$\overline{OE}_3$	I_{16}–I_{23}	O_{16}–O_{23}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
CP_4	$\overline{OE}_4$	I_{24}–I_{31}	O_{24}–O_{31}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level   L = LOW Voltage Level   X = Immaterial   Z = HIGH Impedance O_o = Previous O_0 prior to HIGH-to-LOW transition of LE

Functional Description

The LVT32373 and LVTH32373 contain thirty-two D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 32-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e, a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams

Byte 1 (0:7)

Byte 2 (8:15)

Byte 3 (16:23)

Byte 4 (24:31)
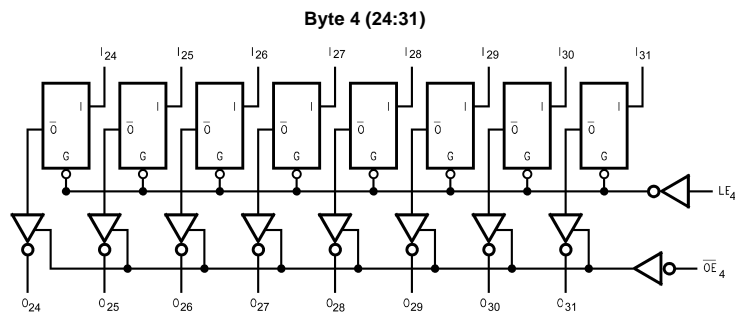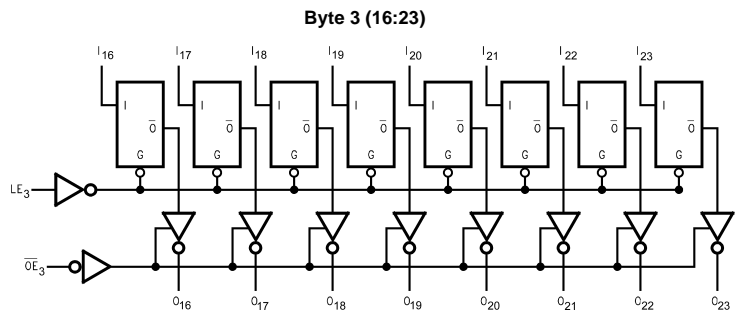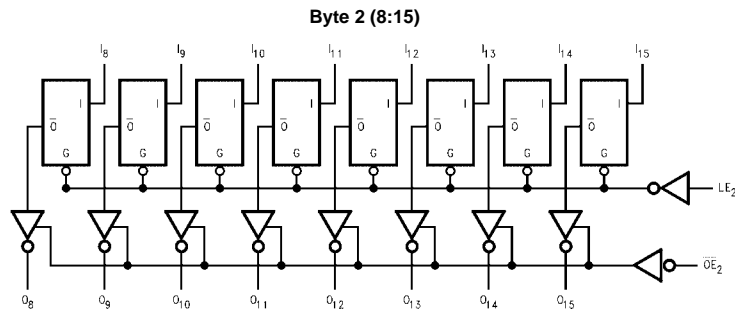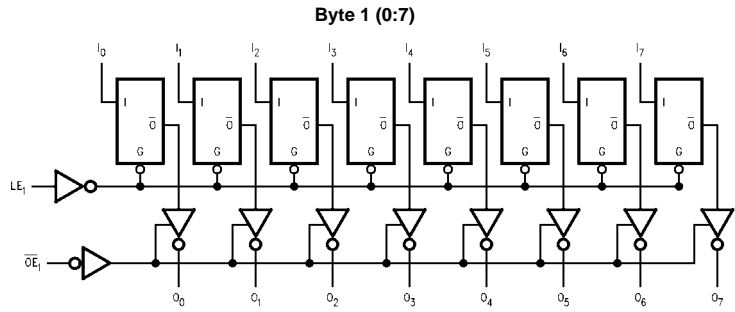
V_{CC1} is associated with Bytes 1 and 2.

V_{CC2} is associated with Bytes 3 and 4.

Note: Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		−32	mA
I_{OL}	LOW Level Output Current		64	mA
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40°C to +85°C Min	Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \leq$ 0.1V or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8	V	$V_O \geq V_{CC}$ − 0.1V
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC} − 0.2		V	I_{OH} = −100 μA
			2.7	2.4			I_{OH} = −8 mA
			3.0	2.0			I_{OH} = −32 mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	I_{OL} = 100 μA
			2.7		0.5		I_{OL} = 24 mA
			3.0		0.4		I_{OL} = 16 mA
			3.0		0.5		I_{OL} = 32 mA
			3.0		0.55		I_{OL} = 64 mA
$I_{I(HOLD)}$ (Note 4)	Bushold Input Minimum Drive		3.0	75		μA	V_I = 0.8V
				−75			V_I = 2.0V
$I_{I(OD)}$ (Note 4)	Bushold Input Over-Drive Current to Change State		3.0	500		μA	(Note 5)
				−500			(Note 6)
I_I	Input Current		3.6		10		V_I = 5.5V
		Control Pins	3.6		±1	μA	V_I = 0V or V_{CC}
		Data Pins	3.6		−5		V_I = 0V
					1		$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	μA	0V $\leq V_I$ or $V_O \leq$ 5.5V
$I_{PU/PD}$	Power up/down 3-STATE Output Current		0–1.5V		±100	μA	V_O = 0.5V to 3.0V V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	μA	V_O = 0.5V
I_{OZH}	3-STATE Output Leakage Current		3.6		5	μA	V_O = 3.0V
I_{OZH}+	3-STATE Output Leakage Current		3.6		10	μA	$V_{CC} < V_O \leq$ 5.5V

Sidebar (vertical text, left margin): **74LVT32373 • 74LVTH32373 Low Voltage 32-Bit Transparent Latch with 3-STATE Outputs (Preliminary)**

Physical Dimensions inches (millimeters) unless otherwise noted

Top View

Bottom View

PIN ONE

1.4 MAX

SEATING PLANE

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A
Preliminary

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